

"A Digital Semiconductor Monolithic Integrated Circuit"

The present invention relates to a digital semiconductor monolithic integrated circuit. More particularly, the invention relates to a digital semiconductor monolithic integrated circuit containing an analog to digital converter
5 (which will hereinafter be referred to as the "A/D converter") for forming at least a part of a digital control system.

A digital control system can have its size reduced by using a semiconductor integrated circuit. Moreover,
10 the digital control system can achieve a high reliability by a substantial reduction in the number of the external wires connected to the semiconductor integrated circuit.

In order to provide a system control of high
15 quality, a control system such as a process control system (making use of a microprocessor) or a computing control system is made receptive of not only the signals of various kinds of sensors (which will be referred to as the "digital sensors") made operative of digital or
20 pulse signals but also analog signals which carry information through the A/D converter.

In this case, both an input circuit (i.e., a digital input circuit) for feeding the data signal from a digital sensor to the data bus of a microprocessor and an input circuit (i.e., an analog input circuit) for feeding the data signal from an analog sensor to the data bus after it has been converted into a digital signal, are constructed from a one-chip monolithic semiconductor integrated circuit (which will hereinafter be referred to as the "monolithic IC" or "IC") in order partly to reduce the size of the device constituting the system and partly to reduce the number of the external connections to the device, as has been mentioned above.

Furthermore, it is desirable that the monolithic IC be constructed so that it can be applied to a number of different types of control systems.

By providing a universal type of monolithic IC, this monolithic IC can be used in a variety of different control systems so that the maintenance of the various control systems can be facilitated. Moreover, any change or development in the control systems can also be facilitated.

However, it should be noted that in the usual type of monolithic IC, the number of the external terminals to be attached to the package is limited by the size of the package.

In the case where the number of the external terminals to be attached to the IC package is limited so that the numbers of both analog and digital input

terminals are accordingly limited, the monolithic IC has its applicability limited to only one specified control system.

For example, in the case where a monolithic IC has had its digital input terminals relatively reduced by the provision of an increase in the number of the analog input terminals, such a monolithic IC cannot be readily used in a control system having a relatively large number of digital input signals. On the contrary, the monolithic IC, which has its analog input terminals substantially reduced by the provision of a relatively large number of the digital input terminals, is difficult to adapt for use in a control system which is fed with a relatively large number of analog input signals.

Accordingly, the above described monolithic IC cannot be readily adapted to be used for different control systems.

For example, the output data signal from the analog sensor has its level made proportional to the physical quantity to be detected so that it can bear more information than that output data signal from the digital sensor, which is made to correspond to whether the physical quantity to be detected exceeds a certain threshold level or not. Therefore, the control system developed in advance can be easily changed, if the digital sensor can be replaced by the analog sensor, into such a control system as can perform a system control

of higher quality. However, in the case where the monolithic IC having its digital input terminals relatively increased is used, the above referred to system change becomes difficult because the analog input terminals are relatively reduced.

In the case where the monolithic IC is to be equipped with the analog and digital input terminals required, the size of its package has to be enlarged because of the increase in the number of external terminals.

It is an object of the present invention to provide a semiconductor integrated circuit which forms at least a part of a digital control system and which exhibits a good adaptability even with a relatively small number of external terminals.

According to one aspect of the present invention there is provided a digital semiconductor^{monolithic} integrated circuit including:

- a plurality of external terminals;
- a digital signal input circuit;
- an analog signal input circuit responsive to an analog input signal for supplying a digital signal corresponding to said analog input signal; and
- at least one common terminal for connecting input terminals of said digital signal input circuit and said analog signal input circuit with at least one of said plurality of external terminals.

According to another aspect of the present

invention there is provided a digital semiconductor monolithic integrated circuit including :

- a plurality of external terminals;
- a digital signal input/output circuit;
- 5 an analog signal input circuit responsive to an analog input signal for supplying a digital signal corresponding to said analog input signal; and
- at least one common terminal for connecting the input/output terminals of said digital signal input/output circuit
- 10 and the input terminal of said analog signal input circuit with at least one of said plurality of external terminals.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein :-

15 Figure 1 is a block diagram showing the circuit of one preferred embodiment of a digital semiconductor monolithic integrated circuit control system;

Figure 2 is a block diagram showing part of the circuit blocks shown in Figure 1 in greater detail; and

20 Figure 3 is a block diagram showing the circuit of a second embodiment of a digital semiconductor monolithic integrated circuit control system.

Referring first to Figure 1, the digital semiconductor monolithic integrated circuit control system

25 includes a micro-processor 1 which is constructed in the form of a one-chip monolithic semiconductor integrated circuit

composed of circuit blocks 2 to 18.

The micro-processor includes: an accumulator 2 which has its data input and output terminals coupled to an internal data bus line BUS; an accumulator latch circuit 3 which is coupled to the accumulator 2; a temporary register 4 which has its data input and output terminals coupled to the internal data bus line BUS; and an arithmetic and logic unit 5 which receives the output data of the accumulator latch circuit 3 and the temporary register 4 as its operand. The circuits 2 to 5 together constitute an arithmetic unit and have their respective operations controlled by the control signals which are generated by a timing control circuit 8.

The arithmetic and logic unit 5 has its operation controlled by the output signal of the timing control circuit 8 so as to perform an arithmetic operation such as addition or subtraction or an OR, AND, exclusive or logical operation.

The output data of the arithmetic and logic unit 5 are different in accordance with the control signal, which is generated by the timing control circuit 8, and are supplied to the accumulator 2 through the internal data bus line BUS.

The micro-processor further includes an instruction register 6 and an instruction decoder 7 and a machine cycle encoder 2 included within the decoder 7. The circuits 6 to 8 together constitute a control unit.

The instruction register 6 is provided to

receive an instruction which is supplied to the internal data bus line BUS through an external data bus line DT and a data buffer 11 from a read only memory 19 (ROM) which is located outside the micro-processor 1.

- 5 The instruction, which is received by the instruction register 6, is supplied to the construction decoder 7 so that it is decoded thereby. The resultant output of the instruction decoder 7 is fed to the machine cycle encoder Z~~X~~ located within the decoder 7.
- 10 The machine cycle encoder Z~~X~~ generates a variety of timing signals which are determined by the output signal of the instruction decoder 7.

 The timing control circuit 8 has its operational timing controlled by the clock signals fed from grouped external control terminals so that it

15 generates both a bus control signal for receiving the data fed from the external data bus line DT and a strobe signal for writing out the data to the external data bus line DT.

- 20 Moreover, the timing control circuit 8 examines a series of signals such as an interrupt signal fed from the grouped external control terminals, a hold signal for holding the operations of the system and a reset signal so that it feeds out a series of signals
- 25 such as a flag signal indicating the reception of the interruption or a flag signal indicating the reception of the requirement for the hold through the grouped external control terminals in response to those signals

examined.

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The micro-processor further includes a register group 9 which consists of general purpose registers, a stack pointer and a program counter.

5 The general purpose registers of the register group 9 are used for memory operation in addition for handling data (including double length data). The stack pointer is used to memorize the return address of a subroutine jump. The program
10 counter is a register for memorizing the address of the instruction to be subsequently read out, and its data are increased one by one each time one instruction is executed except for when the instruction to be fed to the instruction register 6 is a jump instruction.

15 An address decoder 18 also located within the micro-processor 1 receives the output of the general purpose register of the register group 9 and generates a signal for controlling circuits 15 to 17 to be described hereinafter. It should be noted that the
20 circuit 15 to 17 can be controlled by the general purpose registers of the register group 9. However, by using the address decoder circuit 18, the circuits 15 to 17 can also be controlled even with the use of a small number of the general purpose registers.

25 An address buffer 10 also within the micro-processor 1 receives the output signals from the register group 9 and generates an address signal to be fed to the ROM 19, a RAM 20 and an interface circuit 21.

The data buffer 11 effects interchanges of the data between the external data bus line DT and the internal data bus line BUS.

5 The external terminals P_1 to P_3 of the micro-processor 1 are used as the input terminals for exclusively receiving the analog signals, and the external terminals P_6 and P_7 are used as the input and output terminals for exclusively feeding and receiving the digital signals. The external terminals P_4 and P_5 are
10 used as common terminals for the input of the analog signals and for the input and output of the digital signals.

 The external terminal P_4 is fed with the analog signals which are generated by an analog sensor DET_4 , and the external terminal P_5 is fed with the digital
15 signals which are generated by a switch SW. The external terminal P_6 is fed with the digital signals which are generated by a digital sensor DET_5 . The external terminal P_7 is fed with the digital signals which are used to drive a lamp PL.

20 A digital input/output port also within the micro-processor 1 is connected between the external terminals P_4 to P_7 and the register 15.

 Whether the respective external terminals P_4 to P_7 are used as the digital input terminals or the
25 digital output terminals is determined by the control data which are stored in the register 15.

 The control data to be fed to the register 15 are fed out of the ROM 19 together with the instruction.

The input timing of the control data is controlled by the control signal which is supplied from the address decoder 10 in accordance with the execution of the program written in the ROM 19.

5 The register 15 has stored therein both the digital input data, which are fed through the input/output port 12, and the digital output data which are fed from the internal data bus line BUS until it is to be supplied to the external terminals P₄ to P₇.

10 The digital input data, which are stored in the register 15, are written in the RAM 20 through the internal data bus line BUS and the data buffer 11.

15 All the above referred to operations, that is the storing of the control data in the register 15, the storing of the digital output data, and the reading operation of the digital input data, which are stored in the register 15, are suitably effected in accordance with the program which is written in advance in the ROM 19.

20 For example, at the time of writing the digital input data, which are fed to the external terminal P₅, in the RAM 20, there is fed out of the address decoder 18 the control signal for transferring the stored data of the register 15, which is stored to have a value corresponding to the digital input data fed to the external
25 terminal P₅, to the internal data bus line BUS.

 Likewise, at the time of writing the digital input data, which are fed to the external terminal P₆, in the RAM 20, a control signal similar to the above referred

to one is fed out of the address decoder 18.

Incidentally, the program for writing the digital input data in the RAM 20 which are fed from an element such as the starter switch of an automotive engine, is executed for a predetermined period of time at the start of the engine. On the other hand, the program for writing the digital input data in the RAM 20, which are fed from the crank angle sensor of the engine, is executed once for a relatively short period of several milliseconds.

In order to use the external terminal P_7 as the output terminal for the digital signals, the ROM 19 has stored therein a control data presetting program which is executed immediately after the system is supplied with power from a power source. As a result, the input/output port 12 is controlled by the control data set in the register 15 so as to transfer the digital output data in the register 15 to the external terminal P_7 . A control signal is supplied from the address decoder 18 which is used for setting such digital output data in the register 15 as are fed from the circuit 5 to the internal data bus line BUS.

The micro-processor 1 further includes an analog multiplexor 13 which has its input terminals coupled to the corresponding external terminals P_1 to P_5 , respectively, and its output terminal coupled to the input terminal of an A/D converter 14.

The A/D converter 14 is supplied with that one

of the analog input signals fed to the plural external terminals which is selected by the analog multiplexor 13.

The one external terminal of the plural external terminals and the selected timings thereof which are selected by the analog multiplexor 13 are determined by the control signals which are supplied from a control register 17.

The control signals to be stored in the control register 13 are supplied to the internal data bus line BUS through the data buffer 11 from the ROM 19 written with the program, and the control signals for setting the control signals in the control register 13 are supplied from the address decoder 18.

Incidentally, the respective input timings of the analog input signals are determined by the program which is written in advance in the ROM 19.

For example, the level of the analog input signals to be supplied from a temperature detecting element such as a thermistor is varied at a relatively slow rate. Therefore, it is sufficient that such analog input signals are selected once for a relatively long period. On the other hand, the analog input data to be supplied from a detecting element such as the tachometer of the engine are selected once for a relatively short period.

The analog input data thus selected by the analog multiplexor 13 are converted by the A/D converter 14 into digital data signals of several bits.

The digital data signals supplied from the A/D converter 14 are stored in a register 16.

5 The digital data signals thus stored in the register 16 are transferred to the internal data bus line BUS by the control of the register 16 with the aid of the control signals which are supplied from the address decoder 18. The digital data signals in the internal data bus line BUS are written in the RAM 20 through the data buffer 11.

10 In order to receive the analog input signal fed to one of the external terminals, the group of the programs are executed, both for setting the control signals in the control register 17 and also for transferring the digital data signals from the register 16 to the internal data bus line BUS at the end of the A/D conversion.

15 ~~X~~ The terminal P_5 of the common terminals P_4 and P_5 is fed with the digital signals. Therefore, the signal fed to the common terminal P_5 is not detected as an analog signal.

20 As a result, the ROM 19 does not have stored therein the program for transferring the signal, which is fed to the common terminal P_5 , to the internal data bus line BUS through the analog multiplexer 13, the A/D converter 14 and the register 16.

25 In other words, the ROM 19 does not have the instruction of setting the control signals written therein which instruct the aforementioned terminal P_5 , in the control register 17, The ROM 19 is not written with the

instruction of transferring the set data having no special meaning from the register 16 to the internal data bus line BUS. Thus the A/D converter 14 can be prevented from being unnecessarily operated, and the number of the instructions to be written in the ROM 19 can be reduced. Incidentally, the signals at the terminal P_5 may be unconditionally stored in the register 16 through the analog multiplexor 13 and the A/D converter 14. Even in this case, the terminal P_5 can be prevented from being substantially selected by the fact that the instruction of transferring the data from the register 16 to the internal data bus line BUS is not written in the ROM 19.

It should be noted that the common terminals P_4 and P_5 are used as the analog signal input terminal or the digital signal input terminal, and that the input/output port 12 is made to exhibit high output impedance characteristics for the terminals P_4 and P_5 . As a result, the analog input signal level or the digital input signal level to be supplied to the terminals P_4 and P_5 is prevented from being affected by the input/output port 12.

The construction and operation of the circuits described above will now be described in greater detail with reference to Figure 2.

Referring to Figure 2, the multiplexor 13 comprises transfer gate MISFETs Q_{16} to Q_{20} which have their respective gate electrodes coupled to the control register 17.

The register 17 comprises a latch circuit 17a and a decoder circuit 17b. The latch circuit 17a has its input terminals (only three of which are shown for clarity) coupled to the internal data bus line BUS through respective transfer gate MISFETs Q_1 to Q_3 and its output terminals coupled to the input terminals of the decoder circuit 17b. Again, for the sake of clarity, only three such connections are shown.

The control register 17 has stored therein the signal in the internal data bus line BUS by rendering the MISFET Q_3 conductive in response to the output signal of the address decoder 18.

The decoder circuit 17b decodes the signal of the latch circuit 17a thereby generating a signal for selecting that one of the transmission MISFETs Q_{16} to Q_{20} in the multiplexor 13 which corresponds to the signal received by the latch circuit 17a.

As a result, the selecting operations of the multiplexor 13 are executed such that the address signal instructing the register 17 is supplied from the register group 9 to the address decoder 18 and such that the multiplexor-selected data are supplied to the internal data bus line BUS.

The register 16 has its input terminals connected to the respective output terminals of the A/D converter 14 and its output terminals coupled to the internal data bus line BUS through respective transmission gate MISFETs Q_4 to Q_6 .

These transmission gate MISFETs Q_4 to Q_6 are rendered conductive when the address signal instructing the register 16 is supplied from the register group 9 of Figure 1 to the address decoder 18. As a result, the A/D conversion signals, which are supplied from the A/D converter 14 to the register 16, are further supplied to the internal data bus line BUS through the transmission gate MISFETs Q_4 to Q_6 .

The input/output port 12 for receiving and feeding the digital signal comprises input and output buffer amplifiers $12a$ and $12b$ which are coupled in a one-to-one relationship with respect to the terminals P_4 to P_7 , respectively.

The input buffer amplifier $12a$ comprises a high input impedance circuit such as an inverter having a MISFET so that it does not adversely affect the level of the signal fed from either the output buffer amplifier $12b$ or the external sensor.

The output buffer amplifier $12b$ comprises a tri-state circuit having a MISFET. The gate signal for controlling the operation of the output buffer amplifier $12b$ is supplied from a latch circuit $15c$ in the register 15.

If the output signal of the latch circuit $15c$ is at a high level, for example, the output buffer amplifier $12b$ is rendered operative in order that a digital signal at a high or low level is supplied from the output buffer amplifier $12b$ to the external terminal P_4 . If, on the contrary, the output signal of the latch

circuit 15c is at a low level, the output terminal of the output buffer amplifier 12b is rendered to have a high impedance state or a floating state.

The register 15 comprises a first latch circuit 15a, which is receptive to the output signal supplied from the input buffer amplifier 12a of the input/output port 12, a second latch circuit 15b, which is operative to feed the signal to the input terminal of the output buffer amplifier 12b, and a third latch circuit 15c (previously referred to) which is operative to feed the gate input signal to the output buffer amplifier 12b.

The output terminal of the latch circuit 15a, which corresponds to the external terminal P₄, the input terminal of the latch circuit 15b, and the input terminal of the latch circuit 15c are connected in common to a first bit line of the internal data bus line BUS through transmission gate MISFETs Q₇, Q₈ and Q₉, respectively.

Likewise, the input and output terminals of the latch circuit in the register 15, which correspond to the external terminal P₅, are connected in common to a second bit line through transmission MISFETs Q₁₀, Q₁₁ and Q₁₂, respectively, whereas the input and output terminals of the latch circuit in the register 15, which correspond to the external terminal P₇, are connected in common with a third bit line through transmission gates MISFETs Q₁₃, Q₁₄ and Q₁₅, respectively.

The transmission gates MISFETs Q₇ to Q₁₅ are supplied with the addresses, which are selected by the

address decoder 18.

The analog input converted into a digital signal, and the digital input are made common by the internal data bus line BUS. As a result, the reception of the input signals of the two kinds previously referred to is performed by making the address instructions of the registers 16 and 15 different from one another.

In the case where the common external terminal P_5 is used as the digital input terminal, as shown in Figure 1, the ROM 19 has written therein a program containing both the instruction of resetting the latch circuit in the register 15, which corresponds to the transmission gate MISFET Q_{12} , and the instruction of feeding the digital signal, which is fed to the external terminal P_5 , to the internal data bus line BUS through the transmission gate MISFET Q_{10} . In this case, the ROM 19 has neither the instruction of selecting the transmission gate MISFET Q_{11} nor the instruction of selecting the MISFET Q_{20} of the multiplexor 13, written therein.

Also, the ROM 19 has written therein both the instruction of resetting the latch circuit 15c of the register through the transmission MISFET Q_9 and the instruction of selecting the transmission gate Q_{19} of the multiplexor 13 but does not have written therein the instruction of selecting the transmission gates Q_7 and Q_8 .

The integrated circuit shown in Figure 1 is used to control the performance of an internal combustion engine.

Referring to Figure 1, a thermistor DET_1 for detecting the temperature of engine cooling water is connected between the external terminal P_1 of the microprocessor 1 and earth, and a load resistor R_1 is
5 connected between the thermistor DET_1 and a terminal of a voltage source V_B . If an element having a negative temperature coefficient is used as the thermistor DET_1 , the voltage applied to the external terminal P_1 decreases as the temperature of the engine cooling water rises.

10 In a similar manner, a thermistor DET_2 for detecting the temperature of the air intake into engine and a load resistor R_2 are connected to the external terminal P_2 .

A flow meter DET_3 to measure the flow of
15 intake air, is connected to the external terminal P_3 . The flow meter DET_3 comprises a resistance member and a sliding contact which can be moved with respect to the resistance member in accordance with the rate of flow of intake air. As a result, the intake air flow meter
20 supplies the external terminal P_3 with a voltage whose magnitude is proportional to the rate of flow of intake air.

A tachometer DET_4 of the internal combustion engine, is connected to the external terminal P_4 . The
25 tachometer DET_4 supplies the terminal P_4 with a voltage which is proportional to the engine R.P.M.

A starter switch SW of the engine is connected to the external terminal P_5 .

A crank angle sensor DET₅ associated with the engine, is connected to the external terminal P₆. The sensor DET₅ is constructed to generate pulse signals at a high level when the crank-shaft is at a predetermined angular position, e.g., 0 degrees.

On the other hand, the external terminal P₇ is used as an output terminal for giving a warning of an excessive engine temperature, for example. A lamp PL is connected to a buffer circuit 30 which receives the output of the terminal P₇ so that it is lit when the engine temperature reaches an abnormal level.

An interface circuit 21 is fed with the control signal from the grouped external terminals CONT of the microprocessor 1, the address signal from an address bus AD and the data from the data bus DT. The interface circuit 21 has a plurality of output lines Z₁ to Z₄ and contains therein (not shown) a number of memory circuits which are respectively selected by the address signals of the address bus AD and which have their states determined by the data signals of the data bus DT.

The signal on the output line Z₁ of the interface circuit 21 is supplied through an output buffer circuit 22 to an ignition coil 26, whereas the signal on the output line Z₂ is supplied through an output buffer circuit 23 to a solenoid 27 for adjusting the throttle valve in the inlet manifold of the engine. On the other hand, the signal on the output line Z₃ is supplied through

an output buffer circuit 24 to an electromagnetic type fuel pump 28, whereas the signal on the output line Z_4 is supplied to a relay 29 for energizing the starter motor of the engine.

5 In order to control the engine, the ROM 19 has stored therein not only the program but also the various interpolation data which are determined by the characteristics of the engine to be controlled.

10 For example, the angle of ignition advance for the spark is determined not only by the engine R.P.M. but also by other engine characteristics. Therefore, the ignition timing data for the engine R.P.M. have to be stored in advance in the ROM 19. In this instance, the data of the engine characteristics for the ignition
15 timing data are not stored in the ROM in a manner to correspond all the engine R.P.M.s over the entire range, but only a selected number are stored from which the intermediate values can be interpolated. As a
consequence the capacity of the ROM can be reduced.

20 Likewise, the solenoid for controlling the throttle valve is controlled in accordance with the temperature of the intake air, the engine temperature, the engine R.P.M. and other engine characteristics. The data of these engine characteristics for controlling
25 the solenoid are stored as interpolation data in the ROM.

 The various engine control data when the engine is practically at its operating condition are prepared by the arithmetic operations of the microprocessor 1,

which is made responsive to the data fed from the various sensors and the various interpolation data stored in advance in the ROM 19.

Referring to Figure 1, when an ignition switch S_0 is turned on, power is supplied from a battery B to a constant voltage circuit 40 so that the voltage V_B is fed from the constant voltage circuit 40 to the respective circuits referred to above.

The analog data such as the temperature of the engine cooling water or the temperature of the intake air, which are generated by the thermistors DET_1 and DET_2 when the microprocessor 1 becomes operative, are converted in a time-division manner into digital data by the action of the analog to digital converter 14. The respective digital data thus converted are stored in the random access memory (RAM) 20 by means of the data bus.

The fuel pump 28 is rendered operative by the output from the interface circuit 21.

When the starter switch SW is actuated, the relay 29 is energized so that the starter motor cranks the engine.

In order to reduce the capacity of the ROM 19, the data stored therein concerning the ignition timing, for example, are made to correspond only to certain predetermined sample R.P.M.s.

As a result, the data relating to the ignition timing from the tachometer DET_4 for any engine R.P.M. can be obtained by an arithmetic operation, in

which the interpolation data in the ROM 19 for the sampled R.P.M. near any of the stored engine R.P.M.s are connected.

Thus, the practical ignition timing is
5 calculated from the standard ignition timing based upon the output of the crank angle sensor DET₅ and from the ignition timing data determined by the above referred to arithmetic operations. In accordance with the ignition timing thus calculated, the current in the primary winding
10 of the ignition coil 26 is switched off so as to produce a high voltage in the secondary winding for the spark.

The interpolation data of the ROM 19 for controlling the throttle valve in accordance with the R.P.M. data of the engine, the temperature data of the
15 engine cooling water and the air intake temperature data are referred so that the pulse control signals for controlling the throttle valve are generated. By these pulse control signals, the duty ratio of the pulse current of the solenoid 27 to be coupled through the interface
20 circuit 21 is changed. The solenoid 27 has its mean current changed by the duty ratio of the pulse current so that the position of the throttle valve is controlled in accordance with the duty ratio.

The various process controls of different
25 requirements, in other words, the various process controls having different numbers of analog signal inputs and digital signal inputs and outputs are made possible by a reduced number of terminals so that the general

usability of the various process controls of the microprocessor for controlling the internal combustion engine can be improved. Moreover, process controls of high quality, i.e., of high density are also made possible merely by changing a portion of the program even for the change in the system from the digital input to the analog input.

The present invention is not limited to the embodiment described above but can be so modified that the port is constructed of such input and output ports as are independent of each other. In this modification, the common use of the terminals is made between the input port and the analog input.

Even in the case of using the terminals in common, various modifications can be made such that all of the analog inputs are made common or such that all the digital inputs are made common.

Moreover, the construction of the microprocessor can be modified in various manners.

Furthermore, the system for effecting the various process controls is constructed of a digital semiconductor integrated circuit consisting of several chips, comprising a microprocessor, a ROM in which a control program is stored, and a RAM for storing various data.

Therefore, the analog to digital input/output circuit containing the A/D converter may be provided, for example, as shown in Figure 3, in the digital semiconductor integrated circuit 19 comprising the ROM in which the

control program is stored. As shown in Figure 3, the digital semiconductor integrated circuit 19, comprises an address decoder 20 and a memory array 21 in which the program instruction is stored, as well as the input/output port 12, the register 15, the multiplexor 13, the A/D converter 14 and the registers 16 and 17. With this construction, similar operations can be effected by connecting the data and address buses of the digital semiconductor integrated circuit 19 and the micro-processor through the external data and address buses.

Moreover, in the digital control system containing the RAM, the analog to digital input/output circuit containing the A/D converter may be provided in the digital semiconductor integrated circuit comprising the RAM, and the whole system of the microprocessor, ROM and RAM may be similarly constructed of a one-chip digital semiconductor integrated circuit.



CLAIMS:

1. A digital semiconductor monolithic integrated circuit including:

a plurality of external terminals;

a digital signal input circuit;

5 an analog signal input circuit responsive to an analog input signal for supplying a digital signal corresponding to said analog input signal; and

10 at least one common terminal for connecting input terminals of said digital signal input circuit and said analog signal input circuit with at least one of said plurality of external terminals.

2. A digital semiconductor monolithic integrated circuit according to claim 1, further including:

15 an internal bus line;

a switch element for connecting the output terminal of said digital signal input circuit to said internal bus line; and

20 a switch element for connecting the output terminal of said analog signal input circuit to said internal bus line.

3. A digital semiconductor monolithic integrated circuit according to Claim 2, wherein said analog signal input circuit includes:



a plurality of input terminals connected to said external terminals, respectively;

an analog multiplexor for selecting one of the analog input signals to be fed to said plurality of input terminals; and

an analog to digital converter which is supplied with the output signal of said analog multiplexor.

4. A digital semiconductor monolithic integrated circuit including:

a plurality of external terminals;
a digital signal input/output circuit;
an analog signal input circuit responsive to an analog input signal for supplying a digital signal corresponding to said analog input signal; and

at least one common terminal for connecting the input/output terminals of said digital signal input/output circuit and the input terminal of said analog signal input circuit with at least one of said plurality of external terminals.

5. A digital semiconductor monolithic integrated circuit according to claim 4, wherein said digital signal input/output circuit includes;

a digital signal input circuit having its input terminal connected to a first of said input/output terminals; and



a digital signal output circuit having its output terminal connected with a second of said input/output terminals and having its output impedance capable of being raised to a high impedance by a control signal.

6. - A digital semiconductor monolithic integrated circuit according to claim 5, further comprising:

an internal bus line;

a switch element for connecting the output terminal of said digital signal input circuit to said internal bus line;

a switch element for coupling the input terminal of said digital signal output circuit to said internal bus line; and

a switch element for connecting the output terminal of said analog signal input circuit to said internal bus line.

7. A digital semiconductor monolithic integrated circuit according to claim 6, further including:

a latch circuit for storing said control signal to be supplied to said digital signal output circuit; and

a switch element for connecting said internal bus line to the input terminal of said latch circuit.



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8. A digital semiconductor monolithic integrated circuit according to any one of the preceding claims, in combination with a digital control system, said control system including:

5 a controllable device having its operation controlled by digital control signals;

analog and digital sensors for detecting the operation of said controllable device; and

10 a control circuit device responsive to both the analog signal fed out of said analog sensor and the digital signal fed out of said digital sensor for generating said digital control signals.

9. An internal combustion engine including the combination of the digital semiconductor monolithic integrated circuit and digital controlled system according to claim 8, wherein the ignition timing is controlled with the aid of sensors which detect certain engine parameters.

10. A digital integrated monolithic semiconductor circuit constructed substantially as herein described with reference to and as illustrated in Figures 1 and 2 or Figures 1 and 2 as modified by Figure 3 of the accompanying drawings.

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