

MEMORY WITH COLUMN REDUNDANCY AND LOCALIZED COLUMN REDUNDANCY CONTROL SIGNALS

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Abstract of the Disclosure

A memory (20) has a plurality of columns of memory cells and has a plurality of redundant columns of memory cells. A comparator (45) detects an access to a defective column. A
10 redundant write generator (31) and write fuses (32) are provided for each write portion (30A, 30B, 30C, and 30D) to replace the defective column with a redundant column by replacing a write global data line (37) with a redundant write global data line (39). Redundant read generators (60 and 61) and read fuses (59) are
15 provided for each read portion (50A, 50B, 50C, and 50D) to replace a defective column by deselecting a read global data line (29) and replacing it with a redundant read global data line (44). The fuses and redundant generators are located close to their global data lines, thus reducing the routing of control signals and
20 improving the access time of redundant columns.

(FIG. 1 accompanies this abstract)