PATENT SPECIFICATION

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(19)



(54) TRANSISTOR STRUCTURES AND THE MANUFACTURE THEREOF

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 464 Ellis Street, Mountain View, California 94042, United States of America, a corporation organised and existing under the Laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to transistor structures and the manufacture thereof.

MOS (metal-oxide-semiconductor) transistors are well known. Such transistors are extremely sensitive to small amounts of contamination at the interface between insulation layers and the underlying semiconductor material containing the source and drain regions. As the size of MOS transistors has decreased, proper alignment of masks and particularly the source and drain masks, has become more important. The use of a self-aligned gate of polycrystalline silicon as disclosed in U.S. Patent 3,673,471 makes possible the reduction in size of the source and drain regions, reduces the overlap of the gate with respect to the source and drain regions and thus makes possible higher speed performance of MOS transistors.

In an MOS transistor, a thin insulating layer is placed between the semiconductor substrate containing the source and drain regions and the gate electrode. To prevent unwanted inversions of the semiconductor material in the field (i.e. the non-active portion) of the device when a voltage is applied to the gate electrode, a much thicker insulating layer is placed over the field of the device than under the gate electrode. As disclosed in the above-mentioned U.S. Patent 3,673,471, typically the field insulation is an order of magnitude thicker than the gate insulation. To make an MOS transistor by the prior art methods, the field oxide is first formed on the wafer. Those portions of the field oxide over the regions of the semiconductor substrate in which sources and drains are to be formed are then removed. After formation of the source and drain regions, the field oxide over the gate region is removed and the gate oxide is formed. The gate oxide typically has a thickness of the order of 1,000 angstroms.

The removal of the field oxide over the active regions of the semiconductor substrate allows these regions of the substrate to become contaminated and makes difficult the further processing of the device to grow a uniform thickness gate oxide. Typically, contaminants gather on the edges of the field oxide and result in short circuits forming between a subsequently formed gate electrode and the source and/or drain regions. In addition, the different thicknesses of the field and gate oxides cause an abrupt step in the insulation adjacent the source and drain regions. Such a step greatly increases the risk of open circuits in the conductive leads contacting the source and drain regions.

This invention provides a transistor structure comprising semiconductor material containing a source region and a drain region, a layer of gate insulation overlying the surface of the semiconductor material between the source and drain regions, a layer of field insulation overlying the semiconductor material surrounding the source and drain regions and the region between the source and drain regions, insulation bridging the field insulation to the gate insulation and gradually tapering from the thickness of the field insulation layer to the thickness of said gate insulation, a gate electrode formed over the gate insulation between the source and drain regions,

passivation material covering the top surfaces of the source and drain regions, the gate electrode and the field insulation, and contact leads contacting the source and drain regions and the gate electrode.

This invention also provides a method of manufacturing a transistor structure, the method comprising the steps of forming source and drain regions in semiconductor material, forming a gate electrode between the source and drain regions, the gate electrode being separated from the semiconductor material between the source and drain regions by a layer of gate insulation, forming a thick field insulation layer over the fields of the transistor and forming conductive contacts to the source and drain regions and the gate electrode, the gate insulation being formed before the formation of the field insulation so that insulation bridging the field insulation to the gate insulation tapers in thickness gradually from that of the field insulation to that of the gate insulation adjacent the source and drain regions and the gate electrode of the transistor structure.

The invention will be more readily understood from the following illustrative description and accompanying drawings, in which:

Figs. 1*a* to 1*h* are partial sectional schematic side views showing stages in the manufacture of an MOS transistor in accordance with the invention; and

Fig. 2 is a similar view on a larger scale of part of the transistor of Figs. 1*a* to 1*h*.

This invention will be described using silicon semiconductor material. However, it should be understood that this invention can be used with any other semiconductor material suitable for use in forming MOS transistors and capable of having an oxide of the semiconductor material thermally grown from the semiconductor material.

A silicon substrate 11 (Fig. 1*a*) has formed on it a gate oxide 12. Typically, gate oxide 12 is formed by thermal oxidation of substrate 11 and is approximately 1,000 angstroms thick. It should be understood, however, that any thickness gate oxide suitable for yielding an MOS transistor with desired characteristics can be used with the process of this invention. Silicon substrate 11 typically is of four to six ohm-cm resistivity and typically is cut in the {111} orientation although other orientations such as the {100} orientation can also be used. While oxide layer 12 is preferably formed by thermal oxidation of silicon substrate 11, this oxide layer could also be formed by other techniques capable of forming a satisfactory gate insulation.

Hereafter substrate 11 and any attached overlying layers will be called wafer 10.

A layer 13 of silicon nitride is formed over oxide layer 12 (Fig. 1*b*). Nitride layer 13 typically is 1,000 angstroms thick although again, other thicknesses of nitride can be used, as required.

A thin layer 13*a* of oxide (Fig. 1*b*) is next formed from the top surface of nitride layer 13. Techniques for the oxidation of a nitride layer are well known and are described, for example, in a paper by Appels et al entitled "Local Oxidation of Silicon and Its Application in Semiconductor-Device Technology" published in Philips Research Reports 25, 118—132, 1970. Typically, layer 13*a* is 50 angstroms or so thick. It should be noted that this step is optional and can be omitted if desired.

Next layer 14 of silicon dioxide is formed over the thin oxidized nitride layer. In one embodiment silicon dioxide layer 14 is about 6,000 angstroms thick and is formed from the decomposition of silane in an oxygen environment. Silicon dioxide layer 14 adheres well to the oxidized nitride layer 13*a*; in fact layer 13*a* was formed to provide an adherent base for layer 14.

The next step in the process is not illustrated in the drawings but comprises a bulk gettering at typically 1,070°C in a phosphorus oxychloride environment. The resulting phosphorus-rich glass comprising the top portion of layer 14 is removed from the semiconductor device. In one embodiment 3,000 angstroms of layer 14 are removed.

As shown in Fig. 1*c*, dioxide layer 14 and underlying nitride layer 13 are removed from all portions of the field of the semiconductor device. To do this, oxide layer 14 is first masked to leave exposed all oxide in the field of the device. Layer 14 is then etched down to nitride layer 13 using a preferential etch which etches silicon dioxide at a much faster rate than silicon nitride. Then when all the exposed oxide 14 over nitride 13 has been removed, the newly-exposed silicon nitride 13 is removed by an etch which etches nitride at a much faster rate than it does silicon dioxide. Accordingly, when the silicon nitride 13 overlying the gate oxide 12 has been removed, the etch used to remove the silicon nitride does not attack gate oxide 12 to any great extent. The resulting etched structure is shown in Fig. 1*c* wherein portion 14*b* of silicon dioxide layer 14 remains overlying region 13*b* of silicon nitride layer 13 which in turn overlies the active region of the device.

At this point, the field region of the silicon device, that is, the region of the semiconductor device within which will not be formed source, drain and gate regions of MOS transistors, is implanted with a selected impurity by use of ion implantation techniques. Ion implantation

allows the conductivity-type determining impurities to be passed through gate oxide 12 and placed in a region of the semiconductor substrate 11 directly beneath this gate oxide. Thus, regions 11*a* and 11*b* shown in Fig. 1*c* contain ion implanted impurities. When the semiconductor substrate is N-type, these impurities are formed to a concentration such that the implanted semiconductor material has N+ type conductivity. When the silicon substrate is of P type conductivity, the impurities are formed such that the ion implanted regions have a P+ type conductivity. Typical thickness for the ion implanted regions 11*a* and 11*b* is 1,000 angstroms and a typical impurity concentration in these regions is 10^{16} atoms per cc.

Next, wafer 10 is placed in an oxidizing environment at an elevated temperature. The oxygen in the environment combines with the silicon from silicon substrate 11 beneath those portions of the gate oxide 12 not covered by nitride 13*b* to form thick regions 16*a* and 16*b* (Fig. 1*d*) of oxidized semiconductor material. Regions 16*a* and 16*b* are typically about 1.6 microns thick. Oxidation of silicon semiconductor material results in a thickness increase of the material by a factor of about 2.2. Accordingly, regions 16*a* and 16*b* consume approximately 0.7 micron of underlying semiconductor material 11 to form silicon dioxide layers 1.6 microns thick. During the high temperature thermal oxidation process, regions 11*a* and 11*b* of N+ type conductivity migrate further into silicon semiconductor substrate 11. This migration occurs both because of the different diffusivities and segregation coefficients of the conductivity-determining impurities in regions 11*a* and 11*b* in silicon as opposed to silicon dioxide and the prolonged high temperature. Accordingly, the oxidized regions 16*a* and 16*b* do not contain a significant amount of the impurity in regions 11*a* and 11*b*. If, however, substrate 11 contains boron as a predominant impurity and this is P type, regions 16*a* and 16*b* may contain significant amounts of boron. Also, region 16*e* of silicon dioxide is formed on the backside of the wafer during the oxidation process. Region 16*f* (Fig. 12*d*) was formed earlier during formation of gate oxide 12 and oxide layer 14.

The formation of thick field oxide 16*a* and 16*b* is followed by the removal of nitride 13*b* and overlying silicon dioxide 14*b* (Fig. 1*c*). The resulting structure is shown in Fig. 1*d*. Note that in regions 16*c* and 16*d* of the field oxide, the oxide tapers gradually from the thickness of the field oxide 16*a*, 16*b* to the thickness of the gate oxide 12. This taper makes possible the subsequent contacting of source and drain regions by leads crossing the field oxide and then dropping gradually to the elevation of the gate oxide without the high probability of open circuits at steps in the oxide so prevalent in prior art transistors.

Following the formation of the structure shown in Fig. 1*d*, a layer 17 (Fig. 1*e*) of polycrystalline silicon is formed over the top surface of the device. Layer 17 is typically formed after opening 12*b* is formed in gate oxide 12. Thus part of layer 17 contacts the surface of substrate 11. Polycrystalline silicon layer 17 typically is approximately 3,000 to 3,300 angstroms thick. However, other thicknesses can be used for this layer if desired. Techniques for the deposition of polycrystalline silicon suitable for use with this invention are well known and thus will not be described in detail.

The top surface of polycrystalline silicon layer 17 is next oxidized to form a silicon dioxide layer. Standard photoengraving techniques are used to mask the oxidized polycrystalline silicon layer 17 above the gate regions to be formed in or on substrate 11 and above the conductive interconnections to be formed from polycrystalline silicon. The oxide is removed in those areas not protected by photoresist. The exposed polycrystalline silicon is then removed.

The resulting structure (Fig. 1*f*) has polycrystalline silicon region 17*a* formed on its top surface over gate oxide 12 and protected by overlying oxide layer 18*a*. The polycrystalline silicon in regions 17*b* and 17*c* has been removed. Polycrystalline silicon 17*d*, containing on its top surface an oxide layer 18*d*, overlies not only part of the active region of the device, but also part of the field of the device. After being doped, this polycrystalline silicon will serve as a conductive lead to the active region to be formed in substrate 11 beneath opening 12*b* in gate oxide 12. In addition, regions of doped polycrystalline silicon can be used as conductive crossunders beneath metal leads.

Next, the gate oxide 12 not covered by polycrystalline silicon regions 17*a*, 17*d* and not part of field oxide regions 16*a*, 16*b* is removed to expose the top surface of the regions of semiconductor material 11 in which are to be formed the source and drain regions of an MOS transistor. Simultaneously with the selective removal of gate oxide 12, the oxidized portions 18*a*, 18*d* of polycrystalline silicon regions 17*a*, 17*d* are also removed.

An impurity, typically boron when substrate 11 is of N type conductivity, is next diffused into substrate 11 to form the source and drain regions 19*a*, 19*b* of an MOS transistor. While the gate oxide above the source and drain regions 19*a*, 19*b* has

been described as being completely removed during this process step, this gate oxide can be only partially removed, if desired. That portion of gate oxide 12 left on substrate 11 during the diffusion process must, however, be thin enough to allow the passage of the impurity through it to form the source and drain regions 19*a*, 19*b* beneath gate oxide 12.

During diffusion of boron into substrate 11 to form source and drain regions 19*a*, 19*b*, boron also diffuses into regions 17*a* and 17*d* of polycrystalline silicon 17 to form gate electrode 17*a* and conductive lead 17*d*.

If the diffusion is carried out in an oxidizing atmosphere, a thin oxide layer will reform over the source and drain regions. Part of this oxide layer can be removed to allow electrical contact to be made to drain region 19*b*. Note that region 19*a* has already been contacted through window 12*b* (Fig. 1*e*) by polycrystalline silicon 17*d*. Alternatively, a metal contact of a material such as aluminum can be made to region 19*a*.

After the formation of the doped gate electrode 17*a*, the doped conductive lead 17*d*, and the source and drain regions 19*a*, 19*b* by diffusion of a P type impurity, a layer of passivating material 20 (Fig. 1*g*) is formed over the top surface of the device. Typically, layer 20 consists of a phosphorus-doped silicon dioxide layer formed to a thickness of about 6,000 angstroms. However, other insulating and/or passivating layers can also be formed over the top surface of the device, if desired. These layers, can, if desired, comprise multiple layers of material and can include layers of silicon nitride, for example.

Wafer 10 is now heated to allow glass 20 to flow and to continue the diffusion of the boron in regions 19*a*, 19*b* into substrate 11 to further expand the source and drain region 19*a*, 19*b*. This heat treatment is well known in the semiconductor art and thus will not be described in detail.

Upon completion of the above-described heat treatment, contact openings are formed in layer 20 to expose the regions in substrate 11 to which electrical contact is to be made. While region 19*a* already is contacted by doped polycrystalline silicon lead 17*d*, electrical contact must be made to region 19*b*. Contact window 20*a* in layer 20 to expose the surface of region 19*b* is formed using well-known photolithographic and masking techniques. In addition, contact is also made to the doped polycrystalline silicon remaining on the device through other windows in layer 20, to form a gate electrode.

At this point, oxide layers 16*e* and 16*f* on the backside of the wafer (see Fig. 1*d*) are removed by, for example, etching.

A layer 21 of conductive material is now formed over the top surface of layer 20. Typically this layer is formed of evaporated aluminum. Layer 21 contacts the top surfaces of regions in substrate 11 through windows such as window 20*a* through layer 20. Conductive layer 21, which in one embodiment comprised a 1.2 micron thick aluminum layer, is next masked and etched to define the conductive lead pattern on the top surface of the device. This masking and etching step is well known and thus will not be described here.

Wafer 10 is next alloyed to form good electrical contacts between portions of layer 21 and substrate 11.

The final step comprises forming a layer of phosphorus doped silicon dioxide over the wafer surface to an approximate thickness of 1.0 micron. This step is followed by masking the contact pads on the top surface of the device to be formed from layer 21 and etching away the silicon dioxide to expose these contact pads and the scribe regions between dice.

The device formed by the above process has a buried contact 17*d* to region 19*a*. In addition, the surface of substrate 11 on which the transistors are formed has at all times been protected by gate oxide 12 thereby preventing impurities from reaching the interface between oxide 12 and substrate 11. While additional oxide 16*a*, 16*b* in the field of the device is formed during the process, this field oxide is an extension of the gate oxide. The interface between the gate oxide 12 and field oxide 16 is tapered thereby reducing the severity of the steps which must be traversed by conductive leads such as leads 17*d* and 21 which contact the source and drain regions of the underlying semiconductor device. In addition, the severity of the step traversed by the contact to gate 17*a* is likewise reduced by this tapered surface.

Fig. 2 shows in more detail the transition region between gate oxide 12 and field oxide 16*b* with polycrystalline silicon 17 overlying both oxides, as shown in Fig. 1*e*. The structure shown in Fig. 2 is based on an actual photograph of the transition region between gate oxide 12 and field oxide 16*b*. As shown in Fig. 2, field oxide 16*b* is a gradual extension of gate oxide 12 increasing gradually in thickness over region 12*b*. At peak 12*c*, the gradual increase in thickness of the oxide abruptly terminates and the slope of the surface of oxide 16*b* reverses. A trough 16*g* forms on the surface of oxide 16*b* but then in region 16*h* the field oxide gradually acquires a flat surface and becomes uniform in thickness. Region 11*b* of highly doped N type material remains just under the lower surface of the field oxide 16*b*. Polycrystalline silicon 17 forms a

substantially uniform layer over the top surface of gate oxide 12 and field oxide 16 despite the presence of peak 12*c* and trough 16*g* in the gate and field oxides 12 and 16*b*. A silicon dioxide layer 20 overlies polycrystalline layer 17.

A second embodiment of this invention varies several of the process steps. In this second embodiment, substrate 11 is oxidized to form gate oxide 12. Next a nitride layer 13 (Fig. 1*b*) is deposited over gate oxide 12 to a thickness of about 1,000 angstroms. Oxide (not shown in the figures) formed on the backside of wafer 11 is then removed, typically by an etch. This oxide was formed simultaneously with the gate oxide and is the same thickness of the gate oxide (typically about 1,000 angstroms). Next a layer 14 (Fig. 1*b*) of silicon dioxide is deposited over the top surface of nitride 13. Prior to the deposition of layer 14, nitride layer 13 can be oxidized, if desired, to provide an improved base on which layer 14 can be formed. Layer 14 is typically 5,000 angstroms.

The structure is now bulk gettered with a phosphorus trichloride compound at a high temperature, typically around 1,070°C for a selected time. After the gettering is completed, layer 14 is stripped from the device. Nitride layer 13 is now oxidized, typically in steam at 1,000°C, for a time selected to form an oxide to a thickness of about 50 angstroms. The 50 angstrom thick oxide overlying the nitride is then removed throughout the field of the device, leaving oxide over the source, drain and gate regions of the nitride. The nitride exposed by removal of the oxide throughout the field of the device is then removed with phosphoric acid etch at 155°C. Following this step, the exposed gate oxide (a thickness of about 1,050 angstroms) is removed. This allows observation of the unetched or partially etched areas of the field oxide resulting from incomplete nitride removal. Thus regions of nitride inadvertently left in the field of the device are readily discernible at this point in the process and can be readily removed.

Next, impurities are implanted in the field of the device using ion implantation techniques. Typically these impurities are implanted to a surface density of 2×10^{12} atoms per square centimeter using a 40KEV ion beam.

After the ions are implanted throughout the field of device, the field is reoxidized in 1,000°C steam to grow an oxide layer of about 1.3 microns. The oxide on the silicon nitride over the source, drain and gate regions to be formed in or on the underlying substrate 11 initially was 50 angstroms thick. After the field oxidation, this oxide is about 250 angstroms thick. This 250 angstrom thick oxide on the nitride is stripped by etching. The etching continues longer than necessary to remove the 250 angstroms of oxide over the nitride and typically an extra amount of oxide (for example up to 750 angstroms) is removed over the device to insure complete removal of all oxide on the nitride. Finally, the nitride overlying the gate oxide is removed by an etching process leaving the underlying gate oxide (1,050 angstroms) on the surface of substrate 11 overlying the source, drain and gate regions to be formed in or on this substrate. The remainder of the process is as described above in conjunction with the first embodiment of this invention.

A feature of this second embodiment is that the source and drain masking dimensions are controlled by the etching of a thin masking oxide (typically about 50 angstroms thick) rather than by masking and etching a silicon dioxide layer of 6,000 angstroms thickness. A thick silicon dioxide layer can cause variations in the sizes of the source, drain and gate regions due to uncontrollable variations in the lateral etch rates of the thick silicon dioxide layer (see layer 14, Fig. 1*b*). The use of a 50 angstrom thick oxide layer to define the lateral extent of the source, drain and gate regions significantly improves the accuracy with which these regions can be formed due to the decrease in sensitivity of the process to the etch characteristics of silicon dioxide and due to reduction of optical effects such as diffraction and light scattering during the formation of the source and drain openings in the underlying nitride layer 13 and gate oxide layer 12.

In addition, the ion implantation energy required to implant selected impurities in the field of the device is significantly reduced by removal of the initial oxide in the field region. Thus in one embodiment, the phosphorus implant energy was reduced from 120KEV to 40KEV. Alternatively, a chemical deposition can be used to dope the field of the semiconductor device if desired.

Finally, the field oxide thickness can be reduced to about 1.3 microns from the previously required thicker field oxide. This reduces the time required to form the field oxide and thus increases the efficiency of production.

A variation of the above process involves initially forming over all the top surface of substrate 11 only a portion of the gate oxide 12 (Fig. 1*a*). Nitride layer 13 is then formed as before and the backside oxide is removed. Silicon dioxide layer 14 is deposited, gettered and stripped. The nitride layer 13 is then removed over the field of the device typically by etching to expose the underlying gate oxide. The gate

oxide initially was formed thinner than in the above two embodiments, for example, to a thickness of about 500 to 1,000 angstroms. The removal of the nitride exposes this initial gate oxide in the field of the device. Then, this exposed gate oxide is selectively removed in the field regions. The selected impurity is implanted throughout the field of the device in the same manner as in the second embodiment of this invention and the field of the device is then reoxidized at a temperature of about 1,000°C to a desired thickness. This thickness is typically 1.3 microns. The oxide on the remaining parts of nitride layer 13 (over the source and drain regions) is now stripped. This oxide has a thickness of about 250 angstroms as a result of the long field oxidation to which the device has previously been subjected. In removing this oxide, the etch process is continued to overetch this oxide by about the equivalent of 750 angstroms. This insures that all the oxide above nitride layer 13 is completely removed but has little effect on the field oxide. Next the nitride layer 13 overlying the source, drain and gate regions to be formed in the device is removed. The gate is then reoxidized to form an additional 250 to 750 angstroms of oxide over the source, drain and gate regions as desired. If desired, this reoxidation and the initial oxidation are both carried out in a gettering environment. Typically a halogen gettering is used during the oxidation. This is necessary because the nitride deposition can contaminate the oxide.

Note that in the last described embodiment of this invention, the gate oxide again remains over the device after it is initially formed. However, any oxide or nitride layers over the field of the device are removed to allow the placing of an impurity in the field of the device to prevent channeling. Then the field oxide is reformed to the desired thickness over the device. However, that part of the gate oxide covering the source, drain and gate regions is left on the device throughout all of this processing thereby preventing contaminants from forming in the gate or source and drain regions.

The gettering of the oxide after the deposition of nitride layer 13 protects the device from any sodium and other metallic contamination which might have occurred prior to this gettering. Again, the removal of the nitride and the underlying oxidation provides a visual check to insure complete nitride removal. Incomplete nitride removal on the device can cause buried contact problems and certain surface problems.

The additional oxidation of the gate dielectric after the field oxidation and nitride removal eliminates certain high Q_{ss} edge effects characteristic of particularly small MOS transistors.

The increase in the gate oxide thickness to about 1,200 angstroms increases the threshold voltage a slight amount (typically from about 1.3 volts to about 1.5 volts).

The growth of gate oxide layer 12 on substrate 11 before subsequent processing followed by selective oxidation of the field regions offers significant processing advantages. It permits optimized surface preparation of the starting wafer independent of other processing steps required. It virtually eliminates bulk N type impurity "pile-up" subsequent to gate oxidation; almost complete redistribution of any impurity "pile-up" occurring during the initial oxidation step occurs during the subsequent processing. By growth of the field oxide "through" the gate oxide, it avoids any discontinuities due to the non-uniform oxidation rates that occur in prior art processing as a result of growing the gate oxide after the thicker field oxide. It also provides smooth transitions from the field to the gate oxide and thus allows thin metal or resistor films to be smoothly covered and accurately formed.

An alternative embodiment of this invention can be used to manufacture depletion-mode MOS transistors. This process uses basically the previously described process steps with, however, the following modification. After the field of the device is oxidized, the silicon dioxide layer 14*b* and silicon nitride layer 13*b*, together with intermediate oxide layer 13*a* are removed from the surface of the device leaving exposed the gate insulation over the source, drain and gate regions. Then window 12*b* is made through the gate oxide to a selected region in underlying silicon substrate 11. The wafer is then covered with a layer of photoresist and the photoresist above selected source, drain and gate regions is removed by well known photolithographic masking techniques. This is followed by ion implantation of a selected P type impurity such as boron over the top surface of the source, drain and gate regions. This implantation occurs to a thickness of about 1,000 angstroms in a typical embodiment although other thicknesses can also be used if desired and appropriate for the intended purposes. The ion implantation typically takes place at a 50KEV energy level. The result of this ion implantation is to create a thin layer of opposite conductivity type to the predominant conductivity of substrate 11 in and near the top surface of semiconductor material 11. This layer will serve as a channel between to-be-formed source and drain regions with the same conductivity

type in the substrate 11. Thus this ion implanted layer makes possible the formation of a depletion-mode MOS transistor rather than the previously described enhancement-mode MOS transistor. Further processing continues as before.

WHAT WE CLAIM IS:—

1. A transistor structure comprising semiconductor material containing a source region and a drain region,

a layer of gate insulation overlying the surface of the semiconductor material between the source and drain regions,

a layer of field insulation overlying the semiconductor material surrounding the source and drain regions and the region between the source and drain regions,

insulation bridging the field insulation to the gate insulation and gradually tapering from the thickness of the field insulation layer to the thickness of said gate insulation,

a gate electrode formed over the gate insulation between the source and drain regions,

passivation material covering the top surfaces of the source and drain regions, the gate electrode and the field insulation, and

contact leads contacting the source and drain regions and the gate electrode.

2. A transistor structure as claimed in claim 1 in which the insulation bridging the gate and field insulation comprises a first section extending from the gate insulation toward the field insulation and a second section extending from the first section to the field insulation, the first section having a thickness which increases gradually from the thickness of the gate insulation to a peak, the top surface of the first section rising gradually to the peak, and the first section ending at the peak, the second section beginning at the peak and having a thickness equal to that of the first section beneath the peak and which remains approximately constant for a selected distance and then gradually increases to the position at which the second section joins the field insulation, the second section having a top surface which in the region adjacent the peak has a slope opposite in sign to that of the top surface of the first section, and the top surface of the second section forming a trough between the peak and the field insulation.

3. A transistor structure as claimed in claim 1 or 2 in which the gate insulation overlies parts of the source drain regions.

4. A transistor structure as claimed in claim 1, 2 or 3 in which the insulation bridging the gate and field insulation overlies the peripheries of the source and drain regions and field regions directly adjacent the source and drain regions.

5. A transistor structure as claimed in claim 1, 2, 3 or 4 in which at least one of the gate insulation and the field insulation is of substantially uniform thickness.

6. A transistor structure as claimed in any preceding claim in which the insulation comprises an oxide of the semiconductor material.

7. A transistor structure as claimed in any preceding claim in which the semiconductor material comprises silicon.

8. A transistor structure as claimed in any preceding claim in which the gate electrode comprises selectively doped polycrystalline silicon.

9. A transistor structure as claimed in any preceding claim in which the gate insulation has a thickness in the range of 500 to 1,000 angstroms.

10. A transistor structure substantially as herein described with reference to Figs. 1*h* and 2 of the accompanying drawings.

11. A method of manufacturing a transistor structure, the method comprising the steps of forming source and drain regions in semiconductor material, forming a gate electrode between the source and drain regions, the gate electrode being separated from the semiconductor material between the source and drain regions by a layer of gate insulation, forming a thick field insulation layer over the field of the transistor and forming conductive contacts to the source and drain regions and the gate electrode, the gate insulation being formed before the formation of the field insulation so that insulation bridging the field insulation to the gate insulation tapers in thickness gradually from that of the field insulation to that of the gate insulation adjacent the source and drain regions and the gate electrode of the transistor structure.

12. A method as claimed in claim 11 having the steps of forming a first layer of oxide of semiconductor material to constitute the gate insulation over a substrate of the semiconductor material,

forming a layer of silicon nitride over the oxide layer.

forming a relatively thick second layer of silicon dioxide over the layer of silicon nitride,

removing those portions of the second layer of silicon dioxide and the layer of silicon nitride over those regions of the semiconductor material in which the source, drain and gate regions will not be formed,

growing additional oxide of the semiconductor material on those portions from which the second layer of silicon dioxide and the layer of silicon nitride have been removed to constitute the field insulation, the additional oxide being grown through the first layer, and

type in the substrate 11. Thus this ion implanted layer makes possible the formation of a depletion-mode MOS transistor rather than the previously described enhancement-mode MOS transistor. Further processing continues as before.

WHAT WE CLAIM IS:—

1. A transistor structure comprising semiconductor material containing a source region and a drain region,

a layer of gate insulation overlying the surface of the semiconductor material between the source and drain regions,

a layer of field insulation overlying the semiconductor material surrounding the source and drain regions and the region between the source and drain regions, insulation bridging the field insulation to the gate insulation and gradually tapering from the thickness of the field insulation layer to the thickness of said gate insulation,

a gate electrode formed over the gate insulation between the source and drain regions,

passivation material covering the top surfaces of the source and drain regions, the gate electrode and the field insulation, and

contact leads contacting the source and drain regions and the gate electrode.

2. A transistor structure as claimed in claim 1 in which the insulation bridging the gate and field insulation comprises a first section extending from the gate insulation toward the field insulation and a second section extending from the first section to the field insulation, the first section having a thickness which increases gradually from the thickness of the gate insulation to a peak, the top surface of the first section rising gradually to the peak, and the first section ending at the peak, the second section beginning at the peak and having a thickness equal to that of the first section beneath the peak and which remains approximately constant for a selected distance and then gradually increases to the position at which the second section joins the field insulation, the second section having a top surface which in the region adjacent the peak has a slope opposite in sign to that of the top surface of the first section, and the top surface of the second section forming a trough between the peak and the field insulation.

3. A transistor structure as claimed in claim 1 or 2 in which the gate insulation overlies parts of the source drain regions.

4. A transistor structure as claimed in claim 1, 2 or 3 in which the insulation bridging the gate and field insulation overlies the peripheries of the source and drain regions and field regions directly adjacent the source and drain regions.

5. A transistor structure as claimed in claim 1, 2, 3 or 4 in which at least one of the gate insulation and the field insulation is of substantially uniform thickness.

6. A transistor structure as claimed in any preceding claim in which the insulation comprises an oxide of the semiconductor material.

7. A transistor structure as claimed in any preceding claim in which the semiconductor material comprises silicon.

8. A transistor structure as claimed in any preceding claim in which the gate electrode comprises selectively doped polycrystalline silicon.

9. A transistor structure as claimed in any preceding claim in which the gate insulation has a thickness in the range of 500 to 1,000 angstroms.

10. A transistor structure substantially as herein described with reference to Figs. 1*h* and 2 of the accompanying drawings.

11. A method of manufacturing a transistor structure, the method comprising the steps of forming source and drain regions in semiconductor material, forming a gate electrode between the source and drain regions, the gate electrode being separated from the semiconductor material between the source and drain regions by a layer of gate insulation, forming a thick field insulation layer over the field of the transistor and forming conductive contacts to the source and drain regions and the gate electrode, the gate insulation being formed before the formation of the field insulation so that insulation bridging the field insulation to the gate insulation tapers in thickness gradually from that of the field insulation to that of the gate insulation adjacent the source and drain regions and the gate electrode of the transistor structure.

12. A method as claimed in claim 11 having the steps of forming a first layer of oxide of semiconductor material to constitute the gate insulation over a substrate of the semiconductor material,

forming a layer of silicon nitride over the oxide layer.

forming a relatively thick second layer of silicon dioxide over the layer of silicon nitride,

removing those portions of the second layer of silicon dioxide and the layer of silicon nitride over those regions of the semiconductor material in which the source, drain and gate regions will not be formed,

growing additional oxide of the semiconductor material on those portions from which the second layer of silicon dioxide and the layer of silicon nitride have been removed to constitute the field insulation, the additional oxide being grown through the first layer, and

* C L M S *

removing the remaining portions of the silicon nitride and the second layer of silicon dioxide to leave exposed the top surfaces of the first layer and the additional oxide.

13. A method as claimed in claim 12 having the step of forming on the layer of silicon nitride prior to the forming of the second layer of silicon dioxide a thin layer of oxide by oxidizing the top portion of the layer of silicon nitride.

14. A method as claimed in claim 11 having the steps of

forming on a substrate of the semiconductor material a first layer of insulation from an oxide of semiconductor material to constitute the gate insulation,

forming a layer of silicon nitride over the first layer of insulation,

forming a layer of silicon oxide on the top surface of the layer of silicon nitride,

removing all silicon nitride and overlying silicon oxide to expose the gate insulation overlying the field of the transistor structure,

implanting a selected impurity in the semiconductor material throughout the field,

growing additional oxide of the semiconductor material over the field to constitute the field insulation, and

removing that silicon nitride remaining on the substrate together with any silicon oxide overlying the silicon nitride.

15. A method as claimed in claim 11 having the steps of

forming on a substrate of the semiconductor material a first layer of insulation from an oxide of the semiconductor material to constitute the gate insulation,

forming a layer of silicon nitride over the first layer of insulation,

forming a thin layer of oxide on the top surface of the layer of silicon nitride by oxidizing the top surface of the layer of silicon nitride,

removing all silicon nitride except that overlying the region of the substrate in or on which will be formed the source and drain regions and the gate electrode,

removing the gate insulation overlying the field region to leave exposed the top surfaces of regions of the semiconductor material, the gate insulation having been exposed by the removal of said silicon nitride layer,

placing a selected impurity in the exposed regions of the semiconductor material,

growing an oxide of the semiconductor material over the field to constitute the field insulation, and

then removing the nitride layer overlying the source, drain and gate regions.

16. A method as claimed in any one of claims 12 to 15 having the steps of forming a layer of photoresist material capable of absorbing ion-implanted impurities over those portions of the structure in which it is desired not to implant ions, but leaving exposed the gate insulation overlying those regions of said semiconductor material in which the source, drain and gate regions will be formed,

forming an ion-implanted layer in said semiconductor material beneath the gate insulation not covered with the photoresist material, and

removing the photoresist from the surface of the structure.

17. A method as claimed in any one of claims 12 to 15 having the steps of growing additional gate insulation over the portions of gate insulation exposed by the removal of the silicon nitride layer, and

removing the silicon nitride remaining on the structure together with any silicon oxide overlying the silicon nitride.

18. A method as claimed in any one of claims 12 to 17 having the steps of forming a layer of polycrystalline silicon over the top surface of the structure,

forming a gate electrode and conductive leads from the polycrystalline silicon, and

forming the source and drain regions in the underlying semiconductor material while simultaneously doping at least that polycrystalline silicon between the source and drain regions.

19. A method as claimed in claim 18 having the step of using the polycrystalline silicon gate electrode to mask the semiconductor material between the source and drain regions.

20. A method as claimed in any one of claims 12 to 17 having the steps of forming a layer of polycrystalline silicon over the top surfaces of the structure,

forming windows through selected portions of the polycrystalline silicon to expose the top surfaces of those portions of the first layer overlying those regions of the semiconductor material in which will be formed the source and drain regions,

removing at least parts of the exposed regions of the first layer to expose the top surfaces of those regions of the semiconductor material in which will be formed the source and drain regions, and

forming the source and drain regions in the underlying semiconductor material and simultaneously doping that polycrystalline silicon overlying that portion of the first layer of oxide between the source and drain regions and any other exposed polycrystalline silicon.

21. A method as claimed in claim 20 having the step of forming openings in the first layer to expose selected regions of the semiconductor material before forming the layer of polycrystalline silicon.

22. A method as claimed in claim 20 having the additional step of removing all polycrystalline silicon from the surface of the structure except for that polycrystalline silicon which will form the gate electrode and at least one conductive region.

23. A method as claimed in any one of claims 18 to 22 having the steps of forming a passivation layer over the top surfaces of the polycrystalline silicon and any other exposed materials,

forming windows in the passivation layer to expose diffused regions in the underlying semiconductor material to which electrical contact must be made, and

forming conductive leads over the top surface of the passivation layer, the conductive leads contacting through the windows in the passivation layer the underlying diffused regions in the semiconductor material and selectively contacting the polycrystalline silicon.

24. A method of manufacturing a transistor structure substantially as herein described with reference to the accompanying drawings.

25. A transistor structure manufactured by the method claimed in any one of claims 11 to 24.

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