Attorney Docket No. TI-20195

METHOD FOR ASSEMBLING AN INTEGRATED CIRCUIT PACKAGE

TECHNICAL FIELD OF THE INVENTION

The present invention relates in general to the field of integrated circuit packages and more specifically to a method for assembling an integrated circuit package by applying a liquid adhesive layer between the silicon chip and the printed circuit board and eliminating the need for encapsulation.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:39

This Sheet Has Been Replaced

BACKGROUND OF THE INVENTION

Without limiting the scope of the invention, its background is described in connection with integrated circuit packages, as an example.

Heretofore, in this field, integrated circuits have been formed on semiconductor wafers. The wafers are separated into individual silicon chips and the individual silicon chips are then handled and packaged. The packaging process is one of the most critical steps in the integrated circuit fabrication process, both from the point of view of cost and of reliability. Specifically, the packaging cost can easily exceed the cost of manufacturing the integrated circuit silicon chip as the majority of device failures are packaging related.

The integrated circuit must be packaged in a suitable media that will protect it during subsequent manufacturing steps and from the environment of its intended application. Wire bonding and encapsulation are the two main steps in the packaging process. Wire bonding connects leads from the silicon chip to the terminals of the package. The terminals allow the integrated circuit package to be connected to other components. Following wire bonding, encapsulation is employed to seal the surfaces from moisture and contamination.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:39

This Sheet Has Been Replaced



Encapsulation also protects the wire bonding and other components from corrosion and mechanical shock.

Conventionally, the packaging of integrated circuits has involved using an adhesive tape to attach an individual silicon chip to a lead frame, usually a printed circuit board. Following wire bonding and encapsulation, designated parts of the lead frame become the terminals of the package. The packaging of integrated circuits has also involved the placement of silicon chips on a flexible board where, following adhesion of the silicon chip to the surface of the flexible board and wire bonding, an encapsulant is placed over the silicon chip and flexible board assembly to seal and protect the chip and other components.

Unfortunately, current methods for encapsulating silicon chips have led to various problems, including cracking between the encapsulation material and the integrated circuit components. Also, high failure rates are encountered due to the multi-step nature of the process. Cracking has plagued the industry because of differences in the coefficient of thermal expansion of the different components, for example, between the soldering materials at the different interfaces and between metallic and non-metallic components. Cracking also occurs between the silicon chip and the encapsulation

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:39

This Sheet Has Been Replaced

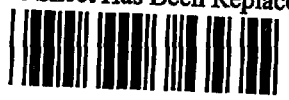
materials, usually epoxies, due to the extreme variations in temperature in various environments and between periods of operation and non-operation.

Even if the encapsulated silicon chip is successfully assembled into a working integrated circuit, another problem is commonly encountered. Once the silicon chip is encapsulated it is typically surface mounted using radiant heat or vapor saturated heating. This process, however, can lead to poor coplanarity due to uneven reflow, leading to integrated circuit failure.

Therefore, a need has arisen for an integrated circuit package and a process for producing the same that reduces cracking, minimizes the overall integrated circuit package size and avoids poor coplanarity due to uneven flow. A need has also arisen for materials and methods that lead to increased yield by more closely matching the coefficient of thermal expansion of the materials used in the package. Further, a need has arisen for a flat integrated circuit package that provides protection during subsequent manufacturing and testing steps and from the environment of its intended purpose. A need has also arisen for an improved method of adhering a chip to a printed circuit board in the assembly of an integrated circuit package.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:39

This Sheet Has Been Replaced



SUMMARY OF THE INVENTION

The present invention disclosed herein comprises a method for assembling an integrated circuit package and a an integrated circuit package produced by the method of the present invention that utilizes an improved method of adhering a chip to a printed circuit board and that protects the components of the integrated circuit package during manufacturing and testing steps and from the environment of its intended purpose.

The method for assembling an integrated circuit package of the present invention comprises obtaining a substrate having a surface, applying a liquid adhesive on the surface of the substrate and contacting a chip to the liquid adhesive, thereby attaching the chip to the substrate. The liquid adhesive may be a liquid epoxy such as X-43-5000 or a liquid polyimide such as G7631 liquid polyimide or G8320 liquid polyimide. The chip may be attached to the substrate at an elevated temperature which may be between about 215 and 250°C. A curing agent may also be added to the liquid adhesive such as aliphatic amines, aromatic amines and anhydrides.

The integrated circuit package assembled by the method of the present invention comprises a substrate having an opening and first and second surfaces. The integrated circuit has a

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:39

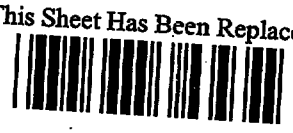
This Sheet Has Been Replaced

plurality of routing strips that are integral with the substrate and extend into the opening. A plurality of pads are disposed on the first surface, at least one of the pads disposed on the first surface being electrically connected with at least one of the routing strips on the substrate. A liquid adhesive is disposed between the second surface of the substrate and a chip having at least one bonding pad. Liquid adhesive is applied to either the substrate or the non electrically conductive surface of the chip, followed by attachment of the substrate and the chip. The chip has bonding pads that are wire bonded to electrically connect the bonding pads on the chip to the routing strips of the substrate.

The liquid adhesives for use with the present invention are liquid thermosetting plastics, such as epoxies or polyimides. In one embodiment, the plastic is a X-43-5000 liquid epoxy, which is applied between the substrate and the chip and provides superior strength and lower environmental impact. In another embodiment, the adhesive layer used to assemble the integrated circuit package of the present invention is a multifunctional epoxy having two or more epoxide rings in the molecule. Alternatively, liquid polyimides may be used as the liquid adhesive. Examples of

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:39

This Sheet Has Been Replaced

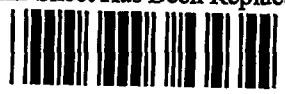


polyimides for use with the present invention are G7631 and G8320.

The integrated circuit package of the present invention may also include solder balls located on the pads disposed on the first surface of the substrate. Alternatively, solder columns may replace solder balls on the pads of the substrate. The present invention also encompasses an integrated circuit package made using the method of the present invention as described herein.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:38

This Sheet Has Been Replaced



BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the features and advantages of the present invention, reference is now made to the detailed description of the invention along with the accompanying figures in which corresponding numerals in the different figures refer to corresponding parts and in which:

Figure 1 is a simplified end cross-sectional view of an integrated circuit package of the present invention;

Figure 2 is a simplified top view of an integrated circuit package of the present invention; and

Figure 3 is a simplified end cross-sectional view of an integrated circuit package of the present invention.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:38

This Sheet Has Been Replaced



DETAILED DESCRIPTION OF THE INVENTION

While the making and using of various embodiments of the present invention are discussed in detail below, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of specific ways to make and use the invention and do not delimit the scope of the invention.

The present invention is related to high frequency integrated circuits using a board-on-chip design to achieve high speed performance and to meet the space constraint requirements of modern semiconductors. The principles of the present invention may be incorporated into, for example, a synchronous DRAM (SDRAM) silicon chip. The present invention, however, is also applicable to LOGIC, SRAM, EPROM and any other integrated circuit components.

Figure 1 is a simplified cross-sectional view of an integrated circuit package that is generally designated 30. The integrated circuit package 30 comprises a silicon chip 50, which can be, for example, any integrated circuit component such as a DRAM, an EPROM, a SRAM or a LOGIC chip. A printed

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:38

This Sheet Has Been Replaced



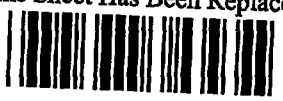
circuit board 70 is attached to the silicon chip 50 by an adhesive layer 60.

The adhesive layer 60 of the present invention may be made of, for example, a liquid thermo-setting plastic such as liquid epoxy or a polyimide. Epoxies are used because of their toughness, processibility, rigidity, chemical resistance, low shrinkage and adhesive properties. Epoxies are also used because they can adhere to a wide variety of substrates, organic and inorganic. While there are many different epoxy resins, most commonly epoxies are formed by reacting diglycidyl esters of Bisphenol-A with epichlorolhydrin. In many cases, bromine is reacted into the phenol ring section of the molecule to improve flame retardance. Multifunctional epoxies may also be used with the present invention, and are characterized by having more than two epoxide rings per monomer.

The basic epoxy resin may be cured or crosslinked by adding a coreactant or catalyst. Many different compounds can react with either the epoxide ring or the hydroxyl group of the epoxy ring such as aliphatic amines, aromatic amines and anhydrides, or catalysts such as piperidine or boron trifluoride ethylamine. The advantage of using an aliphatic amine as a curing agent for epoxies is that curing occurs at

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:38

This Sheet Has Been Replaced



room temperature or temperatures slightly above room temperature, the curing is fast, it is resistant to low heat and is a high exotherm. Examples of aliphatic amines that may be used to cure epoxies include diethylene triamine or dicyandiamide, for example. Alternatively, an aromatic amine may be used to cure the epoxy, the advantages being a long pot life, elevated curing temperatures and higher heat resistance. Samples of aromatic amines that may be used with the present invention include metaphenylene diamine or diamino diphenyl sulfone. Alternatively, anhydrides may be used, such as hexahydrophthalic anhydride. Anhydrides may be selected because they are safer, have a very long pot life, can be cured at an elevated temperature and have very high heat resistance.

Another advantage of epoxy based adhesives is that they can be made with any viscosity, from liquid to solid, and can be flexible or rigid, based on the types of mineral fills or fibers that are used to fill the epoxy. Another advantage of epoxies is that they can be combined with glass containing fabrics to produce laminated printed circuit boards, such as FR-4.

Alternatively, the liquid adhesive 60 used with the present invention can be a polyimide polymer. Polyimide

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:38

This Sheet Has Been Replaced



polymers can be used as an adhesive due to their heat resistance at cryogenic temperatures and their radiation resistance. Polyimides also have favorable electric properties and low outgassing, making them extremely useful in the extreme environment of space and at high temperature. Typically, copolymers used to polymerize polyimides are amideimide, imide phenolics, bismaleimide, epoxy imides and polyester imides.

Alternatively, the adhesive layer 60 may be a liquid epoxy such as X-43-5000, available from Shi-Etsu Chemicals, Ltd., or polyimides such as G7631, -G8320 or Hitachi HM122u. The bonding process generally involves attaching the silicon chip 50 on the printed circuit board 70 at a temperature above room temperature and allowing the epoxy or polyimide liquid adhesive to cure.

An important parameter of polymeric materials is the glass transition temperature, T_g. The T_g is the temperature at which long-range co-operativity between polymer chains becomes sufficient to allow the material to deform in response to an external force. For use with the present invention a temperature of about 215 and 250°C during processing is used to cure the thermosetting adhesive for use in the process of the present invention.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:38

This Sheet Has Been Replaced



The printed circuit board 70 may be constructed from a material such as FR-4 which is available from, for example, Motorola Inc., U.S.A. FR-4 is an epoxy resin reinforced with a woven glass cloth. In selecting the material for printed circuit board 70, one skilled in the art will recognize that four parameters should be considered, namely, thickness, dielectric constant, glass transition temperature and the coefficient of thermal expansion.

Thickness is dependant on the number of layers required and the amount of reinforcement used in a given layer. The reinforcing glass cloth can range in thickness from 2 mil per sheet (type 106) to about 8 mil per sheet (type 7628). Dielectric constant is determined by a combination of the resin used and the thickness and type of reinforcement used. Standard FR-4 has a dielectric constant of about 4.5. This constant can be reduced to about 3 by replacing the epoxy resin with a cyanate ester resin. The greater the thickness, however, the greater the problems associated with thickness control, rough surfaces, excessive drill reflection and poor resin refill.

The temperature at which a resin changes from a glass-like state into a "rubbery" state is generally designated as T_g. Standard FR-4 is made with a bifunctionally polymerizing

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:37

This Sheet Has Been Replaced



epoxy that has a T_g of about 110 °C. Higher T_g temperatures, such as 125-150 °C may be withstood by using a tetrafunctional epoxy. For higher T_g values, in the range of 150 to 200 °C a cyanate ester:epoxy blend can be used. Additionally, polyimides provide for printed circuit boards having a T_g above 250 °C.

The coefficient of thermal expansion for FR-4 is about 16 ppm/°C. A difference in the coefficient of thermal expansion between the printed circuit board 70 made from FR-4 and the silicon chip 50 can lead to failure of the integrated circuit package 30 during, not only the assembly of the integrated circuit package 30, but also during the use of integrated circuit package 30.

Referring collectively to Figures 1 and 2, intermediate layer 74 has routing strips 82 that are electrically connected through vias 84 to pads 100 located on top surface 92 of top layer 72 and bottom surface 94 of bottom layer 78. It should be understood by one skilled in the art that the terms "top" and "bottom" as well as the terms "side" and "end" are used for illustration purposes only, as the integrated circuit package 30 of the present invention can be assembled and used in a variety of positions and ways.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:37

This Sheet Has Been Replaced

Intermediate layer 76 includes a pair of bus bars 110. The bus bars are electrically connected through vias 84 to one or more of the pads 100. The bus bars 110 may serve, for example, as power supplies or grounds, and it is preferred that one bus bar 110 serve one function, such as a power supply, and the second bus bar 110 serve another function, such as a ground.

The silicon chip 50 has bonding pads 120 located generally in the central area of silicon chip 50. The bonding pads 120 are connected to routing strips 82 and bus bars 110 by wire bonding 80. Solder balls 150 are located on pads 100 to allow integrated circuit package 30 to be attached to other components, such as a motherboard or a single in-line memory module. Although described as solder balls 150, solder columns are also encompassed by the present invention.

Even though Figure 1 depicts printed circuit board 70 as having four layers 72, 74, 76 and 78, it should be understood by one skilled in the art that printed circuit board 70 may consist of a single layer or may be a multi-layered board having an alternate number of layers.

The above described components and their constructions and interrelation provide an assembly that does not require encapsulation. The term "assembly" refers to the assembled

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:37

This Sheet Has Been Replaced

components without the need for encapsulation. The assembly consists of printed circuit board 70, adhered silicon chip 50 and wire bonding 80. The printed circuit board 70 has a top opening 86 and a cavity 88 with routing strips 82 and bus bars 110 extending into the top opening 86. The top opening 86 and the cavity 88 are open with respect to one another.

The wire bonding 80 process may begin after silicon chip 50 has been adhered to printed circuit board 70. Silicon chip 50 and printed circuit board 70 are then positioned on a heated pedestal to raise the temperature of the combination to a point between 100°-300°C. A gold wire having a diameter typically ranging from 0.7 mil. to 1.3 mil. is strung through a heated capillary where the temperature may range between 200°-500°C. A soldering ball is created at the end of the wire using either a flame or a spark technique. This soldering ball is then brought to bonding pad 120 or the silicon chip 50 and a combination of compression force and ultrasonic energy are used to create the desired metallurgical bond. Using this "stitch" technique significantly reduces the cross-section of the wire at that point. A loop is then created in the wire bonding 80 above the bond that has just been achieved, and the wire bonding 80 is routed to the desired connection on the printed circuit board 70 such as

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:37

This Sheet Has Been Replaced

routing strip 82 or bus bar 110. The wire bonding 80 is clamped and the capillary raised, such that the wire bonding 80 will break free at the outer edge of the bond. This process is repeated until all the bonding pads 120 that require electrical connection on the silicon chip 50 are electrically connected to printed circuit board 70.

Following the assembly of the above-described components, top opening 86 may be filled with a potting material 90, represented by the dashed line above top opening 86. In one preferred embodiment of the present invention, cavity 88 is not filled with potting material 90. Instead, the non-operative side of the silicon chip 50 is left exposed. This arrangement reduces the overall size of the SIMM and lessens the environmental impact caused by the chemicals used in the encapsulation process.

In another embodiment of the present invention there is no cavity 88 and the silicon chip 50 is adhered to the bottom surface of the printed circuit board 70. Clearly, there are other permutations that can be used in arranging the silicon chip 50 on the printed circuit board 70 as will be apparent to those of skill in the art in light of the present disclosure.

A potting material 90 for use with the present invention may be a cyanate ester-type resin available from Shin-Etsu

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:37

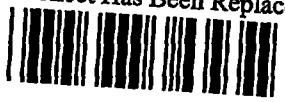
This Sheet Has Been Replaced

Chemical Co., Ltd., such as KMC 184VA and KMC 188VA-4. Other examples of potting materials 90 that may be used with the present invention include epoxies, polyesters, polyimides, cyanoacrylates, ceramic, silicone and urethane. The potting materials 90 may also contain fillers that affect the coefficient of thermal expansion, as well as the strength and flexibility of the potting material 90.

The solder balls 150 used with the present invention may be attached to the pads 100 using conventional solder reflow systems. For example, a vapor phase solder reflow system may be used, which condenses vapor to surround the integrated circuit package 30 and the printed circuit board 70 with a cloud of steam. A liquid, such as a nonchlorinated (non CFC) fluorocarbon is first heated with enough energy to form a vapor and to sustain a vapor cloud. When the integrated circuit package 30 is then passed through the vapor, the vaporized liquid condenses thereon and gives off the latent heat of vaporization. This energy is then transferred to the integrated circuit package 30. As long as the integrated circuit package 30 remains in the vapor, the vapor continues to give off energy at a repeatable fixed rate and temperature, until the integrated circuit package 30 reaches the temperature of the vapor.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:36

This Sheet Has Been Replaced



The advantage of using a nonchlorinated fluorocarbon is that it is extremely thermally stable, colorless, odorless and nonflammable. In addition, it has a low toxicity, low surface temperature, low boiling point, and low heat of vaporization. Because the fluid form of the non-chlorinated fluorocarbon is inert, it does not react with fluxes or component materials, nor does it absorb oxygen or other gases that cause reactions during the solder reflow. Most commercially available fluorocarbons used for vapor phase reflow are formulated to vaporize at precisely stable reflow temperatures for different solder materials, as will be known to those skilled in the art.

The vaporization temperature will depend on the solder type being used. A brief list of the temperatures that are used to vaporize different solder types is shown below.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:36

This Sheet Has Been Replaced

Vaporization Temperatures and Solder Types

Fluid Temperature	Solder Type
56, 80, 97, 101, 102°C and 155°C	100 In 37 Sn/38 Pb/25 In
165°C	70 Sn/18 Pn/12 In 70 In/30 Pb
174°C	60 In/40 Pb
190°C	90 In/10 Ag 50 In/50 Pb 63 Sn/37 Pb 70 Sn/30 Pb 60 Sn/40 Pb
215°C and 230°C	60 Sn/40 In 60 Sn/40 Pb 63 Sn/37 Pb 70 Sn/30 Pb 62 Sn/36 Pb/2 Ag
240°C and 253°C	75 Pb/25 In 81 Pb/19 In
260°C and 265°C	96.5 Sn/3.5 Ag

Alternatively, infrared or radiant heated solder reflow may be used. In such a system each component of the soldering system is directly exposed to radiation from a heating element. Heat from the radiant energy element is absorbed by the different components according to its molecular structure.

Conventional radiant heat systems expose only the outer surfaces of the components to the radiant heat, which may not reach interior areas as efficiently as with vapor saturated heating methods as described above. The present invention,

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:36

This Sheet Has Been Replaced



however, is not affected by this typical problem because solder balls 150 may be used instead of leads. In fact, due to the reduced overall size of the integrated circuit package 30 of the present invention either method, vapor phase solder reflow or radiant heated solder reflow, may be effectively used with the present invention.

The present invention also solves other problems associated with solder reflow systems. These problems include the creation or failure due to voids, coplanarity, tombstoning, open joints, component cracking, thermal shock and thermal stressing. The present invention solves these problems because it dispenses with the need for electrically connecting soldering leads to the integrated circuit package 30 followed by encapsulation. By using solder balls 150 instead of leads, the problems associated with voids around pad areas or under leads caused by incomplete reflow or poor welding of the soldering surface due to improper flux or badly oxidized surfaces is eliminated. The problems of coplanarity and tombstoning are also reduced or eliminated using the solder balls 150 because surface tension on both sides of the solder balls 150 is equal.

Open joints are usually caused by problems with coplanarity, while cracking may occur when trapped moisture

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:36

This Sheet Has Been Replaced

within an integrated circuit package expands as the device is heated for reflow. The increase in internal pressure, causes the integrated circuit package to split open, usually at one of the corners. The splitting of the package causes wire bonding from the lead frame to the silicon chip to break and in some cases the silicon chips have cracked due to the warpage at the top of the package as the temperature differentials between the top and the bottom of the device cause different rates of expansion.

Using the present invention, the only surface temperature differential that occurs is between the solder ball 150 and the printed circuit board 70, which allows either vapor phase solder reflow or radiant heat solder reflow to be available for producing the present invention. The small size of the solder balls 150, and of the integrated circuit package 130 as a whole, allows for any of the reflow systems to be usec with the because the temperature differential between the components is almost negligible. Furthermore, by selecting a potting material 90 having a coefficient of thermal expansion similar, or equal to, the coefficient of thermal expansion of the other components of the integrated circuit package 30, heat reflow effects and problems can be minimized.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:36

This Sheet Has Been Replaced



Although the board-on-chip layout of integrated circuit package 30 as depicted in Figures 1 and 2 has been described using centralized bonding pads 120, it should be understood by one skilled in the art that the principles of the present invention are applicable to a silicon chip 50 with bonding pads 120 in alternate layouts such as positioned along the sides of the silicon chip 50.

Also, it should be noted by one skilled in the art that pads 100 and bus bars 110 may be located on a single layer of printed circuit board 70. Generally, a layer of insulated tape or coating may be placed on the bus bars 110 to provide for electrical isolation. The advantage of a multi-layer printed circuit board 70, however, is the elimination of the need to insulate the bus bars 110. The present invention disposes with the need for isolation. Additionally, the multi-layer printed circuit board 70 provides a greater process margin for wire bonding.

Figure 3 is a simplified cross-sectional view of another embodiment of an integrated circuit package of the present invention that is generally designated 32. The integrated circuit package 32 comprises a silicon chip 50 and a printed circuit board 70 that is attached to the silicon chip 50 by an adhesive layer 60. In this embodiment, the printed circuit

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:35

This Sheet Has Been Replaced

board 70 consists of three layers, a top layer 72, an intermediate layer 74 and a bottom layer 76. The printed circuit board 70 has a top opening 86. As best seen in figure 2, routing strips 82 and bus bars 110 extend into the top opening 86. After assembly, top opening 86 is filled with potting material 90 as represented by the dashed line above top opening 86 and around silicon chip 50. Vias 84 electrically connect pads 100 located on top surface 92 of top layer 72 and bottom surface 94 of bottom layer 78.

The present invention allows for decreased failure due to the reduced number of adhesive, coating and encapsulation materials having varying coefficients of thermal expansion. The present invention further reduces the overall number of steps in the assembly of, for example, memory units by streamlining the assembly process not only in reduced number of steps, but also by eliminating the curing steps associated with encapsulating integrated circuits. The present invention further reduces the amount of material used in producing integrated circuit packages 30, thereby saving time, money and the environment.

Furthermore, the method of the present invention takes advantage of the opening 86 at the center of the printed circuit board 70 for potting the wire bonding 80 that connect

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:35

This Sheet Has Been Replaced



the silicon chip 50 and the printed circuit board 70 in a single step. By filling the opening 86 with potting material 90, the wire bonding 80 between silicon chip 50 and the printed circuit board 70 are generally protected from the environment and are particularly protected from moisture due to the hermetic nature of the encapsulation.

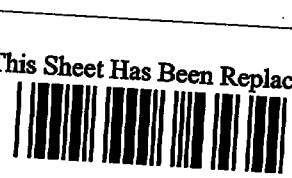
This means of adhering the components of the integrated circuit package 30 of the present invention greatly reduces the overall profile by allowing the non-operative or backside of the silicon chip 50 to be exposed. By hermetically protecting the connections between the silicon chip 50 and the printed circuit board 70 at the top opening 86, there is no need to completely encapsulate the entire assembly.

Additionally, reduced environmental impact is obtained using the method and apparatus of the present invention due to the overall decrease in the size of the integrated circuit package 30. Reduced environmental impact is also achieved by eliminating the number of components required to assemble an integrated circuit package 30.

This invention reduces warpage caused by resin shrinkage by eliminating the need for resin on the backside of the silicon chip's housing. In addition, the overall size of the integrated circuit package is reduced by eliminating the need

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:35

This Sheet Has Been Replaced



for a housing for the silicon chip, thus creating a stress-free condition. Eliminating the housing for the chip also minimizes the shrinkage and cracking due to the shrinkage of the encapsulating resin.

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:35

* C L M S *

What is claimed is:

1. A method for assembling an integrated circuit package comprising the steps of:

obtaining a substrate having a surface;

applying a liquid adhesive on said surface of said substrate; and

contacting a chip to said liquid adhesive, thereby attaching said chip to said substrate.

2. The method as recited in claim 1 wherein said liquid adhesive is a liquid epoxy.

3. The method as recited in claim 2 wherein said liquid adhesive is further defined as being a X-43-5000 liquid epoxy.

4. The method as recited in claim 1 wherein said liquid adhesive is a liquid polyimide.

5. The method as recited in claim 4 wherein said liquid polyimide is selected from the group consisting of a C7631 liquid polyimide and a G8320 liquid polyimide.

This Sheet Has Been Replaced

Received Time 5. Feb. 22:19 Print Time 5. Feb 22:35

* C L M S *

6. The method as recited in claim 1 wherein the step of contacting a chip to said liquid adhesive occurs at a temperature between about 215 and 250°C.

7. The method as recited in claim 1 further comprising the step of adding a curing agent to said liquid adhesive.

8. The method as recited in claim 7 wherein said curing agent is selected from the group consisting of aliphatic amines, aromatic amines and anhydrides.

This Sheet Has Been Replaced

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:35

* C L M S *

9. A method for assembling an integrated circuit package comprising the steps of:

obtaining a chip having a surface;

applying a liquid adhesive on said surface of said chip; and

contacting a substrate to said liquid adhesive, thereby attaching said substrate to said chip.

10. The method as recited in claim 9 wherein said liquid adhesive is a liquid epoxy.

11. The method as recited in claim 10 wherein said liquid adhesive is further defined as being a X-43-5000 liquid epoxy.

12. The method as recited in claim 9 wherein said liquid adhesive is a liquid polyimide.

13. The method as recited in claim 12 wherein said liquid polyimide is selected from the group consisting of a G7631 liquid polyimide and a G8320 liquid polyimide.

This Sheet Has Been Replaced



Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:34

* C L M S *

14. The method as recited in claim 9 wherein the step of contacting said substrate to said liquid adhesive occurs at a temperature between about 215 and 250°C.

15. The method as recited in claim 9 further comprising the step of adding a curing agent to said liquid adhesive.

16. The method as recited in claim 15 wherein said curing agent is selected from the group consisting of aliphatic amines, aromatic amines and anhydrides.

This Sheet Has Been Replaced

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:34

17. An integrated circuit package assembled according to the method of claim 1.

18. The integrated circuit package as recited in claim 17 wherein said liquid adhesive is selected from the group consisting of a liquid epoxy and a liquid polyimide.

19. The integrated circuit package as recited in claim 17 wherein said chip is contacted to said liquid adhesive at a temperature between about 215 and 250°C.

20. The integrated circuit package as recited in claim 17 further comprising the step of adding a curing agent to said liquid adhesive.

This Sheet Has Been Replaced

Received Time 5. Feb. 22:19 Print Time 5. Feb. 22:34