INTEGRATED CIRCUIT MANUFACTURE

The present invention relates to integrated circuit (IC) manufacture and particularly to a method of identifying rejects at the IC packaging stage.

In manufacture of ICs, the completed circuit, on a silicon substrate or chip, is physically attached to a lead frame or printed circuit board (PCB) substrate and electrical connections to the chip are made with gold wire. The connected chip is then encapsulated, e.g. in resin, to form the completed package.

At various stages in the manufacturing process the ICs are tested and marked as rejects if found to be defective in any way. How this marking is done depends on the stage of manufacture at which the reject is detected. If the encapsulation has not been completed, a known method is to attach a piece of polyimide adhesive tape on or near the rejected IC. If the encapsulation has been completed, it is known to use a diamond pen to mark, e.g. with an X, the surface of the reject IC. These methods have disadvantages. For example, marking with a diamond pen by hand does not always produce an easily visible or consistent mark.

Another known method of identifying rejects is to punch a hole in the lead frame adjacent the rejected unit. However, in this case, it is necessary to provide substantial space between the ICs on the lead frame to prevent damage being caused to other ICs when the hole is made. Punching a hole can cause stresses in the lead frame that affect neighbouring ICs and can deform the lead frame out of planarity.

On PCB substrates such as Ball Grid Array (BGA) substrates, rejects that are detected before encapsulation are known to be marked by writing on the substrate with a permanent marker or by punching a hole through the electrical circuitry. Both of these methods suffer from the defect that the mark is not visible after the encapsulation process.

According to the present invention, there is provided a method of manufacturing integrated circuits, the method comprising:

providing a substrate having an array of mounting positions for semiconductor devices and an array of predefined reject marking points corresponding to said mounting positions;

testing said substrate; and

where a fault is detected in said testing step, effecting a mark at the reject marking point corresponding to the mounting position at which the fault was detected.

The present invention also provides a substrate for mounting semiconductor devices, the substrate comprising:

an array of mounting positions for a plurality of semiconductor devices; and

an array of predefined reject marking points corresponding to respective mounting positions.

Preferably, the predefined reject mark comprises a partially formed through-hole which is completed to indicate a rejected IC. The partially formed through-hole may be an incomplete annular through-hole that leaves an island joined to the rest of the substrate by relatively narrow tie-bars. These are easily broken out to leave a complete through-hole. The island may be circular, which is usable if the substrate is a lead frame or ball grid array (BGA) substrate. Alternatively, the island may take the form of a zig-zag path or Greek key pattern, this is useful with BGA substrates.

In this way, the present invention allows the location of a faulty device to be quickly and reliably indicated. The use of a partial through-hole which is then completed to indicate a reject ensures that rejects are indicated by a through-hole of consistent size which ensures their recognition by human operators as well as vision recognition systems or other automated detectors.

The present invention is applicable to lead frame, BGA and other printed circuit board (PCB) substrates.

The present invention will be further described below with reference to exemplary embodiments and the accompanying drawings, in which:

Figure 1 is a schematic cross-sectional view of a lead-on-chip (LOC) DRAM device to the manufacture of which the present invention may be applied;

Figure 2 is a schematic view of a lead frame substrate to which the present invention is applied;

Figures 3A and B are enlarged views of the reject mark according to a first embodiment of the present invention;

Figures 4A and B are enlarged views of the reject mark according to a second embodiment of the present invention; and

Figure 5 is a schematic view of a lead frame substrate showing alternative ways in which the present invention may be applied.

In the drawings, like parts are identified by like references.

As shown in Figure 1, a silicon chip 1 is bonded to lead frame 2 by adhesive, e.g. polyimide, tape 3. Electrical connections are made by gold wires 4 which connects bond pads 5 on the chip to tracks on the lead frame 2. At the chip end the wires 4 are connected by gold ball bonds 6 and the lead frame 2 end by stitch bonds 7. The whole chip is then encased in resin to form the complete package 8.

Figure 1 shows a typical lead-on-chip (LOC) dynamic random access memory (DRAM) design but the present invention may be readily applied to other types of integrated circuit and other packaging methods.

A typical lead frame substrate will have a number of IC packages set out in a rectangular array. Figure 2 shows a lead frame substrate 2 having a 3x3 array of IC package mounts but other arrangements are possible.

In the embodiment of the invention shown in Figure 2, a row of predefined reject markers 10a-c is provided at the top of each column of IC package mounts, with one marker for each IC package mount in the column, in this case 3. The row of markers 10a-c is in this case inclined but may be horizontal or vertical as space permits. The inclination of the row forms a visual reminder that marker 10a corresponds to IC package mount 8a, marker 10b to IC package mount 8b and marker 10c to IC package mount 8c. Any suitable mapping of reject markers in their array to IC mount positions in their array may be used.

As shown enlarged in Figure 3A, each marker 10 comprises an island 11 joined to the remainder of the substrate by tie-bars 12. The island and tie bars are defined by making part-annular through-holes 13 in the substrate.

At various stages in the manufacturing process, the IC mounts, the associated wiring, the silicon chip mounted on each IC mount and the encapsulation are tested in various ways. If, at any stage, a mount or the IC mounted there fails a test and is considered a reject, the island 11 in the corresponding reject marker 10 is broken out to indicate the reject status of the associated IC. The island can easily be broken out by breaking the tie bars, either automatically or manually with an appropriate tool. Once broken out, the marker will appear as in Figure 3B, with only short stubs 12' of the tie bars remaining. The marker thus presents a through-hole of regular size and shape which can easily be detected visually or automatically.

In an alternative embodiment of the invention shown in Figure 4A, the marker takes the form of a zig-zag path or Greek key pattern 14 joined to the remainder of the substrate by two tie bars 15. When broken out, as shown in Figure 4B, a uniform through-hole is again presented and can again be easily recognised or detected.

As mentioned above, the predefined reject marking points of the invention need not be arrayed as shown in Figure 2. Instead, the array of reject marking points may be interleaved with the array of IC mounting positions. Figure 5 shows two possibilities. Reject marking points 20a to 20c, which may be the same as the reject marking points shown in Figures 3 and 4, are arrayed alongside the column of IC mounting positions with each reject marking point alongside the respective IC mounting position. Reject marking points 30a to 30c, which again may be the same as the reject marking points shown in Figures 3 and 4, are arrayed within the column of IC mounting positions with each reject marking point below the respective IC mounting position.



CLAIMS

1. A method of manufacturing integrated circuits, the method comprising:

providing a substrate having an array of mounting positions for semiconductor devices and an array of predefined reject marking points corresponding to said mounting positions;

testing said substrate; and

where a fault is detected in said testing step, effecting a mark at the reject marking point corresponding to the mounting position at which the fault was detected.

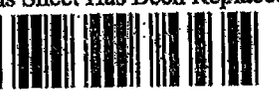
2. A method according to claim 1 wherein said step of providing a substrate comprises the step of partially forming through-holes in the substrate at said predefined reject marking points; and wherein said step of effecting a mark comprises completing the formation of a through-hole at the reject marking point corresponding to the mounting position at which the fault was detected.

3. A method according to claim 2 wherein said step of partially forming through-holes comprises forming an incomplete annular through-hole in the substrate to form an island connected to the remainder of the substrate by one or more tie-bars and said step of effecting a mark comprises breaking the or each tie bar to detach said island.

4. A method according to claim 3 wherein said island is disc shaped.

5. A method according to claim 3 wherein said island is in the shape of a zig-zag path.

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6. A method according to any one of the preceding claims, wherein said substrate comprises a lead frame or a printed circuit board such as a ball grid array substrate.

7. A method according to any one of the preceding claims, wherein said steps of testing and effecting a mark are carried out at one or more of: before mounting of ICs on the substrate, before encapsulation of ICs mounted on the substrate, and after encapsulation of ICs mounted on the substrate.

8. A substrate for mounting semiconductor devices, the substrate comprising:

an array of mounting positions for a plurality of semiconductor devices; and

an array of predefined reject marking points corresponding to respective mounting positions.

9. A substrate according to claim 8 wherein said reject marking points comprise partially formed through-holes in said substrate.

10. A substrate according to claim 9 wherein said partially formed through-holes comprise incomplete annular through-holes forming islands connected to the remainder of said substrate by one or more tie-bars.

11. A substrate according to claim 10 wherein said islands are circular in shape.

12. A substrate according to claim 10 wherein said islands have the shape of a zig-zag path.

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13. A substrate according to any one of claims 8 to 12 wherein said array of reject marking points is situated outside of the area covered by said array of mounting positions.

14. A substrate according to any one of claims 8 to 13 wherein each said reject marking points is located in the array thereof at a location corresponding to the location of its respective mounting position.

15. A method of manufacturing integrated circuits substantially as hereinbefore described with reference to the accompanying drawings.

16. A substrate for mounting integrated circuits constructed substantially as hereinbefore described with reference to the accompanying drawings.

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