voltage and current probe 111 is provided via the communication device 189 and a cable 193 to the host system 130. Examples of a communication device include an Ethernet device that converts data into Ethernet packets and converts Ethernet packets into data, an Ethernet for Control Automation Technology (EtherCAT) device, a serial interface device that transfers data in series, a parallel interface device that transfers data in parallel, a Universal Serial Bus (USB) interface device, etc.

**[0062]** Examples of the host system 130 include a computer, e.g., a desktop, a laptop, a tablet, etc. As an illustration, the host system 130 includes a processor and the storage HU 162. As used herein, a processor may be a central processing unit (CPU), a microprocessor, an application specific integrated circuit (ASIC), a programmable logic device (PLD), etc. Examples of the storage HU include a read-only memory (ROM), a random access memory (RAM), or a combination thereof. The storage HU may be a flash memory, a redundant array of storage disks (RAID), a hard disk, etc.

**[0063]** The impedance matching model 104 is stored within the storage HU 162. The impedance matching model 104 has similar characteristics, e.g., capacitances, inductances, complex power, complex voltage and currents, etc., as that of the impedance matching circuit 114. For example, the impedance matching model 104 has the same number of capacitors and/or inductors as that within the impedance matching circuit 114, and the capacitors and/or inductors are connected with each other in the same manner, e.g., serial, parallel, etc. as that within the impedance matching circuit 114. To provide an illustration, when the impedance matching circuit 114 includes a capacitor coupled in series with an inductor, the impedance matching model 104 also includes the capacitor coupled in series with the inductor.

**[0064]** As an example, the impedance matching circuit 114 includes one or more electrical components and the impedance matching model 104 includes a design, e.g., a computer-generated model, of the impedance matching circuit 114. The computer-generated model may be generated by a processor based upon input signals received from a user via an input hardware unit. The input signals include signals regarding which electrical components, e.g., capacitors, inductors, etc., to include in a model and a manner, e.g., series, parallel, etc., of coupling the electrical components with each other. As another example, the impedance matching circuit 114 includes hardware electrical components and hardware connections between the electrical components and the impedance matching model 104 ~~include~~ includes software representations of the hardware electrical components and of the hardware connections. As

## CLAIMS

1. A method for determining wafer bias, the method comprising:

detecting output of a generator to identify receiving, by a processor from an output of a generator, a generator output complex voltage and current, the generator coupled to an impedance matching circuit, the impedance matching circuit coupled via a radio frequency (RF) transmission line to an electrostatic chuck (ESC) of a plasma chamber;

determining, by the processor, from the generator output complex voltage and current a projected complex voltage and current at a point along a path between an output of a model of the impedance matching circuit and a model of the ESC, the determining of the projected complex voltage and current performed using a model for at least part of the path, the model for at least part of the path characterizing physical components along the path, the model for at least part of the path including an RF transmission model of the RF transmission line, wherein the RF transmission model includes a model of an RF tunnel and a model of an RF strap, the RF tunnel model coupled with the RF strap model; and

applying, by the processor, the projected complex voltage and current as an input to a function to map the projected complex voltage and current to a wafer bias value at the ESC model.

2. The method of claim 1, wherein the function is characterized by a summation of values that represent physical attributes of the path, wherein the projected complex voltage and current is used in the summation of the values.

3. The method of claim 2, wherein the physical attributes of the path are derived values from test data.

4. The method of claim 1, wherein the function is a sum of characterized values and a constant, the characterized values including magnitudes and coefficients, the magnitudes derived from the projected complex voltage and current, the coefficients and the constant incorporating empirical modeling data.

5. The method of claim 4, wherein the coefficients are coefficients of the magnitudes.

6. The method of claim 4, wherein the empirical modeling data includes data obtained based on measurements of wafer bias at the ESC, based on determinations of magnitudes of complex voltages and currents, and based on an application of estimation statistical method to the measurements of the wafer bias at the ESC and the magnitudes of complex voltages and currents, the determination of the magnitudes of complex voltages and currents made based on the model of the impedance matching circuit and the model for at least part of the path.

7. The method of claim 1, wherein the function includes a sum of a first product, a second product, a third product, and a constant, wherein the first product is a product of a coefficient and a voltage magnitude, the second product is a product of a coefficient and a current magnitude, the third product is a product of a coefficient and a square root of power magnitude, the voltage magnitude extracted from the projected complex voltage and current, the current magnitude extracted from the projected complex voltage and current, the power magnitude calculated from the current magnitude and the voltage magnitude.

8. A method for determining wafer bias, the method comprising:

receiving, by a processor, one or more generator output complex voltages and currents measured at one or more outputs of one or more generators, the one or more generators coupled to an impedance matching circuit, the impedance matching circuit coupled via a radio frequency (RF) transmission line to an electrostatic chuck (ESC) of a plasma chamber;

determining, by the processor, from the one or more generator output complex voltages and currents a projected complex voltage and current at a point along a path between a model of the impedance matching circuit and a model of the ESC, the ~~models~~ model of the impedance matching circuit characterizing ~~physical components along the path~~ the impedance matching circuit and the model of the ESC characterizing the ESC, wherein the path includes an RF transmission model of the RF transmission line, wherein the RF transmission model includes a model of an RF tunnel and a model of an RF strap, the RF tunnel model coupled with the RF strap model; and

calculating, by the processor, a wafer bias at the point by using the projected complex voltage and current as an input to a function.

9. The method of claim 8, wherein the function is characterized by a summation of values that represent physical attributes of the path, wherein the projected complex voltage and current is used in the summation of the values.

10. The method of claim 9, wherein the physical attributes of the path are derived values from test data.

11. The method of claim 8, wherein the function is a sum of characterized values and a constant, the characterized values including magnitudes and coefficients, the magnitudes derived from the projected complex voltage and current, the coefficients and the constant incorporating empirical modeling data.

12. The method of claim 11, wherein the coefficients are coefficients of the magnitudes.

13. The method of claim 11, wherein the empirical modeling data includes data obtained based on measurements of wafer bias at the ESC, based on determinations of magnitudes of complex voltages and currents, and based on an application of estimation statistical method to the measurements of the wafer bias at the ESC and the magnitudes of complex voltages and currents, the determination of the magnitudes of complex voltages and currents made based on the model of the impedance matching circuit and a model for at least part of the path.

14. The method of claim 8, wherein the function includes a sum of a first product, a second product, a third product, and a constant, wherein the first product is a product of a coefficient and a voltage magnitude, the second product is a product of a coefficient and a current magnitude, the third product is a product of a coefficient and a square root of power magnitude, the voltage magnitude identified from the projected complex voltage and current, the current magnitude identified from the projected complex voltage and current, the power magnitude determined from the current magnitude and the voltage magnitude.

15. A method for determining wafer bias, the method comprising:

identifying, by a processor, a first complex voltage and current measured at an output of a radio frequency (RF) generator when the RF generator is coupled to a plasma chamber via an impedance matching circuit, the impedance matching circuit having an input coupled to the output of the RF generator and an output coupled to an RF transmission line;

generating, by the processor, an impedance matching model based on electrical components defined in the impedance matching circuit, the impedance matching model having an input and an output, the input of the impedance matching model receiving the first complex voltage and current, the impedance matching model having one or more elements;

generating, by the processor, an RF transmission model based on circuit components defined in the RF transmission line, wherein the RF transmission model includes a model of an RF tunnel and a model of an RF strap, the RF tunnel model coupled with the RF strap model;

propagating, by the processor, the first complex voltage and current through the one or more elements from the input of the impedance matching model to the output of the impedance matching model to determine a second complex voltage and current, wherein the second complex voltage and current is at the output of the impedance matching model; and

determining, by the processor, a wafer bias based on a voltage magnitude of the second complex voltage and current, a current magnitude of the second complex voltage and current, and a power magnitude of the second complex voltage and current, wherein the wafer bias is determined using at least a portion of the RF transmission model.

16. The method of claim 15, wherein determining the wafer bias comprises:

calculating the power magnitude based on the voltage magnitude and the current magnitude; and

calculating a sum of a first product, a second product, a third product, and a constant, wherein the first product is of the voltage magnitude and a first coefficient, the second product is of the current magnitude and a second coefficient, and the third product is of a square root of the power magnitude and a third coefficient.

17. The method of claim 15, wherein determining the wafer bias is performed based on whether the RF generator is on.

18. The method of claim 15, ~~further comprising: generating an RF transmission model based on circuit components defined in the RF transmission line,~~ wherein the RF transmission model ~~having~~ has an input and an output, the input of the RF transmission model coupled to the output of the impedance matching model, the RF transmission model having a portion, wherein the wafer bias is determined at ~~the~~ an output of the RF transmission model portion.

19. The method of claim 15, ~~further comprising: generating an RF transmission model based on circuit components defined in the RF transmission line,~~ wherein the RF transmission model ~~having~~ has an input and an output, the input of the RF transmission model coupled to the output of the impedance matching model, wherein the wafer bias is determined at the output of the RF transmission model.

20. The method of claim 19, wherein the ~~electrical~~ circuit components of the RF transmission line include capacitors, or inductors, or a combination thereof, the RF transmission model including one or more elements, wherein the elements of the RF transmission model have similar characteristics as that of the ~~electrical~~ circuit components of the RF transmission line.

21. The method of claim 15, wherein the first complex voltage and current received is measured at the output of the RF generator with a voltage and current probe, the voltage and current probe calibrated according to a pre-set formula.

22. The method of claim 21, wherein the pre-set formula is a standard.

23. The method of claim 22, wherein the standard is a National Institute of Standards and Technology (NIST) standard, wherein the voltage and current probe is coupled with an open circuit, a short circuit, or a load to calibrate the voltage and current probe to comply with the NIST standard.

24. The method of claim 15, wherein the second complex voltage and current includes a voltage value, a current value, and a phase between the voltage value and the current value.

25. The method of claim 15, wherein the elements of the impedance matching model include capacitors, inductors, or a combination thereof, wherein the electrical components of impedance matching circuit include capacitors, inductors, or a combination thereof, wherein the elements of the impedance matching model have similar characteristics as that of the electrical components of the impedance matching circuit.

26. The method of claim 15, wherein the wafer bias is for use in a system, wherein the system includes ~~an~~ another RF transmission line and excludes a voltage probe on the other RF transmission line.

27. The method of claim 15, ~~further comprising: generating an RF transmission model based on electrical components defined in the RF transmission line,~~ wherein the RF transmission model ~~having~~ has an input and an output, the input of the RF transmission model coupled to the output of the impedance matching model~~; and~~, said method further comprising generating an electrostatic chuck (ESC) model based on characteristics of an electrostatic chuck of the plasma chamber, the ESC model having an input, the input of the ESC model coupled to the output of the RF transmission model, wherein the wafer bias is determined at the output of the ESC model.

28. The method of claim 15, wherein propagating the first complex voltage and current through the one or more elements from the input of the impedance matching model to the output of the impedance matching model to determine the second complex voltage and current comprises:

determining an intermediate complex voltage and current within an intermediate node within the impedance matching model based on the first complex voltage and current and characteristics of one or more elements of the impedance matching model coupled between the input of the impedance matching model and the intermediate node; and

determining the second complex voltage and current based on the intermediate complex voltage and current and characteristics of one or more elements of the impedance matching model coupled between the intermediate node and the output of the impedance matching model.

~~29. The method of claim 15, wherein the RF transmission model includes a model of an RF tunnel and a model of an RF strap, the RF tunnel model coupled with the RF strap model.~~

~~30.~~29. A plasma system for determining wafer bias, comprising:

one or more radio frequency (RF) generators for generating one or more RF signals, the one or more RF generators associated with one or more voltage and current probes, wherein the one or more voltage and current probes are configured to measure one or more complex voltages and currents at corresponding one or more outputs of the one or more RF generators;

an impedance matching circuit coupled to the one or more RF generators;

a plasma chamber coupled to the impedance matching circuit via an RF transmission line, the plasma chamber including an electrostatic chuck (ESC), the ESC coupled to the RF transmission line; and

a processor coupled to the one or more RF generators, the processor configured to:

receive the one or more complex voltages and currents;

determine from the one or more complex voltages and currents projected complex voltage and current at a point along a path between a model of the impedance matching circuit and a model of the ESC, the ~~models~~ model of the impedance matching circuit characterizing ~~physical components along the path~~the impedance matching circuit and the model of the ESC characterizing the ESC, wherein the path includes an RF transmission model of the RF transmission line, wherein the RF transmission model includes a model of an RF tunnel and a model of an RF strap, the RF tunnel model coupled with the RF strap model; and

calculate a wafer bias at the point by using the projected complex voltage and current as an input to a function.

~~31.~~30. The plasma system of claim ~~30~~29, wherein the function is characterized by a summation of values that represent physical attributes of the path, wherein the projected complex voltage and current is used in the summation of the values.

~~32.~~31. The plasma system of claim ~~31~~30, wherein the physical attributes of the path are derived values from test data.

~~33.~~32. The plasma system of claim ~~30~~29, wherein the function is a sum of characterized values and a constant, the characterized values including magnitudes and coefficients, the magnitudes derived from the projected complex voltage and current, the coefficients and the constant incorporating empirical modeling data.

~~34.~~33. The plasma system of claim ~~33~~32, wherein the coefficients are coefficients of the magnitudes.

~~35.~~34. The plasma system of claim ~~33~~32, wherein the empirical modeling data includes data obtained based on measurements of wafer bias at the ESC, based on determinations of magnitudes of complex voltages and currents, and based on an application of estimation statistical method to the measurements of the wafer bias at the ESC and the magnitudes of complex voltages and currents, the determination of the magnitudes of complex voltages and currents made based on the impedance matching model and a model for at least part of the path.

~~36.~~35. The plasma system of claim ~~30~~29, wherein the function includes a sum of a first product, a second product, a third product, and a constant, wherein the first product is a product of a coefficient and a voltage magnitude, the second product is a product of a coefficient and a current magnitude, the third product is a product of a coefficient and a square root of power magnitude, the voltage magnitude extracted from the projected complex voltage and current, the current magnitude extracted from the projected complex voltage and current, the power magnitude calculated from the current magnitude and the voltage magnitude.