



159159

AN ELECTRON EMITTER AND A DISPLAY APPARATUS UTILISING THE SAME

This application is cross referenced to a related co-pending application filed on the same
5 date, entitled “An electron emitter and a display apparatus utilizing the same”, naming
Takehisa Ishida and Wei Beng Ng as the inventors.

FIELD OF THE INVENTION

The present invention relates to an electron emitter and a display apparatus
10 utilising the same, particularly though not exclusively to a field effect electron emitting
apparatus, a field effect display, a method of fabricating a electron emitter array, and a
method of manufacturing a field effect display.

BACKGROUND

15 Recently Flat Panel Displays (FPD) have become popular due to their smaller
footprint and larger flatter screen compared to conventional technology. For example,
Liquid Crystal Displays (LCD) and Plasma Display Panels (PDP) are replacing Cathode
Ray Tubes (CRT) in many domestic applications. However some types of FPD
technology have disadvantages compared to conventional CRT technology. For example
20 LCDs have a slow response rate, which degrades the quality of fast-moving images and
PDPs have a reduced life expectancy.

An alternative technology to LCD or PDP is a Field Emission Display (FED). A
typical FED incorporates a large array of fine metal tips or carbon nano-tubes (CNT),



G00002

which emit electrons through a process known as field emission. The array of electron emitters lie behind a phosphor coated screen, which similar to a CRT, emits light when the electrons strike.

There are many challenges to the commercial fabrication of such devices. The
5 use of CNT electron emitters for example, may improve the potential performance of FEDs but adds further complexity to the fabrication process.

United States Patent publication number 2006/0046602 discloses a method of manufacturing a field emitter electrode using self-assembling carbon nanotubes as well as a field emitter electrode manufactured thereby. The method comprises anodizing an
10 aluminum substrate to form an anodized aluminum oxide film having a plurality of uniform pores on the aluminum substrate, preparing an electrolyte solution having carbon nano-tubes dispersed therein, immersing the anodized aluminum substrate in the electrolyte solution and applying a given voltage to the aluminum substrate as one electrode, so as to attach the carbon nano-tubes to the pores, and fixing the attached
15 carbon nano-tubes to the pores. The suggested application is as a back light for an LCD and a gate electrode is not disclosed.

The emitter current for those prior art devices above, can be quite high, which reduces the life expectancy. Also the CNT for those prior art devices above, are longer than the depth of the pore. In other words, the tips of the CNT are exposed from the pores.
20 It would therefore be desirable to provide an electron emitter array which has fast response, long lifetime, uniformity and/or high luminous intensity and/or improved methods of fabrication.

SUMMARY OF THE INVENTION

It is therefore the objective of at least one embodiment to provide a field effect emitting apparatus that overcomes at least one of the above mentioned problems.

In general terms, a first aspect of the invention proposes that in a field effect
5 emitting apparatus comprising an insulating layer having an array of pores, each pore has at least one nano-wire electron emitter which is shorter than the pore. This may give the advantage that a gate electrode may be provided on or near the insulating layer without the need for a spacer between them.

A second independent aspect of the invention is that each pore may have a
10 plurality of nano-wire electron emitters. This may give the advantage that the life of the emitter is improved because the current emitted from one nano-wire can be reduced to obtain the same amount of current in comparison with the case of using only one nano-wire in a single pore.

In a first specification expression of the invention there is provided a field effect
15 electron emitting apparatus comprising
a cathode,
an insulating layer on or adjacent to the cathode having an array of pores,
at least one nano-wire electron emitter within each pore, each nano-wire electron emitter being shorter than the pore and connected to the cathode, and
20 a gate electrode on or adjacent to the insulating layer.

In a second specification expression of the invention there is provided a field effect electron emitting apparatus comprising
a cathode,

an insulating layer on or adjacent to the cathode having an array of pores,
a plurality of nano-wire electron emitters in each pore connected to the cathode,
a gate electrode on or adjacent to the insulating layer.

In a third specification expression of the invention there is provided a field effect
5 electron emitting apparatus comprising

a cathode,
an insulating layer on or adjacent to the cathode having an array of pores,
at least one electron emitter within each pore, each electron emitter being shorter
than the pore and connected to the cathode,
10 a gate electrode on or adjacent to the insulating layer, and
a secondary electron emission (SEE) layer on the sidewall of each pore.

In a forth specification expression of the invention there is provided a field effect
display comprising
a field effect electron emitting apparatus as described above, and
15 a phosphor coated screen on or spaced parallel to the field effect electron
emitting apparatus.

In a fifth specification expression of the invention there is provided a method of
fabricating an electron emitter array comprising:
providing a cathode,
20 providing a insulating layer including an array of pores on or adjacent to the
cathode,
providing at least one nano-wire electron emitter within each pore, each
nano-wire electron emitter being shorter than the pore and connected to the cathode, and

providing a gate electrode on or adjacent to the insulating layer.

In a sixth specification expression of the invention there is provided a method of fabricating an electron emitter array comprising:

providing a cathode,

5 providing a insulating layer including an array of pores on or adjacent to the cathode,

providing a plurality of nano-wire electron emitters in each pore connected to the cathode, and

providing a gate electrode on or adjacent to the insulating layer.

10 In a seventh specification expression of the invention there is provided a method of fabricating an electron emitter array comprising

providing a cathode,

providing a insulating layer including an array of pores on or adjacent to the cathode,

15 providing at least one nano-wire electron emitter in each pore, each electron emitter being shorter than the pore and connected to the cathode, and

providing a gate electrode on or adjacent to the insulating layer, and

providing a secondary electron emission (SEE) layer on the sidewall of each pore.

20 In an eighth specification expression of the invention there is provided a method of fabricating a field effect display comprising

providing an electron emitter array according to the method as described above, and

providing a phosphor coated screen on or spaced parallel to the electron emitter array.

BRIEF DESCRIPTION OF THE DRAWINGS

5 One or more example embodiments of the invention will now be described, with reference to the following figures, in which:

Figure 1 is a cross section of a display according to an embodiment of the invention.

Figure 2(a) is a front view of an example of the emitter array in Figure 1.

10 Figure 2(b) is a cross section of Figure 2(a).

Figure 3(a) is a cross section of an example of the screen in Figure 1.

Figure 3(b) is a cross section of an alternative example of the screen in Figure 1.

Figure 4 is a flow chart of a fabrication process according to an embodiment of the invention.

15 Figures 5(a) to 5(e) are schematics of an implementation of the fabrication process in Figure 4.

Figures 6(a) to 6(g) are schematics of an alternative implementation of the fabrication process in Figure 4.

20 DETAILED DESCRIPTION

Referring to Figure 1 a Field Emission Display (FED) 100 is shown, including an emitter array 102 and a phosphor coated screen 104 in a housing 108. The phosphor coated screen 104 is spaced parallel to the emitter array 102 by a series of spacers 106.

The accelerated electrons from the emitter array 102 collide against the phosphor coated screen 104 and fluorescent light is generated.

Referring now to Figure 2 the emitter array 102 is shown in more detail. The emitter array includes a substrate 200, an insulating layer 202, a cathode 214, electron
5 emitters 216 and a gate electrode 220.

The substrate 200 is typically rectangular in shape, and may for example be made from a sheet of glass typically 1 mm thick.

The insulating layer 202 is attached the substrate 200 by an adhesive 204, or otherwise deposited. The insulating layer 202 may be made of, for example, aluminium
10 oxide or silicon. The insulating layer 202 has a substantially uniform array of pores, each pore 206 being of sufficient depth and width to accommodate an electron emitter 216. Pore density of more than 10^5 /mm², for example 10^6 /mm², may result in good uniformity and good luminous intensity.

Each pore 206 in turn contains a base 208, side wall 210 and an opening 212.
15 The cathode 214 lies on the substrate and forms base 208 of each pore 206. The electron emitter 216 is connected to the cathode 214 at the base 208. The gate electrode 220 lies on top of the insulating layer 202.

The cathode 214 may be a series of strips which may be independently energised. Alternatively the cathode 214 may simply be a single element. Each strip 214 is typically
20 rectangular in shape and 100 nm in thickness. Each strip is provided with an external electrical connection at the edge of the substrate.

The gate electrode 220 may be a series of strips which may be independently energised. Alternatively the gate electrode 220 may simply be a single element. Each

strip is typically rectangular in cross section and 100 nm in thickness. Each strip is provided with an external electrical connection at the edge of the insulating layer. Each strip has a uniform array of apertures, where each aperture surrounds the opening 212 of a one or more pores in the insulating layer.

5 The strips of the gate electrode may for example be arranged generally perpendicularly to the strips of the cathode. This patterning of the strips to intersect perpendicularly, also known as passive matrix electrode configuration, enables the display of moving pictures. Thus the emitter array is thereby divided into independently controllable pixels at respective intersections of the strips. Each pixel may cover a
10 plurality of emitter 216. To activate each pixel the respective strip of the gate electrode is energised with a positive voltage with respect to the corresponding strip of the cathode.

Each electron emitter 216 may be made of conductive material such as metal or carbon. For example each electron emitter 216 may have a sharp point or acute tip from which a stream of electrons is emitted. Typically each electron emitter 216 does not
15 extend past the gate electrode. For example each electron emitter 216 may be shorter than the pore, such as less than half the length of the pore. Typically each electron emitter includes at least one nano-wire. In this document the term nano-wire is used to mean an elongate conductor less than 500nm in width. For example each electron emitter may include a plurality of nano-wires, such as carbon nanotubes.

20 On the side wall 210 of each pore 206 there may be a secondary electron emission (SEE) layer 218. Typically each SEE layer 218 is 50 nm in thickness and is made from, for example magnesium oxide, diamond-like carbon or amorphous carbon nitride.

Referring now to Figure 3(a) and Figure 3(b) the phosphor coated screen 104 is shown in more detail. The phosphor coated screen 104 includes a phosphor layer(s) 300, an anode(s) 302 and a glass plate 304. As seen in Figure 1 the distance between the phosphor screen 104 and the emitter array 102 is maintained by spacers 106. A cavity 110 in the housing 108, between the phosphor screen 104 the electron emitter 102 and the spacers 106, is maintained as a vacuum, for example 10^{-5} Pa.

The anode 302 may be a conductive transparent sheet-like electrode 302 between the phosphor layer 300 and the glass plate 304 as shown in Figure 3(a). Alternatively as seen in Figure 3(b) the anode 302 may be a conductive grid-like electrode 306 between the phosphor layer 300 and the cavity 110. In a further alternative the anode 302 can be coated between the phosphor layer 300 and the cavity 110. In this case, aluminium can be also utilized. The accelerated electrons penetrate the aluminium anode and collide against the phosphor layer 300. The aluminium anode between the phosphor layer 300 and the cavity 110 also acts as a reflective layer which enhances the generated light from the phosphor.

A voltage V_g is applied by variable voltage source 308 between the cathode 214 and the gate electrode 220. The voltage between the cathode 214 and the anode 302 is kept at V_a by voltage source 310.

In operation, V_g is applied between the gate electrode 220 and the cathode 214 so that the gate electrode has a positive potential and the cathode has a negative potential. The electron emitter 216 is electrically conductive so the potential of the electron emitter 216 is equal to that of the cathode. The electric field concentrates on the tip of the electron

emitter 216 and electrons are emitted from the tip of the electron emitter 216 and accelerated toward the gate electrode 220.

Where an SEE layer 218 is provided, in the course of travelling through the pore 206, some electrons may bump against the SEE layer 218 which generates further electron emission. The generated electrons may also bump against the SEE layer 218, generating
5 still further electrons. Thus emitted electrons originally from the electron emitter are multiplied by the SEE layer 218 and travel toward the gate electrode 220.

The electrons are accelerated through the pore 206 and are emitted from the opening 212. The phosphor coated screen 104 is energised at a higher potential than the
10 gate electrode. The accelerated electrons collide against the phosphor and fluorescent light is generated.

By controlling the voltage V_g , the energy and / or density of the electron stream, and therefore the intensity of the fluorescent light, can be adjusted. This may be in terms of the average brightness of the display, or brightness of specific emitters or pixels as
15 required in display of dynamic images.

Method of fabrication

Referring to Figure 4 a method 400 of fabricating an emitter array for a display is shown. In step 402 a cathode is provided. In step 404 an insulating layer is provided
20 including an array of pores. In step 406 a SEE layer may be provided on the sidewall of each pore. In step 408 at least one electron emitter is provided within each pore. In step 410 a gate electrode is provided. One skilled in the art will appreciate the order listed is for example only, and that the method 400 could be implemented in other orders.

Figure 5 illustrates one implementation of the method 400.

Step 402 may be implemented by depositing cathodes 214 made of tungsten, molybdenum or other suitable material onto a rigid substrate 200, as seen in Figure 5(a).

A catalyst layer 500 is deposited on top of the cathodes 214. Nickel, copper, iron
5 or cobalt can be used for the catalyst layer 500.

Step 404 may be implemented by bonding the insulating layer 202 using adhesive 204 on top of the substrate 200, seen in Figure 5(b).

A sheet of anodized aluminium oxide (AAO), is suitable for the insulating layer 202. AAO is formed by anodising an aluminium sheet in acid. Pores 206 are generated
10 and a self-assembled lattice and honeycomb-like AAO porous sheet 502 is obtained. This process avoids the numerous steps involved in using photolithographic techniques to form pores. Furthermore, pore density greater than $10^6/\text{mm}^2$ (which is impossible by photolithography) can be obtained. Pore density may be controlled by varying the anodising conditions for the aluminium sheet. For example, conditions including the
15 concentration of the acid, applied voltage, temperature and surface roughness of the aluminium sheet, all affect the pore density.

Step 406 may be implemented by depositing a SEE layer 218 on the sidewall 210 of the pore, shown in Figure 5(c). Magnesium oxide, diamond-like carbon, and amorphous carbon nitride, for example, may be used for the SEE layer. The SEE layer
20 may be deposited by vacuum evaporation, sputtering or chemical vapour deposition.

Step 408 may be implemented by processing the AAO plate 502 bonded on the substrate 200 by Chemical Vapour Deposition (CVD) in order to produce Carbon Nano-Tubes (CNT) 504 at the base 208 of each pore 206. By controlling a flow of

methane gas in plasma toward the plate 202, a number of CNT 504 grow in each pore 206 from the catalyst layer 500, shown in Figure 5(d). The CNT provide an apex to concentrate the electric field and emit electrons.

Step 410 may be implemented by depositing the gate electrode 220 on top of the plate 502, shown in Figure 5(e).

Figure 6 illustrates an alternative implementation of the method 400.

Step 402 may be implemented by depositing cathodes 214 made of tungsten or molybdenum onto a rigid substrate 200, seen in Figure 6(a)

Step 404 may be implemented by bonding a silicon wafer 600 on top of the cathodes by using an adhesive layer 204. Pores 602 are patterned in the silicon wafer 600 using photolithography, as shown in Figure 6(b).

Step 406 may be implemented by depositing the SEE layer 218 on the sidewall 210 of the pore, as seen in Figure 6(c). Magnesium oxide, diamond-like carbon, amorphous carbon nitride or other appropriate material is used for the SEE layer. The SEE layer may be deposited by vacuum evaporation, sputtering or chemical vapour deposition.

In this example step 410 precedes step 408.

Step 410 may be implemented by depositing gate electrode 220 on top of the wafer 600, as shown in Figure 6(d).

Step 408 may be implemented by deposition of a sacrificial layer 604 onto the gate electrodes 220, seen in Figure 6(e). This is followed by depositing a layer of tungsten, molybdenum or other material 606 onto the sacrificial layer 604. The aperture 608 of the pore 610 is gradually capped with the deposited material, which results in a cone 612

forming at the base of the in the pore, as shown in Figure 6(f). The sacrificial layer 604, together with deposits above the sacrificial layer, are then dissolved with acid or solvent, leaving the cones 612 and the gate electrodes 220, seen in Figure 6(g).

The emitter array, fabricated according to the above, may then be installed into a housing, together with the spacers, anode and screen. Control electronics are provided to energise the cathode, gate electrode and anode according to an input signal and/or stored instructions. Thus each electron emitter can be selectively energised, and the energisation varied to achieve the desired display. A skilled reader will also readily appreciate other applications for one or more embodiments, such as in a Scanning Electron Microscope, a Back-light of Liquid Crystal Display or a Stepper for semiconductor production.

Where AAO is used as the insulating layer, a pore density greater than $10^6/\text{mm}^2$ (which is impossible by photolithography) may be achievable. This density provides good uniformity and luminous intensity as well as good response speed.

Where a SEE material is used on the sidewall of the pore, emitter current can be reduced and therefore the lifetime of the emitter may be improved.

Where nano-wire electron emitters are used, a low emission threshold voltage and good durability may be achieved.

CLAIMS:

1. A field effect electron emitting apparatus comprising
a cathode,
an insulating layer on or adjacent to the cathode having an array of pores,
5 at least one nano-wire electron emitter within each pore, each nano-wire electron
emitter being shorter than the pore and connected to the cathode, and
a gate electrode on or adjacent to the insulating layer.
2. A field effect electron emitting apparatus comprising
a cathode,
10 an insulating layer on or adjacent to the cathode having an array of pores,
a plurality of nano-wire electron emitters in each pore connected to the cathode,
a gate electrode on or adjacent to the insulating layer.
3. A field effect electron emitting apparatus comprising
a cathode,
15 an insulating layer on or adjacent to the cathode having an array of pores,
at least one electron emitter within each pore, each electron emitter being shorter
than the pore and connected to the cathode,
a gate electrode on or adjacent to the insulating layer, and
a secondary electron emission (SEE) layer on the sidewall of each pore.
- 20 4. The electron emitting apparatus as claimed in any of the preceding claims wherein
each nano-wire is a carbon nano-tube (CNT).
5. The electron emitting apparatus as claimed in any of the preceding claims wherein
the insulating layer has a pore density greater than $10^6/\text{mm}^2$.

6. The electron emitting apparatus as claimed in any of the preceding claims wherein the insulating layer is anodised aluminium oxide (AAO).
7. The electron emitting apparatus as claimed in any one of claims 1 to 4 wherein the insulating layer is silicon.
- 5 8. The electron emitting apparatus as claimed in claim 3 wherein the SEE layer is selected from the group of magnesium oxide, diamond-like carbon and amorphous carbon nitride.
9. The electron emitting apparatus display as claimed in any of the preceding claims wherein each nano-wire electron emitter is less than half the length of the corresponding
10 pore.
10. A field effect display comprising
 - a field effect electron emitting apparatus as claimed in any of claims 1 to 9, and
 - a phosphor coated screen on or spaced parallel to the field effect electron emitting apparatus.
- 15 11. The display as claimed in claim 10 wherein the display is divided into independently controllable pixels, and each pixel including a plurality of nano-wire electron emitters.
12. The display as claimed in claim 10 or 11 further comprising an anode on or adjacent to the phosphor coated screen.
- 20 13. A method of fabricating an electron emitter array comprising:
 - providing a cathode,
 - providing a insulating layer including an array of pores on or adjacent to the cathode,

providing at least one nano-wire electron emitter within each pore, each nano-wire electron emitter being shorter than the pore and connected to the cathode, and

providing a gate electrode on or adjacent to the insulating layer.

14. A method of fabricating a electron emitter array comprising:

5 providing a cathode,

providing a insulating layer including an array of pores on or adjacent to the cathode,

providing a plurality of nano-wire electron emitters in each pore connected to the cathode, and

10 providing a gate electrode on or adjacent to the insulating layer.

15. A method of fabricating a electron emitter array comprising

providing a cathode,

providing a insulating layer including an array of pores on or adjacent to the cathode,

15 providing at least one nano-wire electron emitter in each pore, each electron emitter being shorter than the pore and connected to the cathode, and

providing a gate electrode on or adjacent to the insulating layer, and

providing a secondary electron emission (SEE) layer on the sidewall of each pore.

20 16. The method as claimed in any one of claims 13 to 15 wherein each nano-wire electron emitter is a carbon nano-tube (CNT).

17. The method as claimed in any one of claims 13 to 16 further comprising anodising an aluminium sheet in acid to form anodised aluminium oxide (AAO) as the insulating layer.
18. The method as claimed in claim 17 wherein the anodising conditions are selected
5 to achieve pore density greater than $10^6/\text{mm}^2$.
19. The method as claimed in any one of claims 13 to 16 further comprising depositing a layer of silicon and etching an array of pores in the layer of silicon to form the insulating layer.
20. The method as claimed in claim 14 wherein the SEE layer is selected from the
10 group of magnesium oxide, diamond-like carbon and amorphous carbon nitride.
21. The method as claimed in claim 16 wherein providing the nano-wire electron emitter comprises using Chemical Vapour Deposition (CVD) to grow at least one Carbon Nano-Tube (CNT) within each pore, from a catalyst at the base of each pore.
22. The method as claimed in any of claims 13 to 21 wherein each nano-wire electron
15 emitter is less than half the length of the corresponding pore.
23. A method of fabricating a field effect display comprising
providing an electron emitter array according to the method as claimed in any of
claims 13 to 22, and
providing a phosphor coated screen on or spaced parallel to the electron emitter
20 array.
24. The method as claimed in claim 23 wherein the emitter array is divided into independently controllable pixels, and each pixel including a plurality of emitters.

25. The method as claimed in claim 23 or 24 further comprising providing an anode on or adjacent to the phosphor coated screen.