

FORMATION OF SEMICONDUCTOR LAYER / FORMATION OF INSULATING FILM /
FORMATION OF FIRST CONDUCTIVE FILM AND SECOND CONDUCTIVE FILM

Fig. 1A

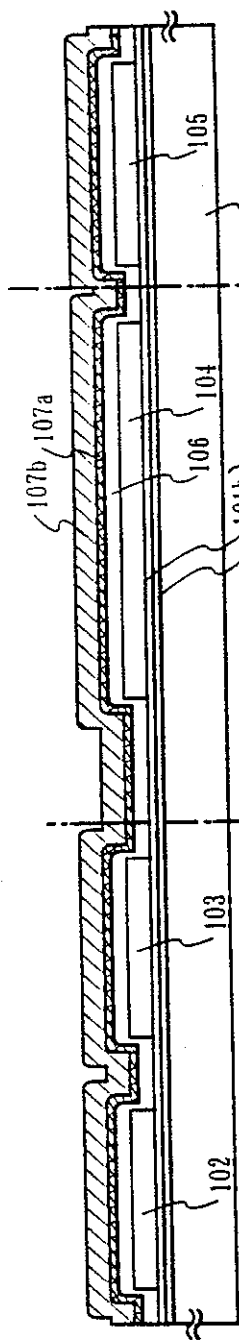


Fig. 1B FIRST ETCHING PROCESSING

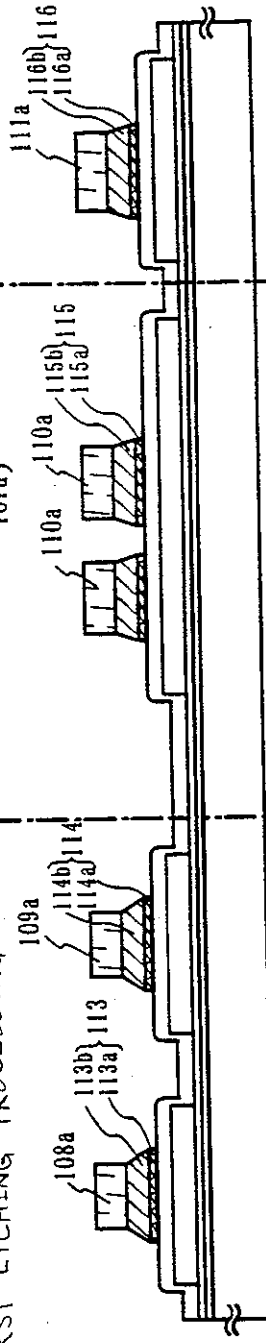


Fig. 1C FIRST DOPING PROCESSING

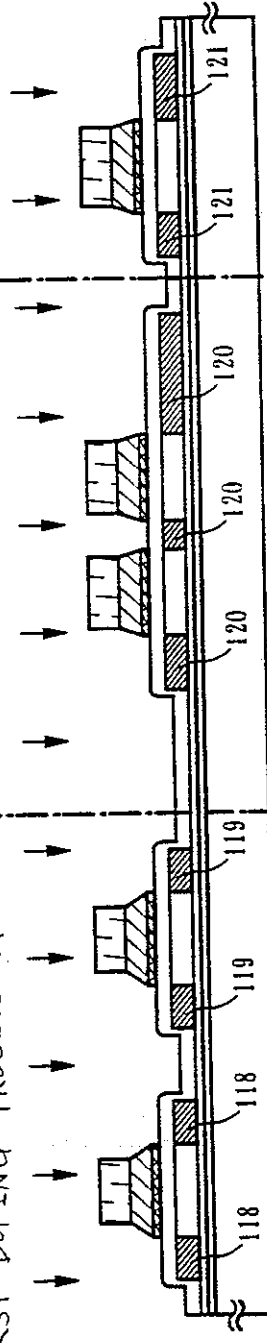
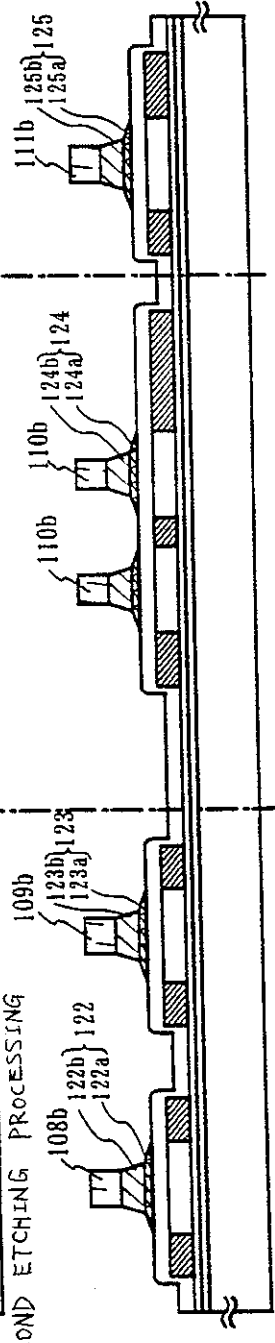


Fig. 1D SECOND ETCHING PROCESSING



2/14

Fig. 2A SECOND DOPING PROCESSING

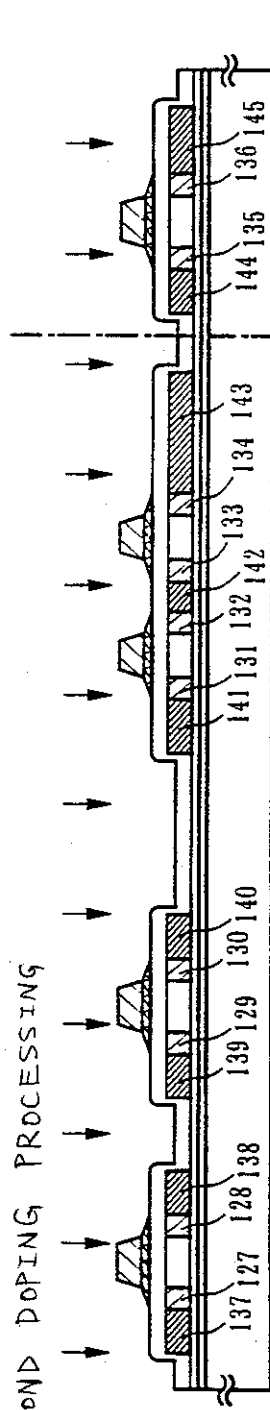
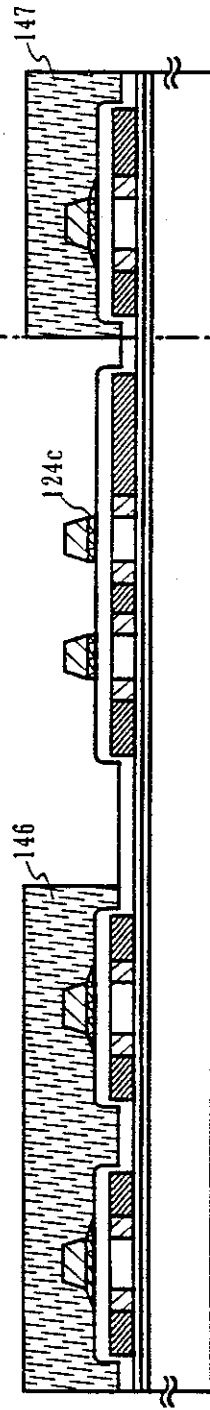
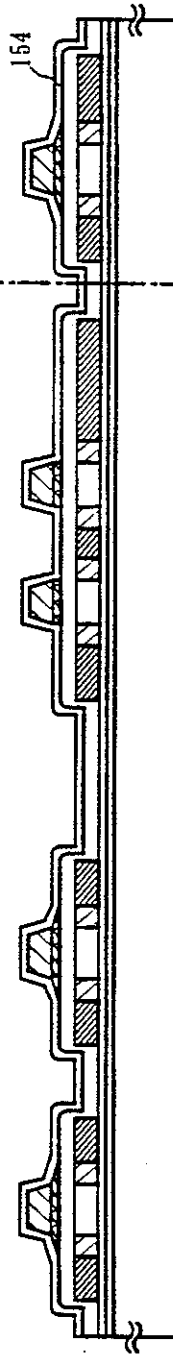


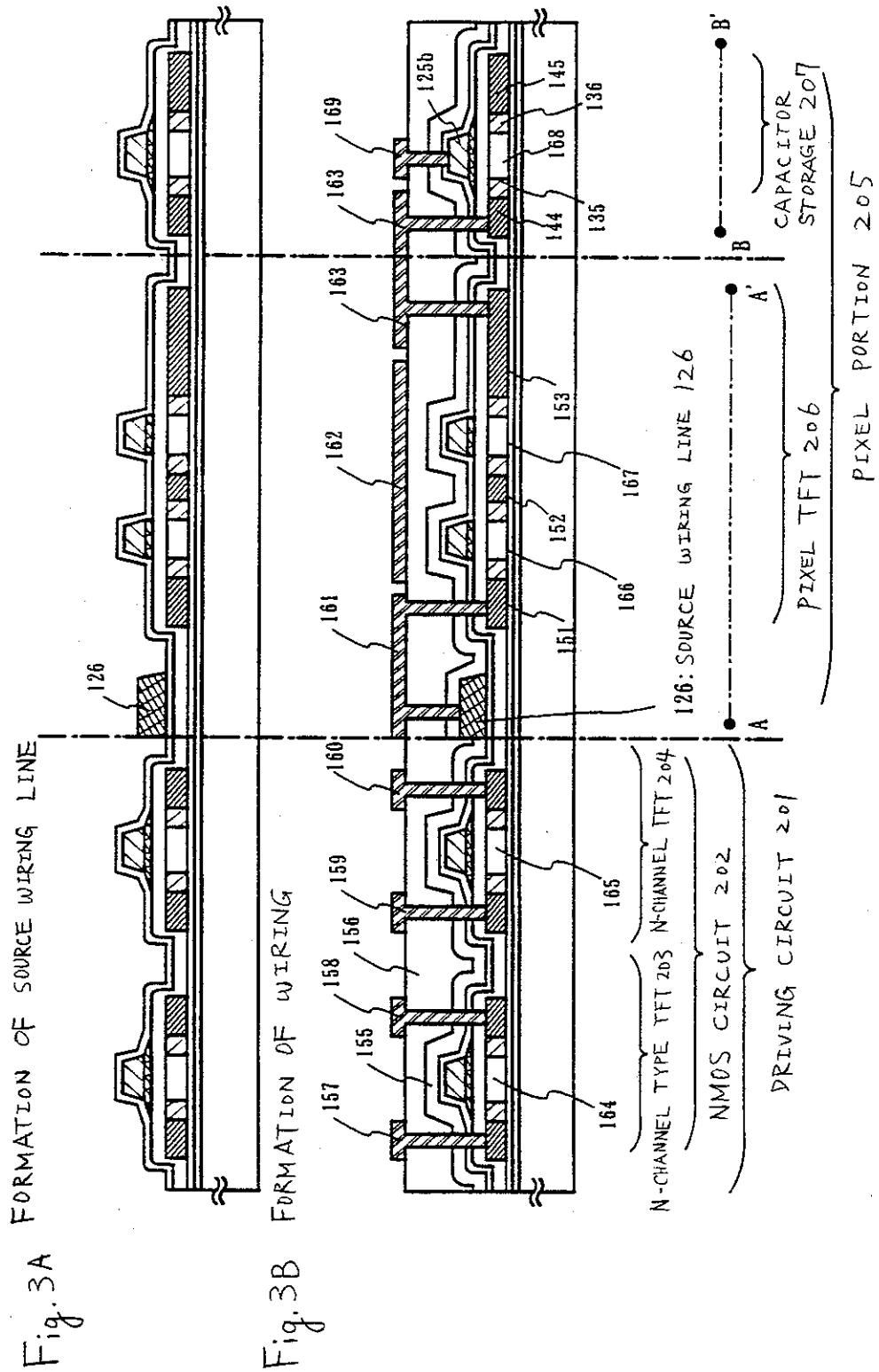
Fig. 2B THIRD ETCHING TREATMENT



FORMATION OF FIRST INTERLAYER INSULATING FILM / ACTIVATION

Fig. 2C





4/14

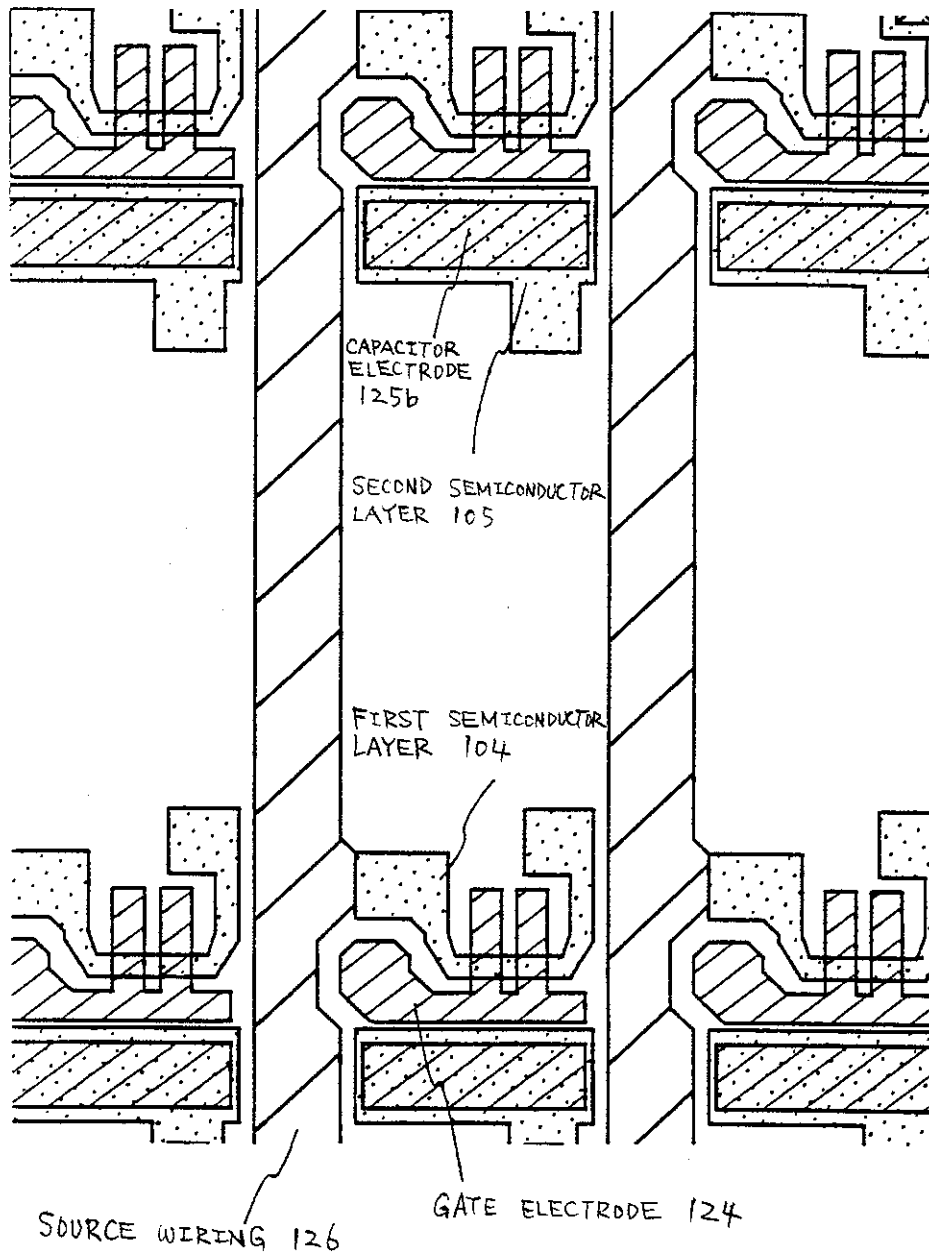


Fig. 4

5/14

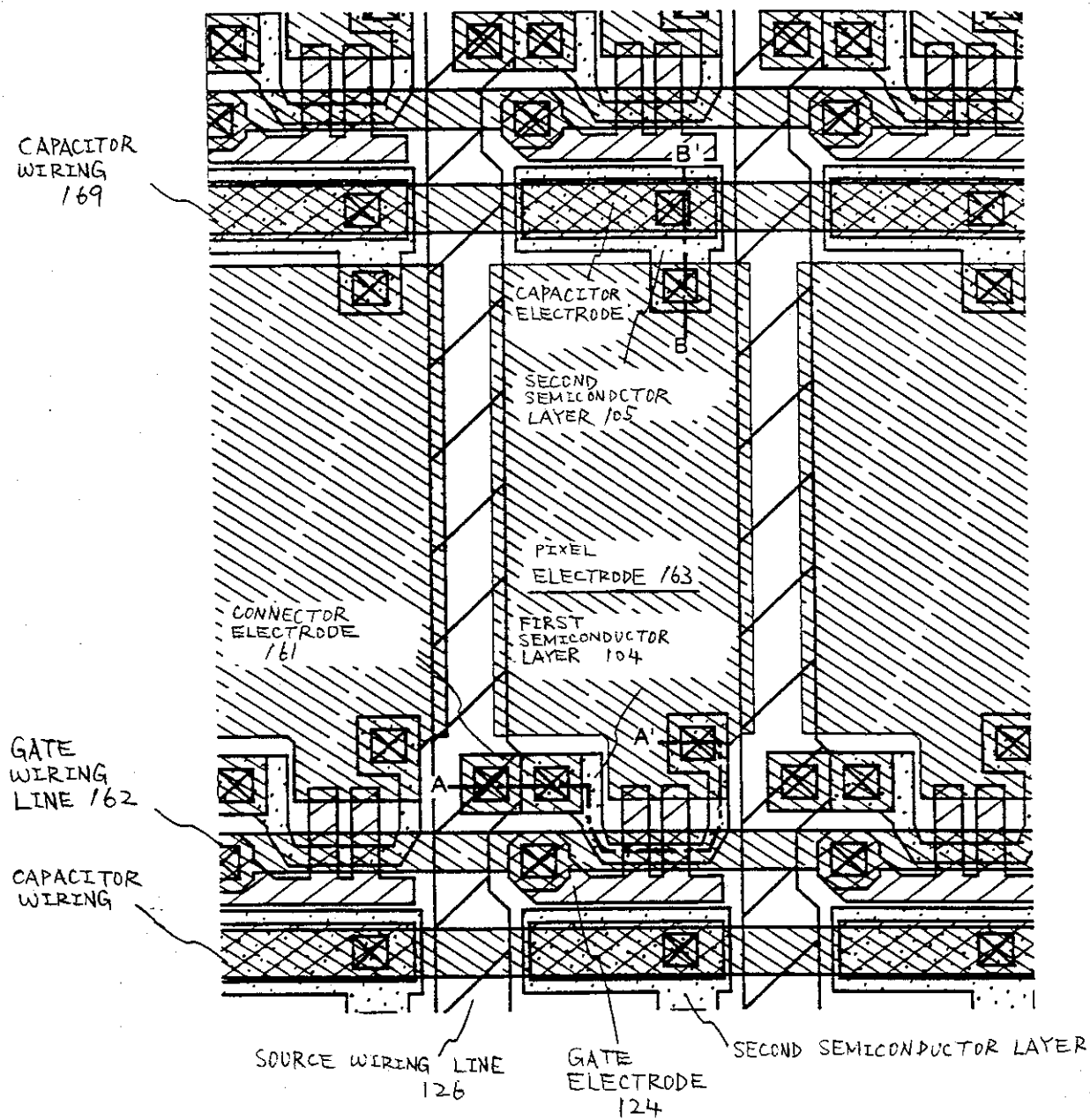


Fig. 5

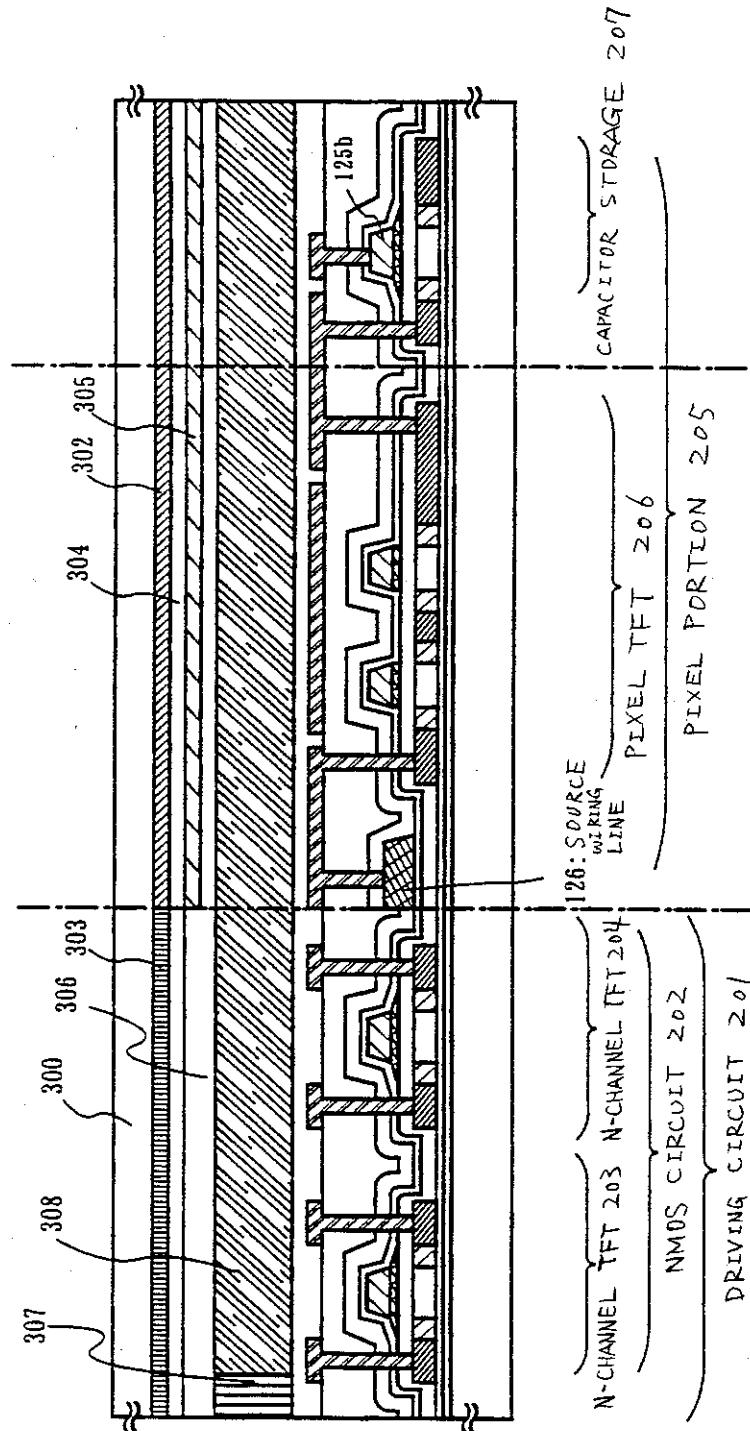
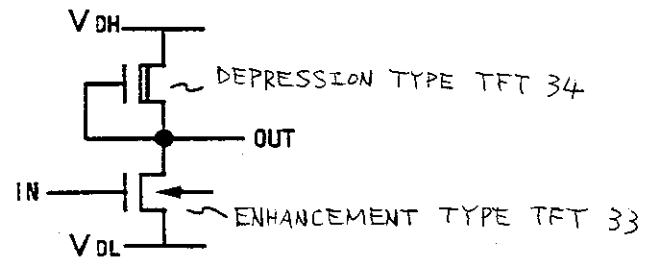
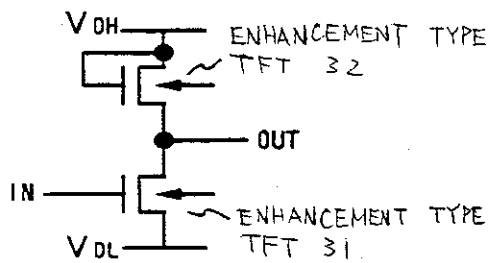
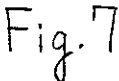


Fig. 6



8/14

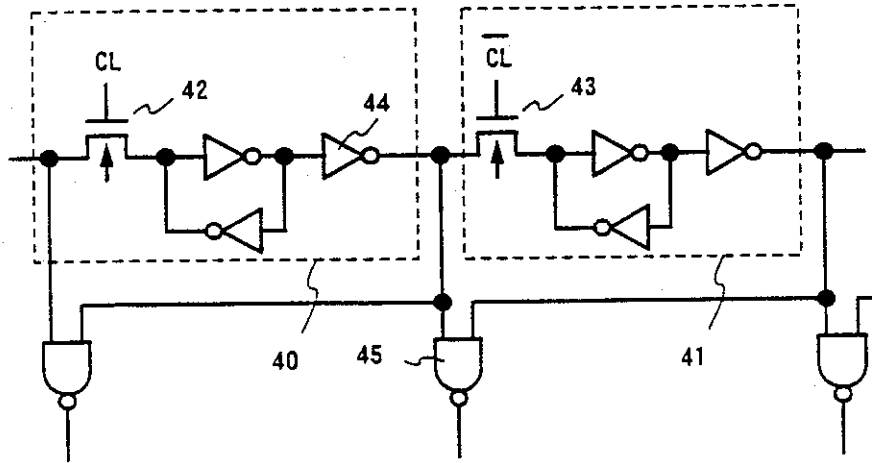


Fig. 9A

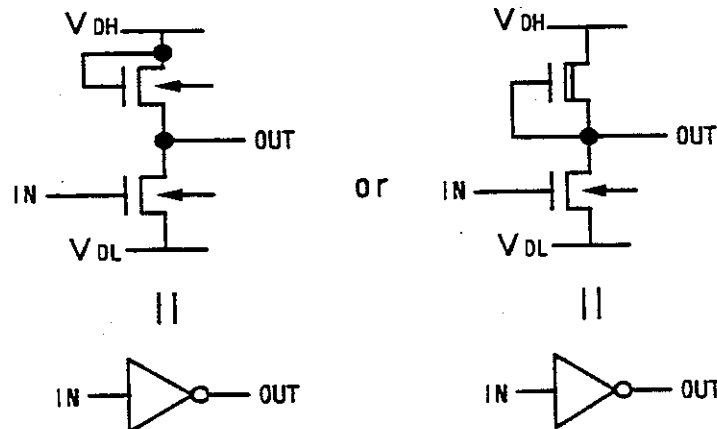


Fig. 9B

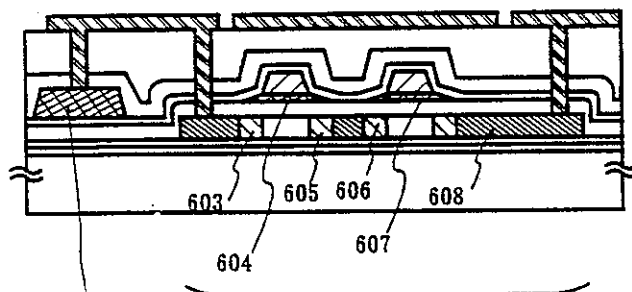
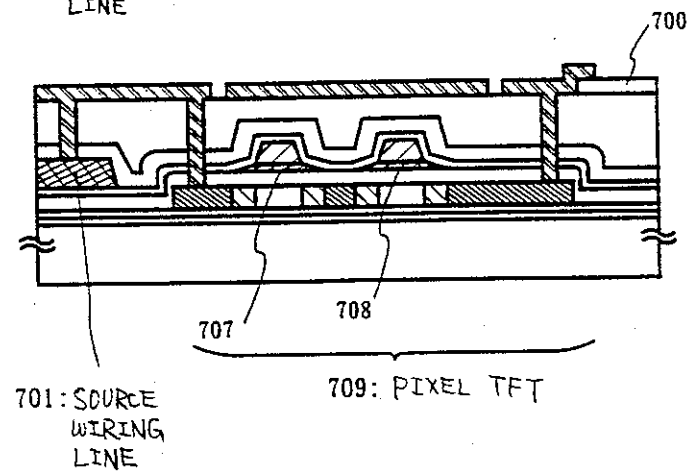
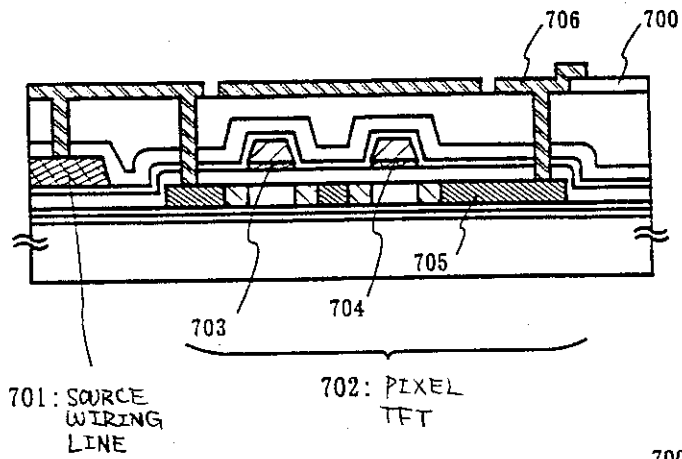


Fig. 10

601: SOURCE
WIRING
LINE

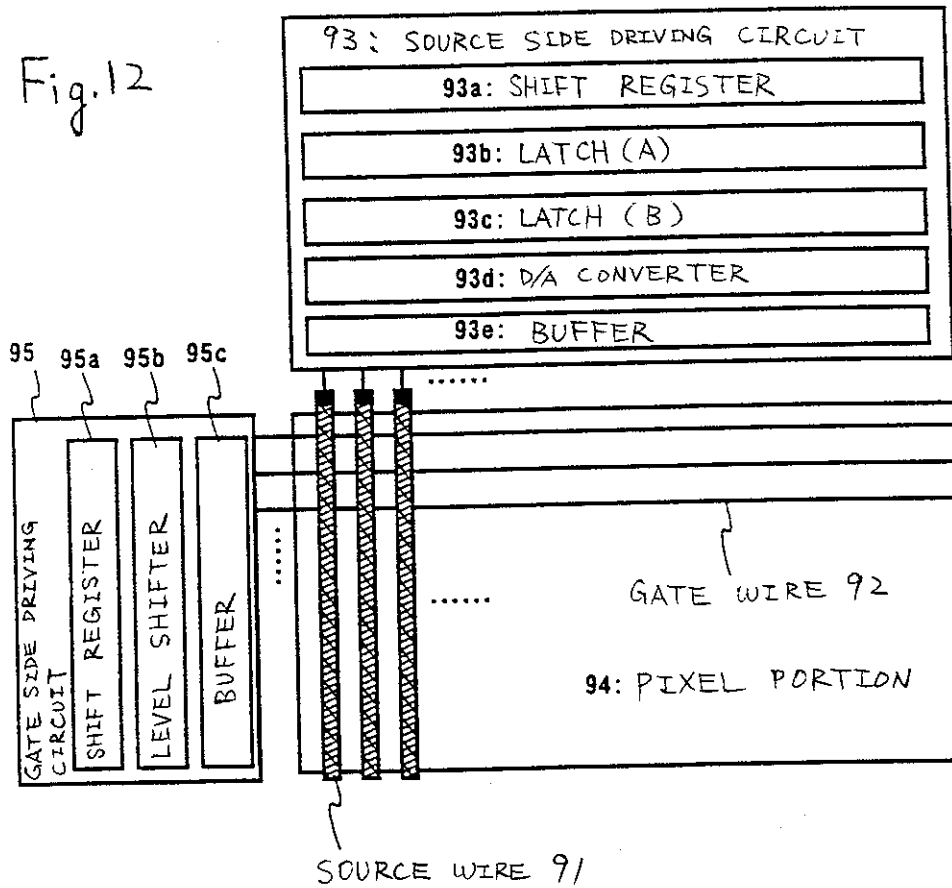
602: PIXEL TFT

9/14



10/14

Fig. 12



11/14

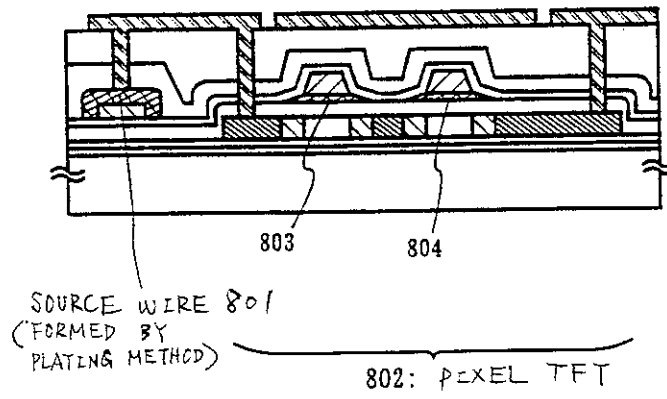


Fig. 13A

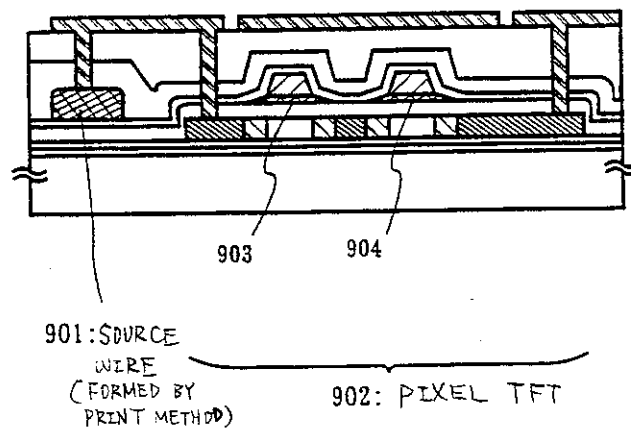


Fig. 13B

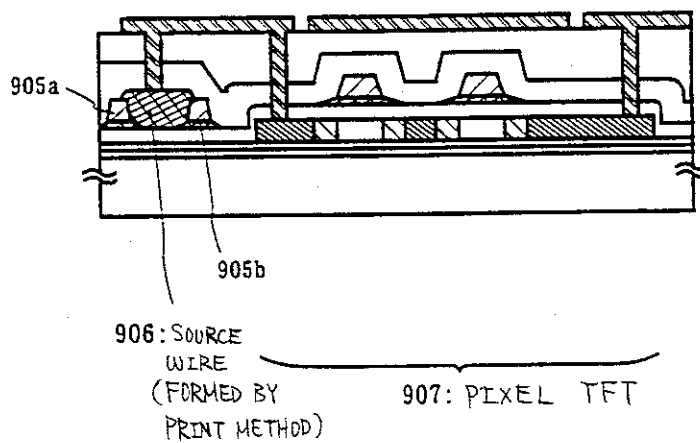


Fig. 13C

12/14

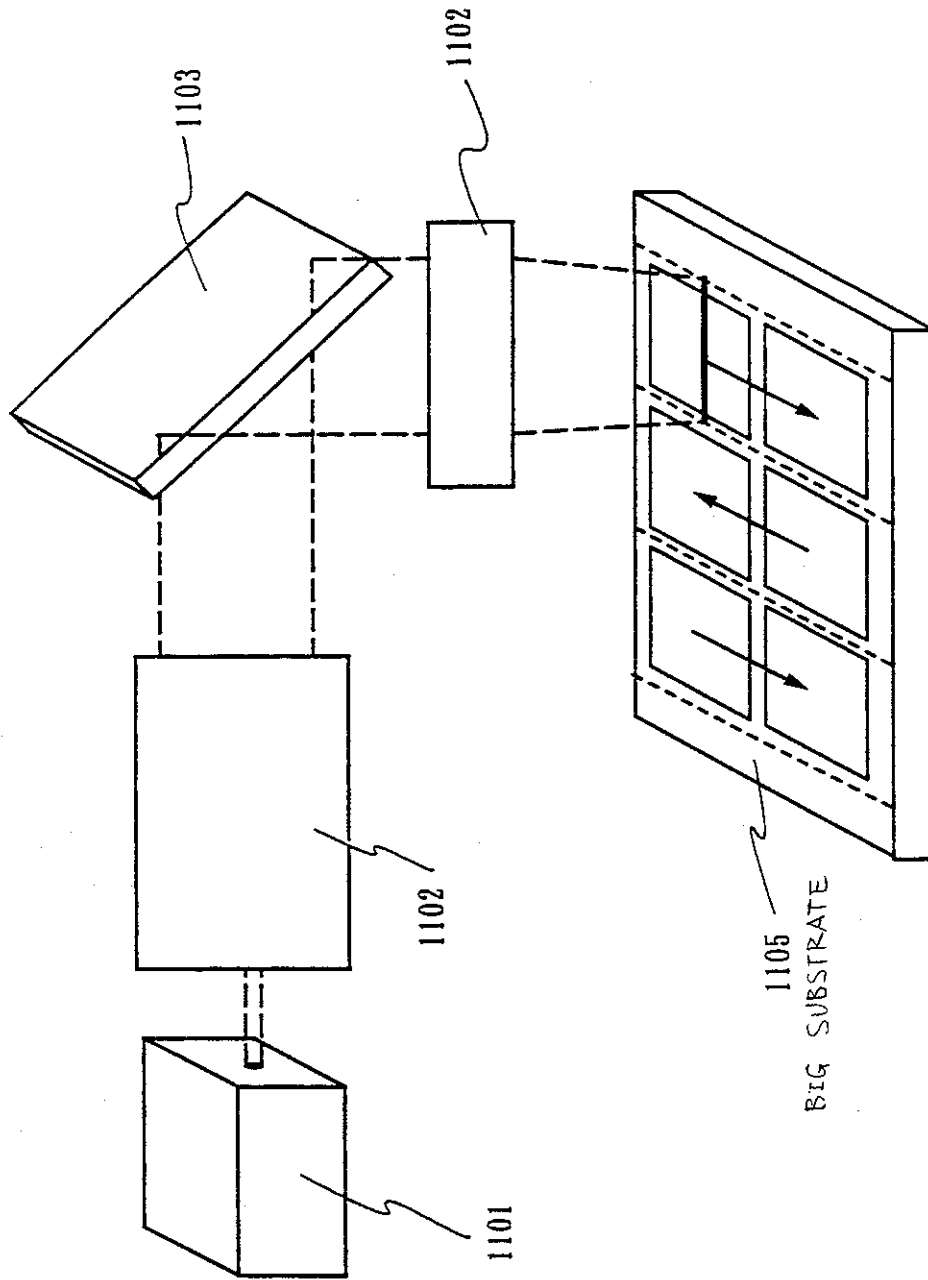


Fig. 14

13/14

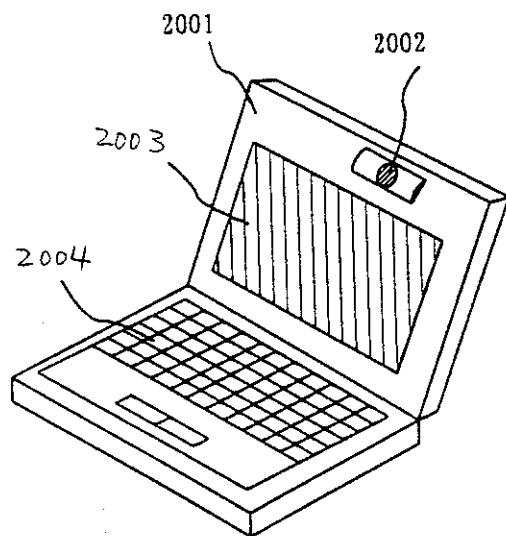


Fig. 15A

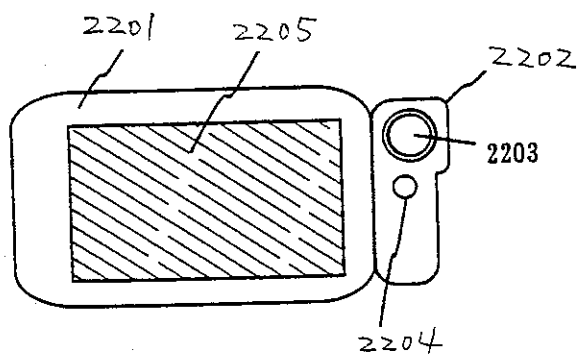


Fig. 15B

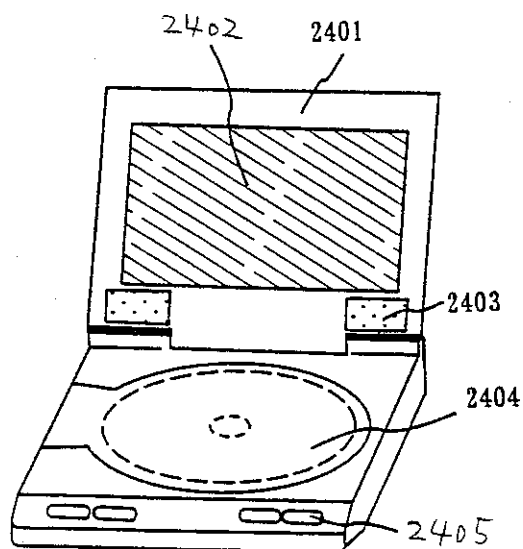


Fig. 15C

14/14

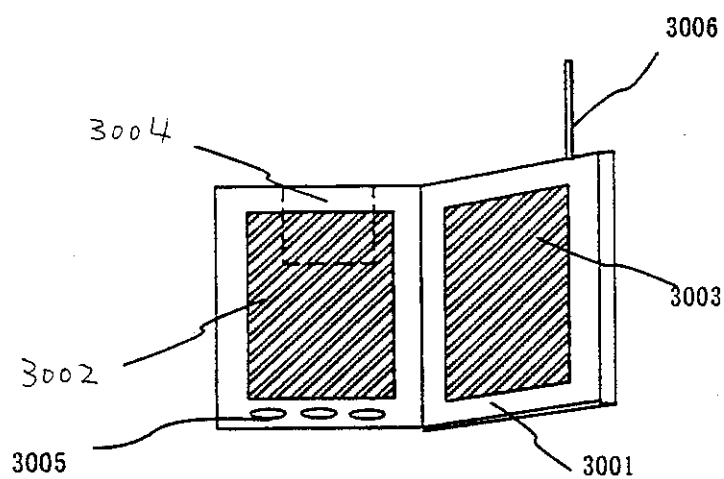


Fig. 16A

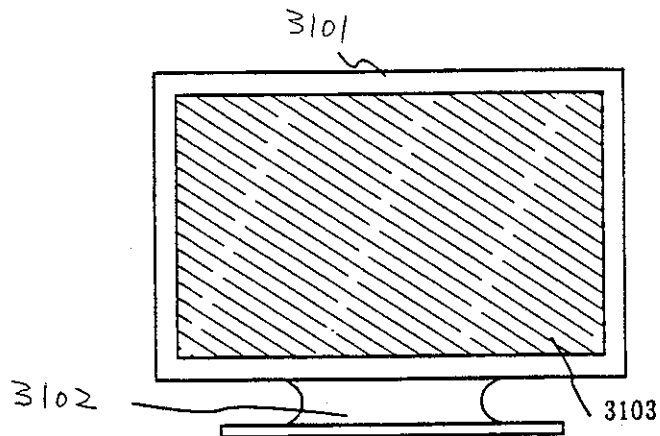


Fig. 16B