

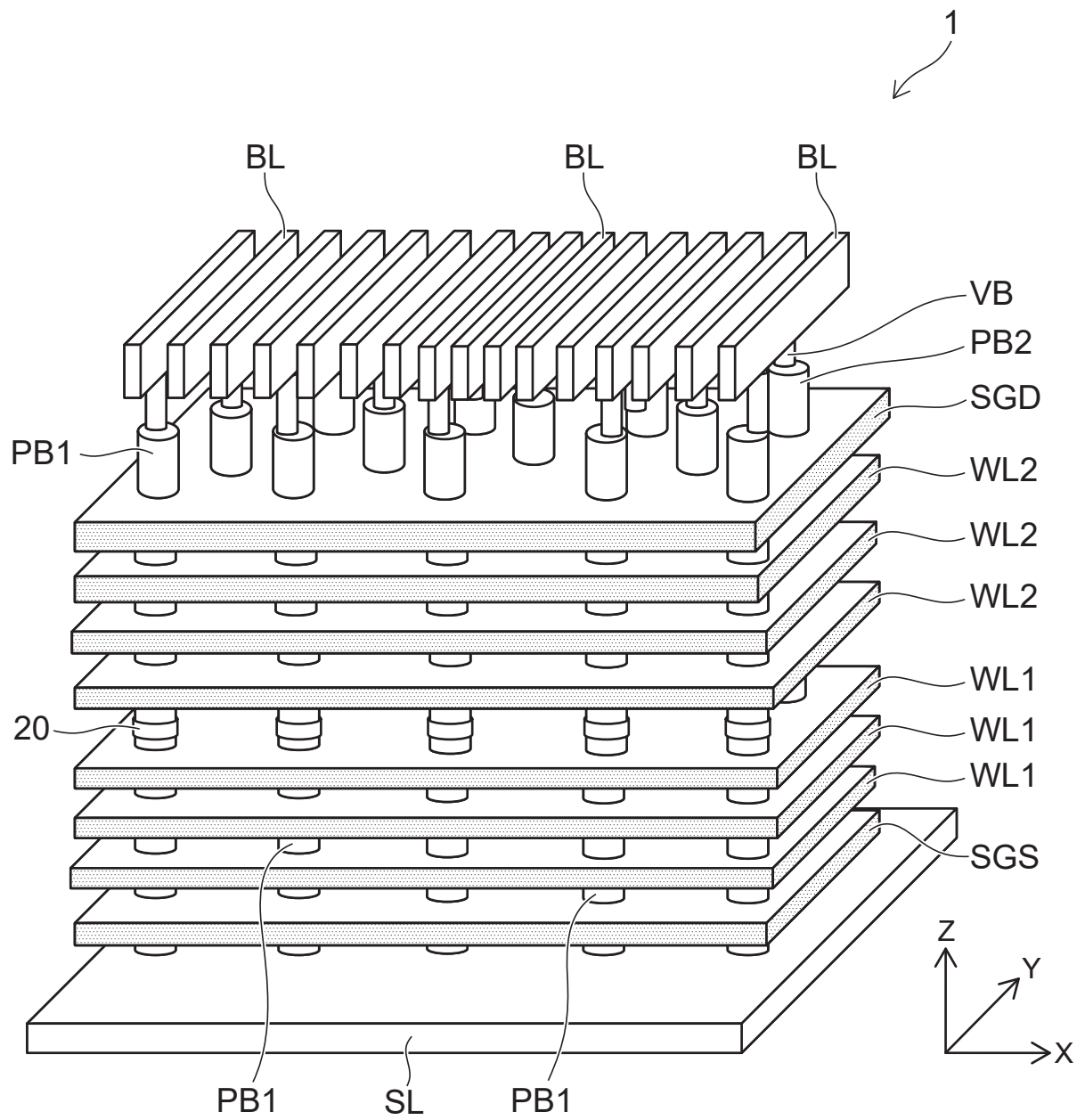


FIG. 1

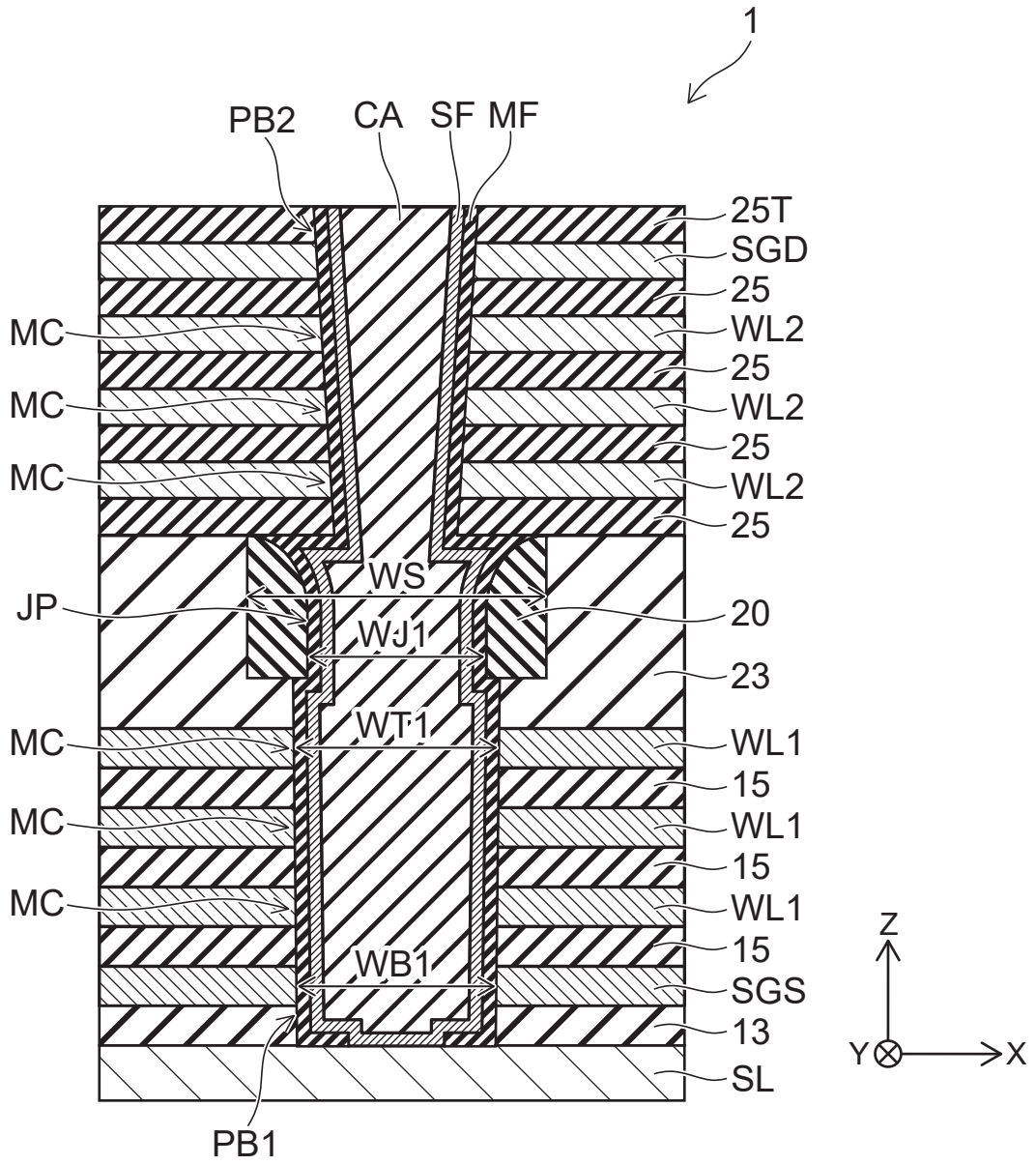


FIG. 2

3/28

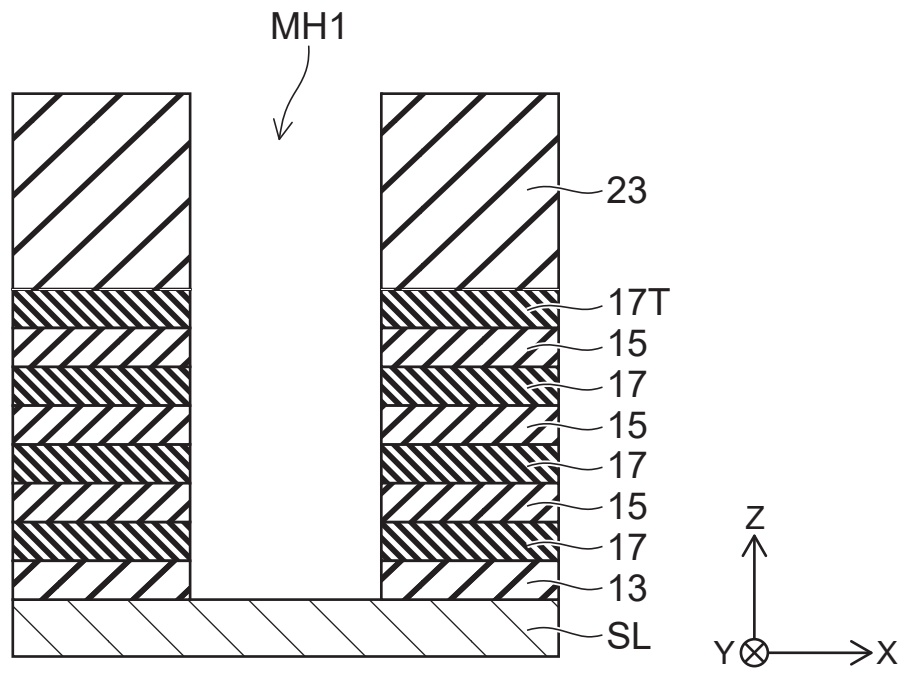


FIG. 3A

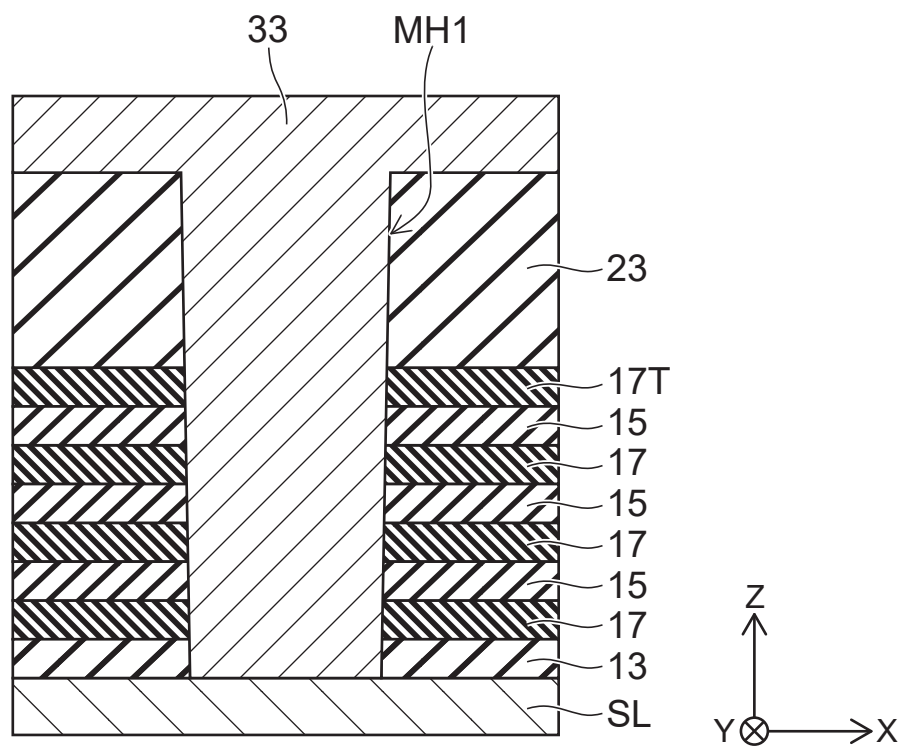


FIG. 3B

4/28

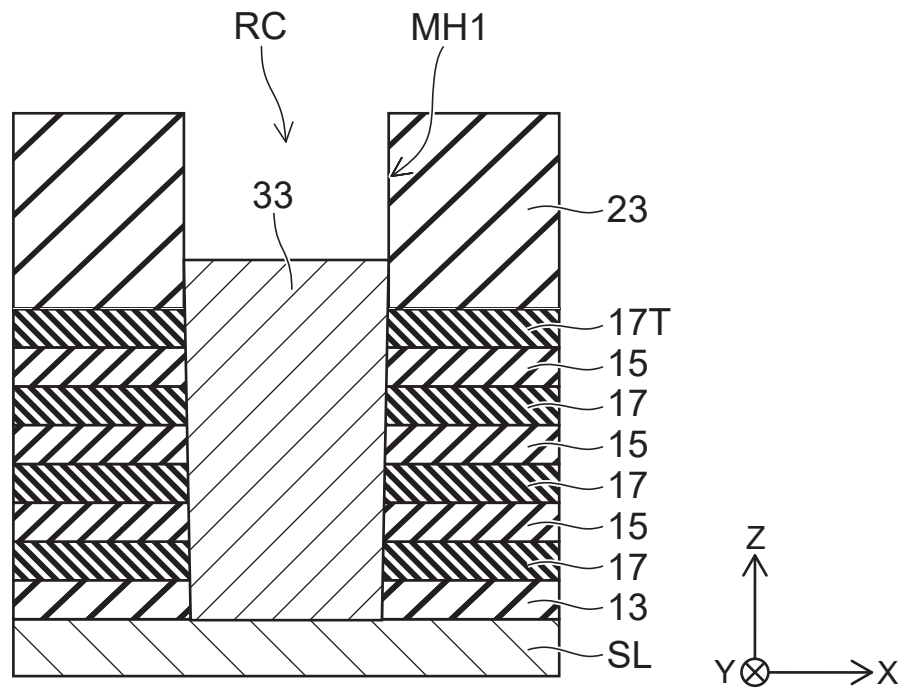


FIG. 4A

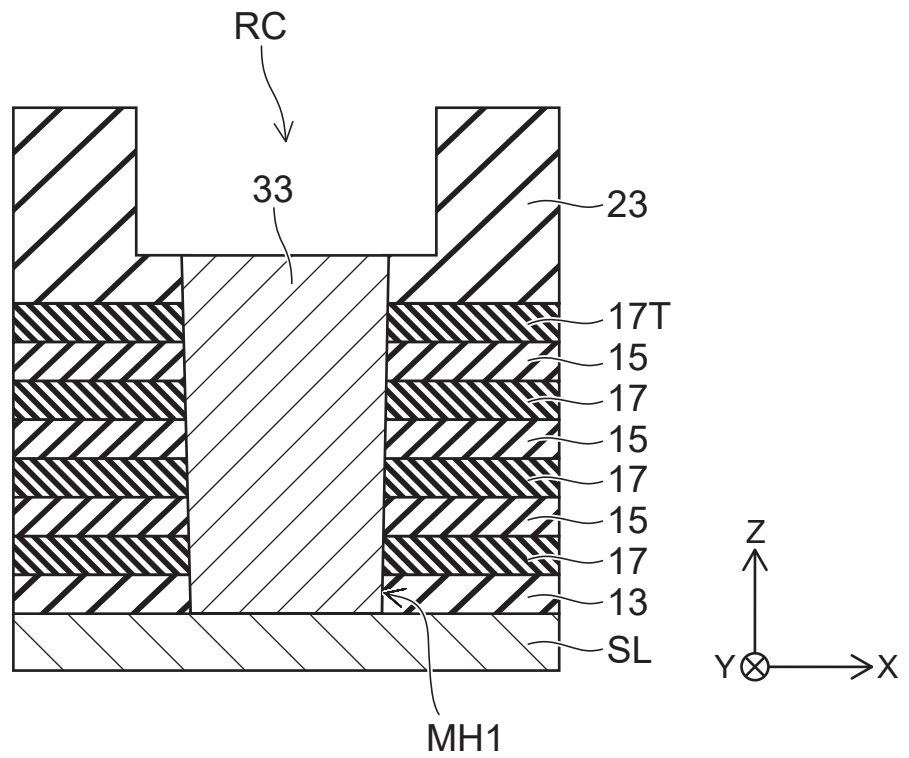


FIG. 4B



6/28

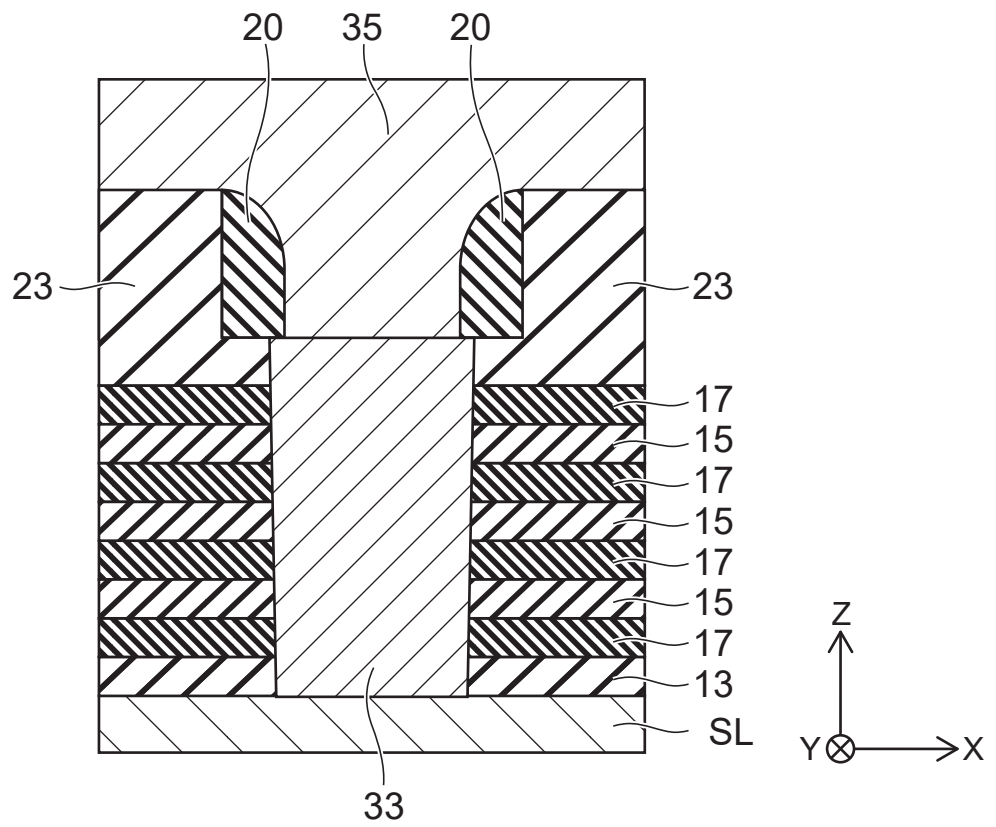


FIG. 6A

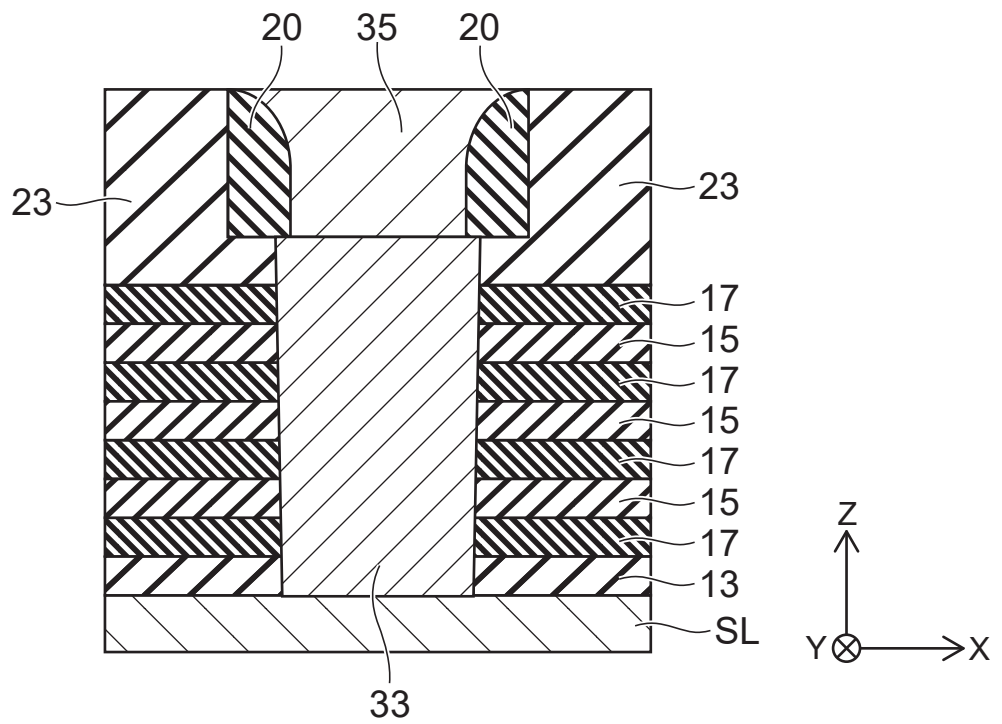


FIG. 6B

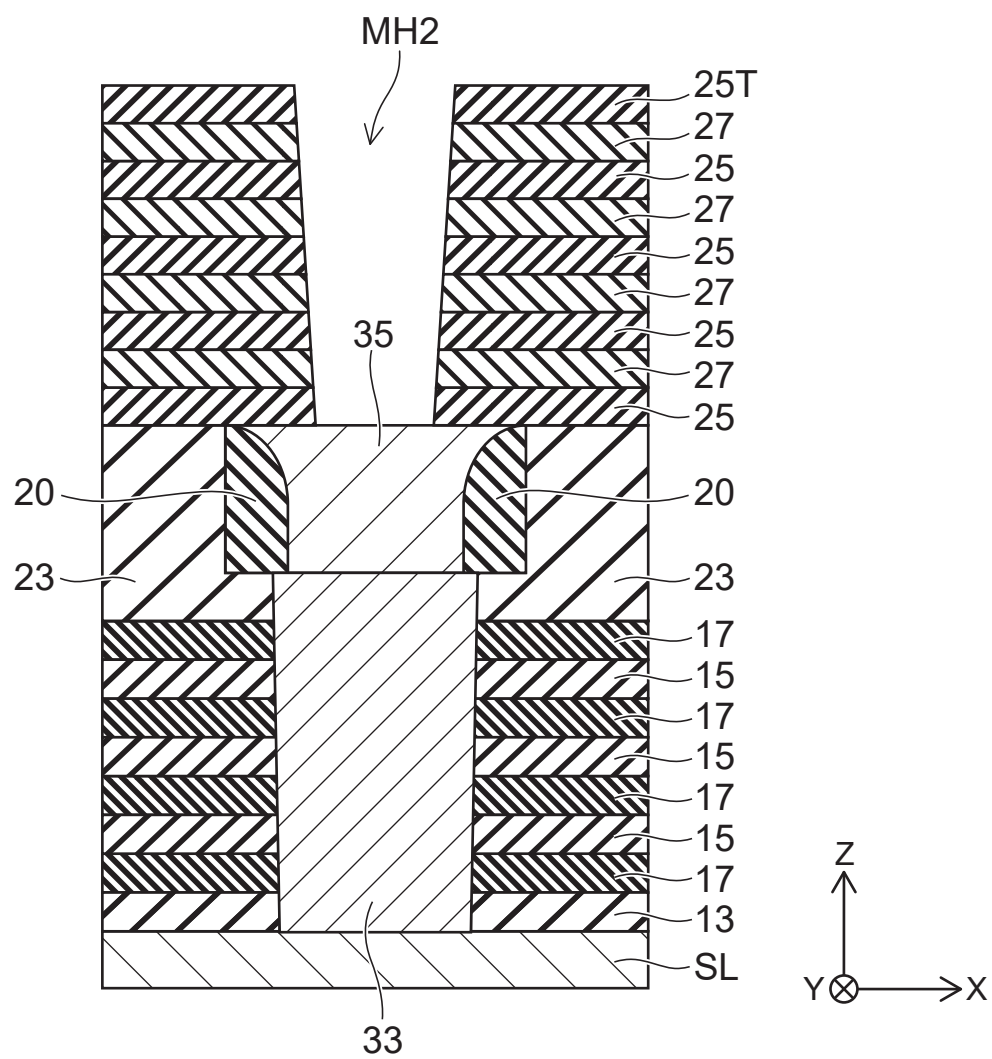


FIG. 7

8/28

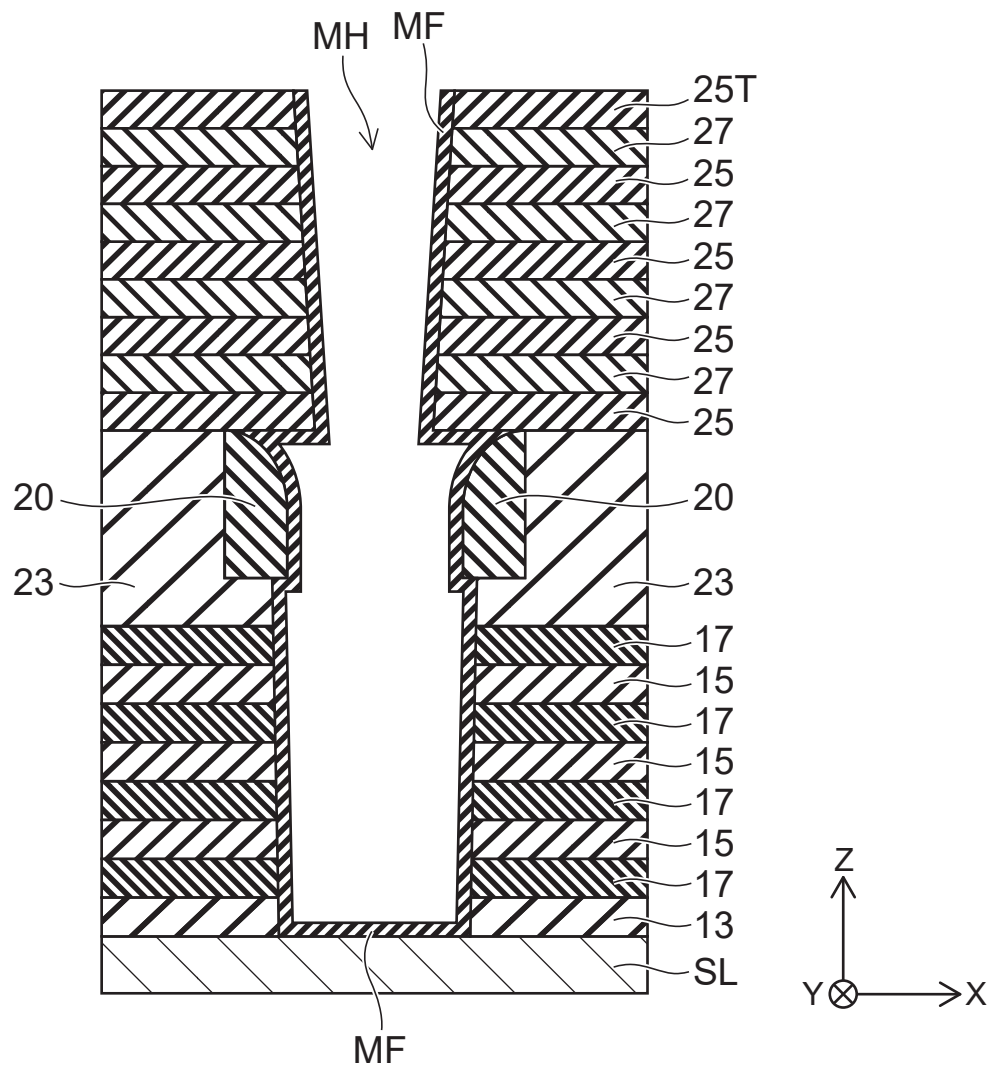


FIG. 8A

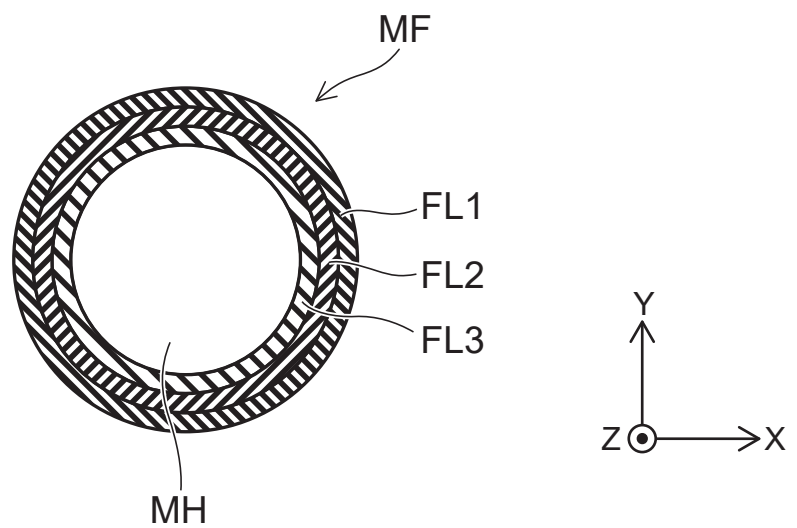


FIG. 8B

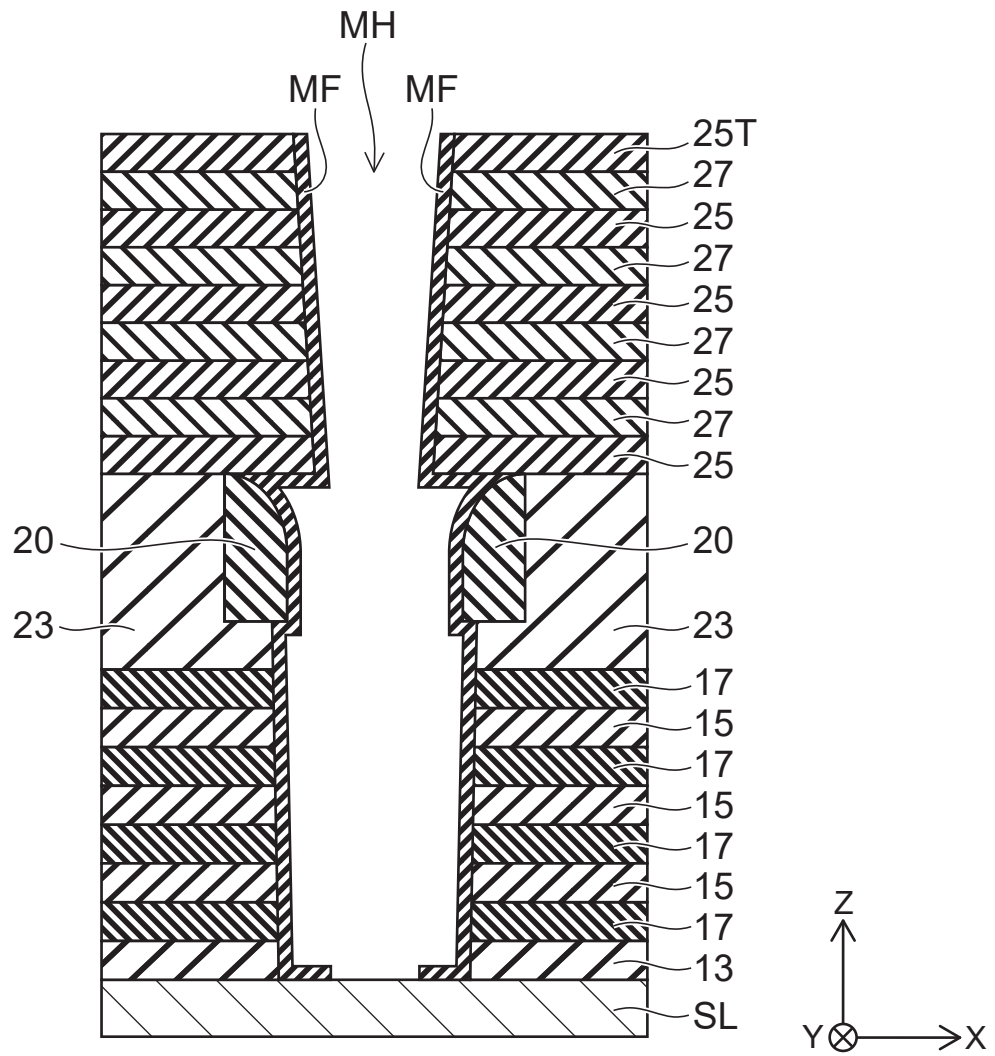


FIG. 9

10/28

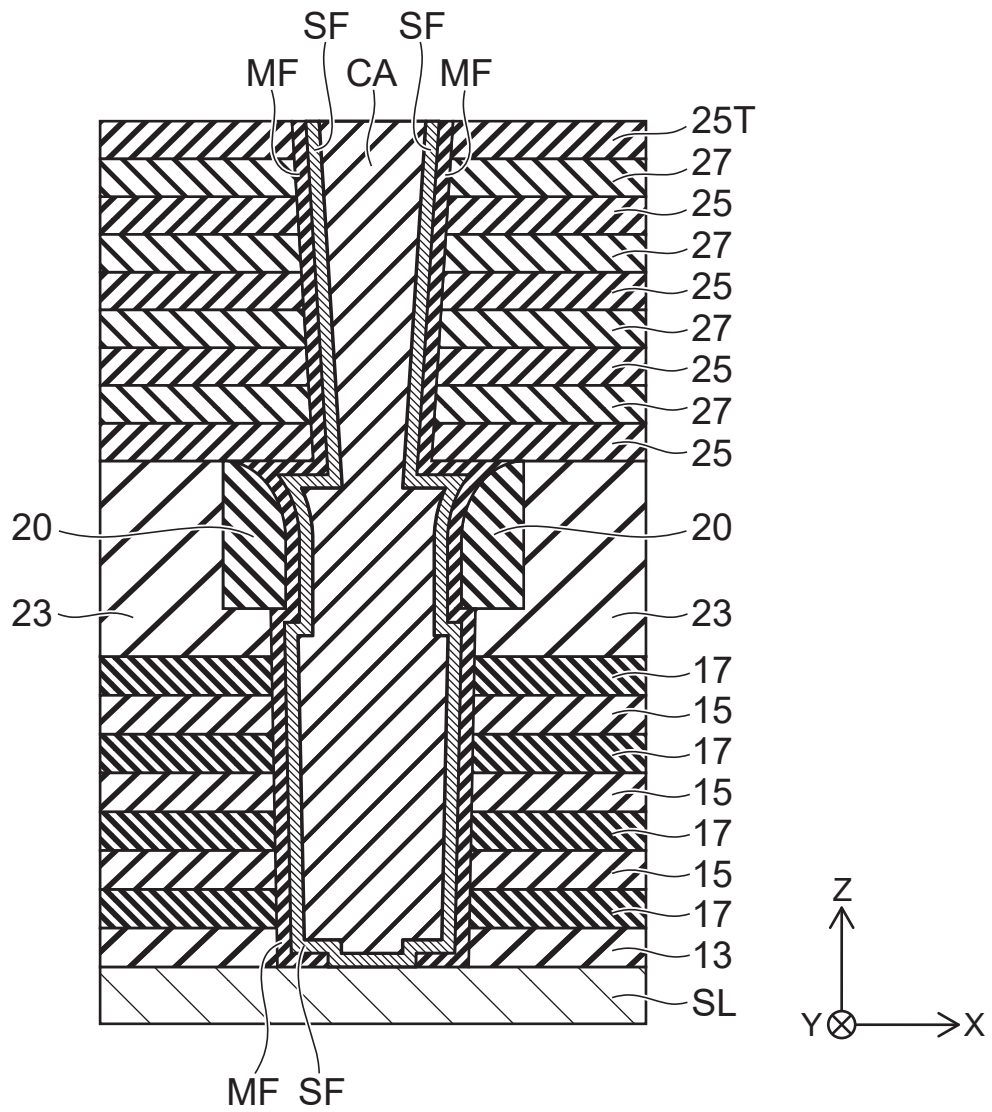


FIG. 10

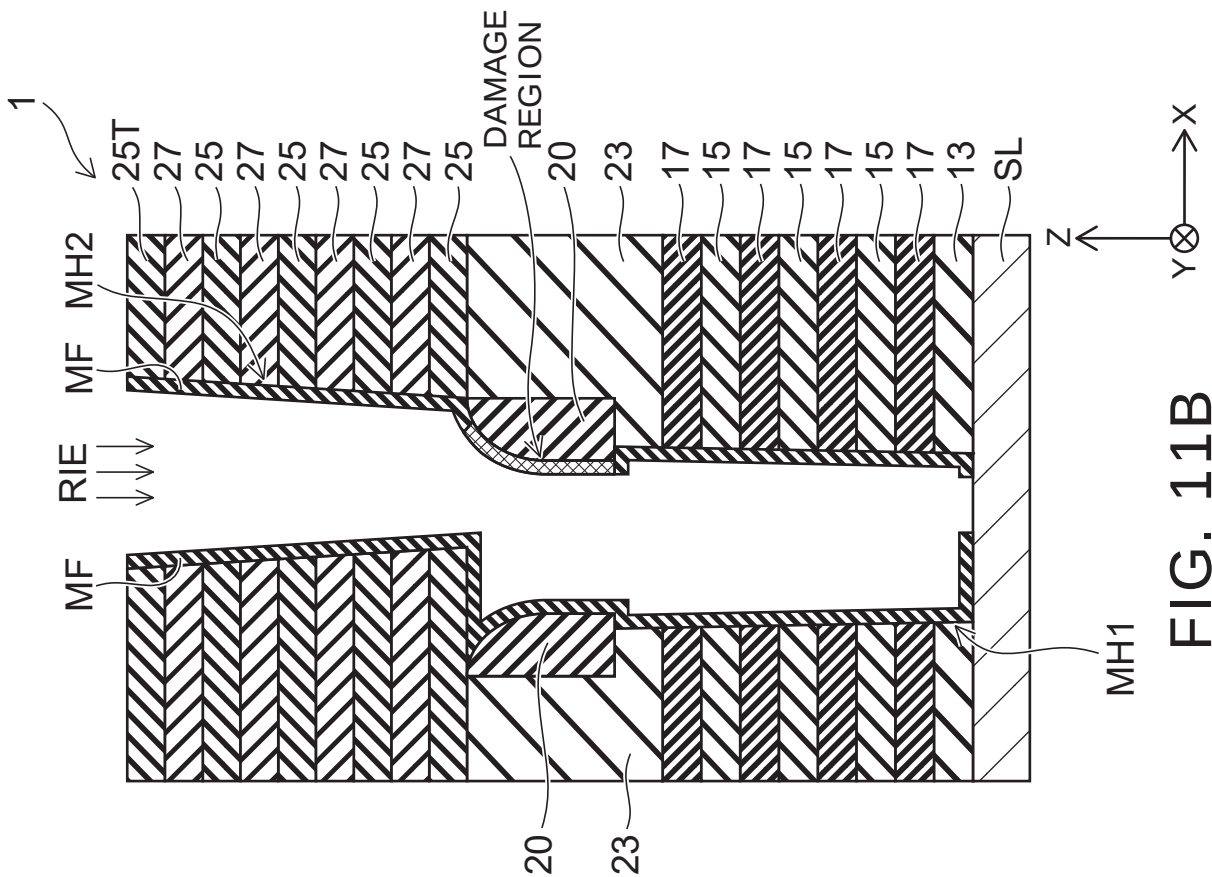


FIG. 11B

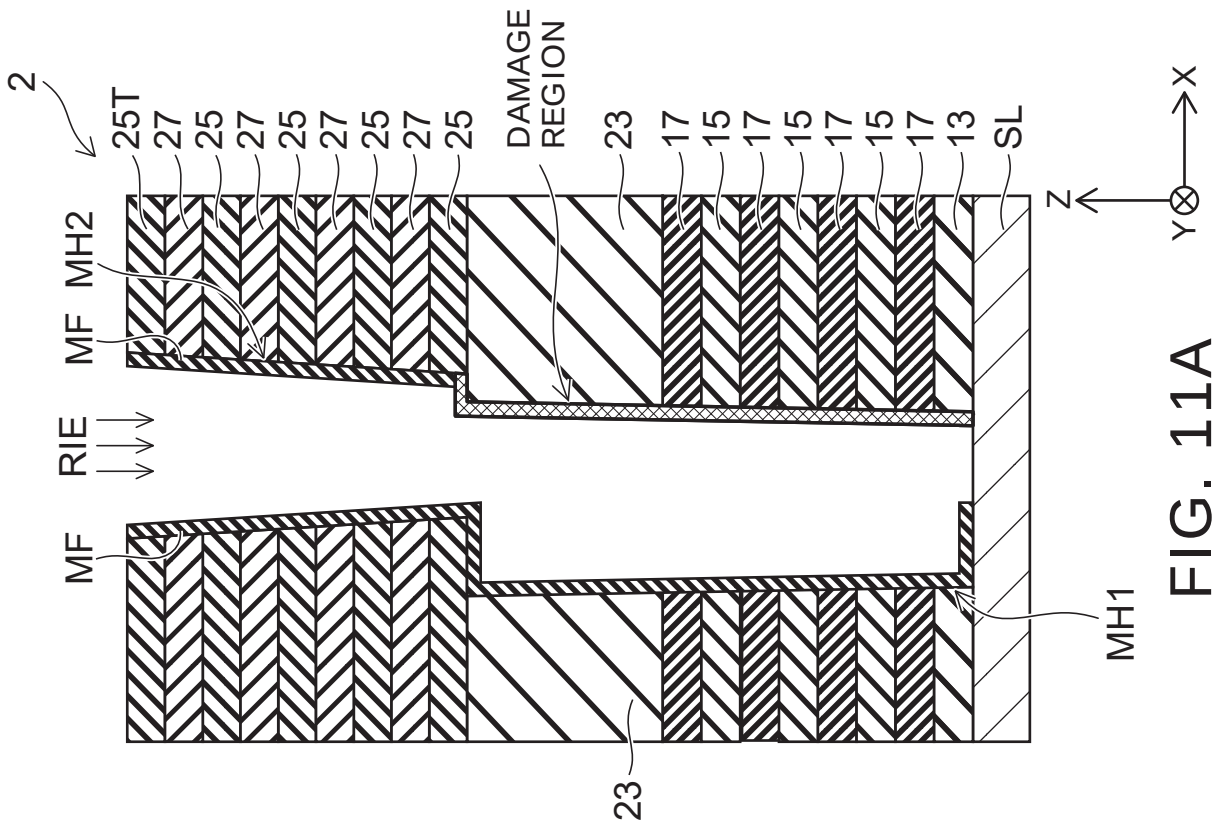


FIG. 11A

12/28

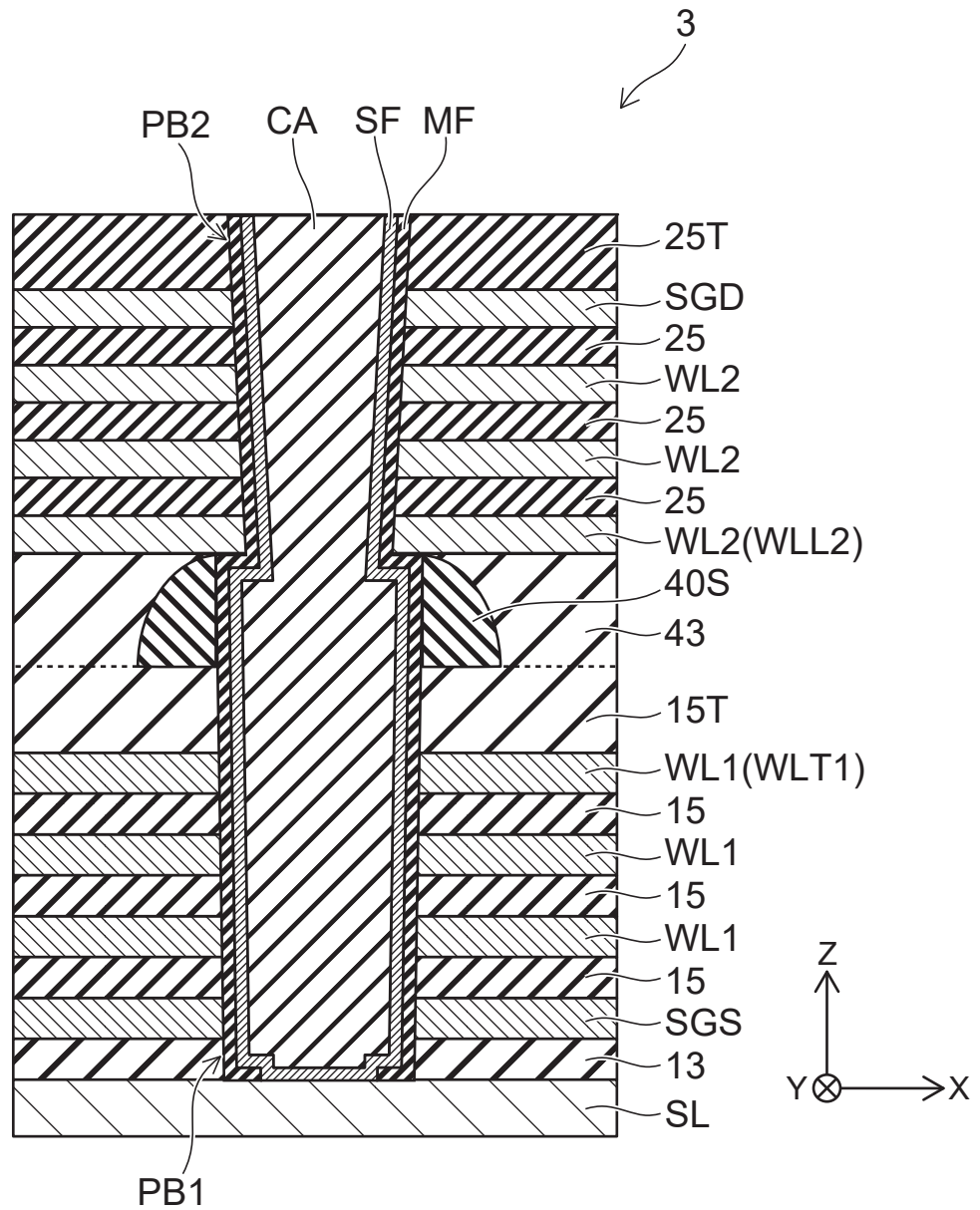


FIG. 12

Figure 1 is a cross-sectional view of a semiconductor device 100. The device 100 includes a substrate 13, a base layer 15, and a patterned layer 17. The patterned layer 17 is formed on the base layer 15 and has a series of rectangular openings 15T. The openings 15T are filled with a material 33. The top surface of the patterned layer 17 is covered by a layer 40. A coordinate system (X, Y, Z) is shown to the right of the device.

[illegible]

FIG. 13C

14/28

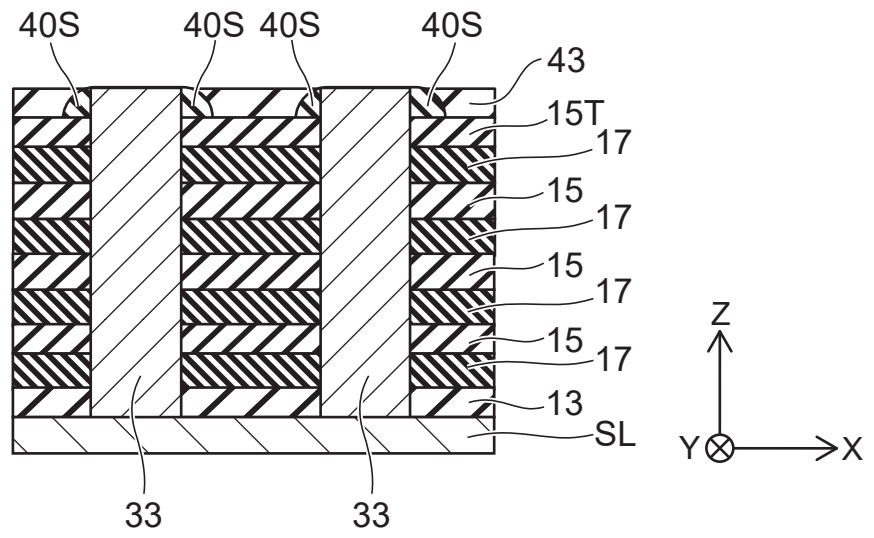


FIG. 14A

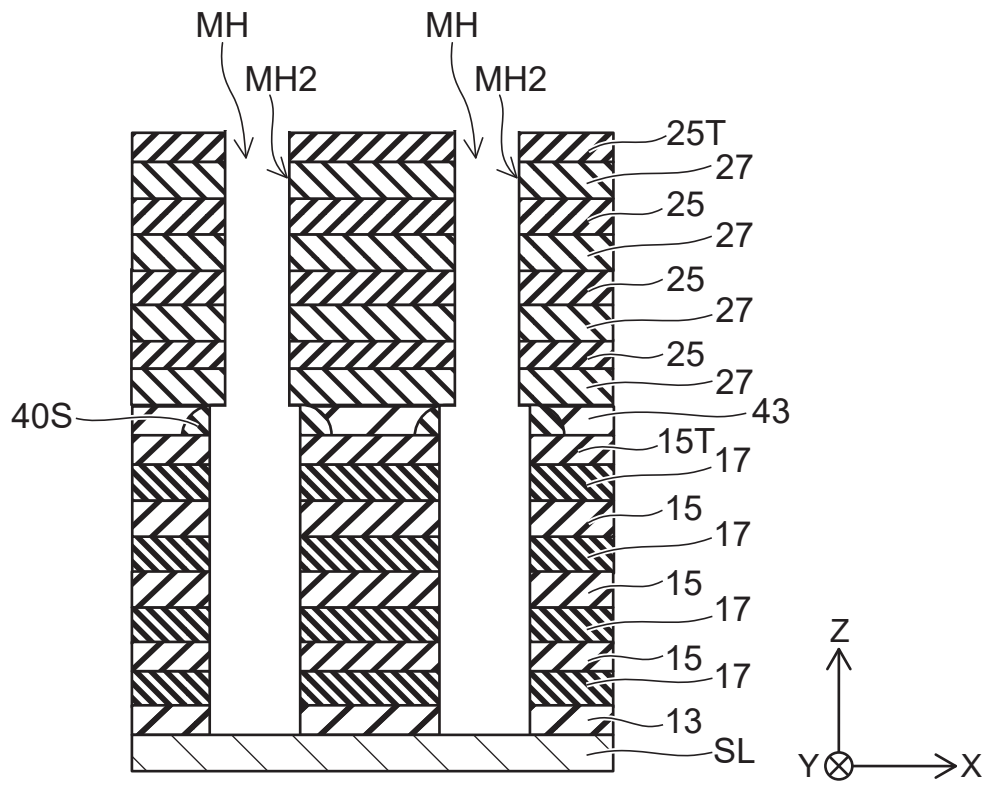


FIG. 14B

15/28

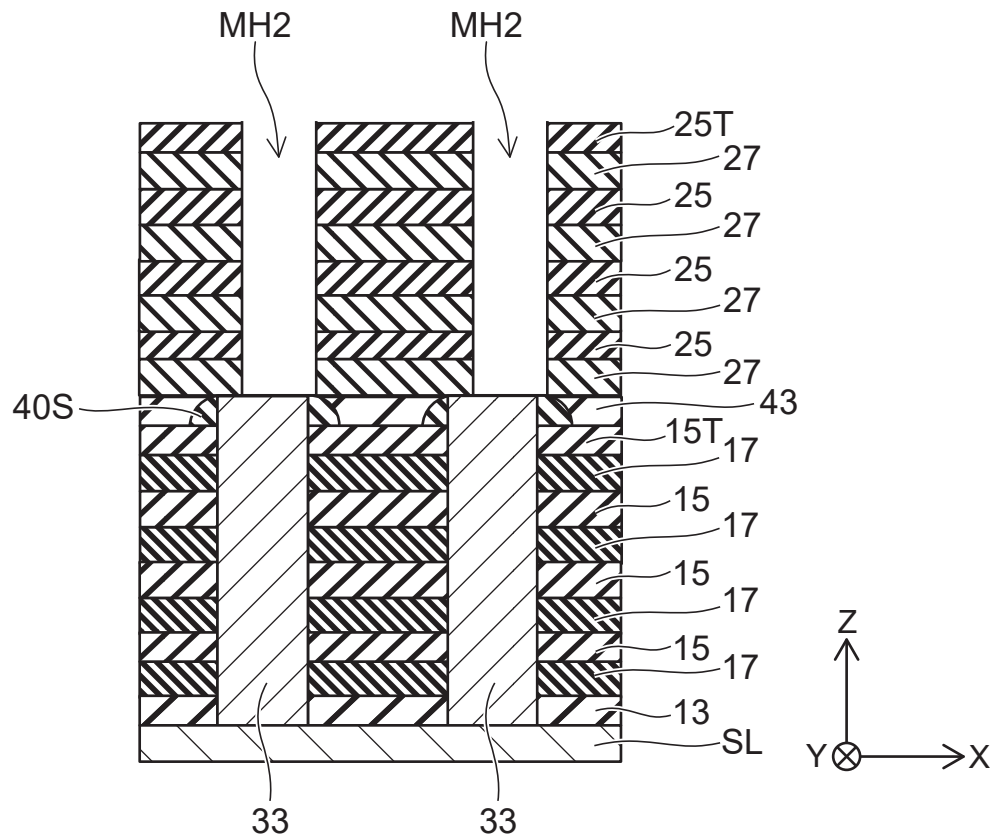


FIG. 15A

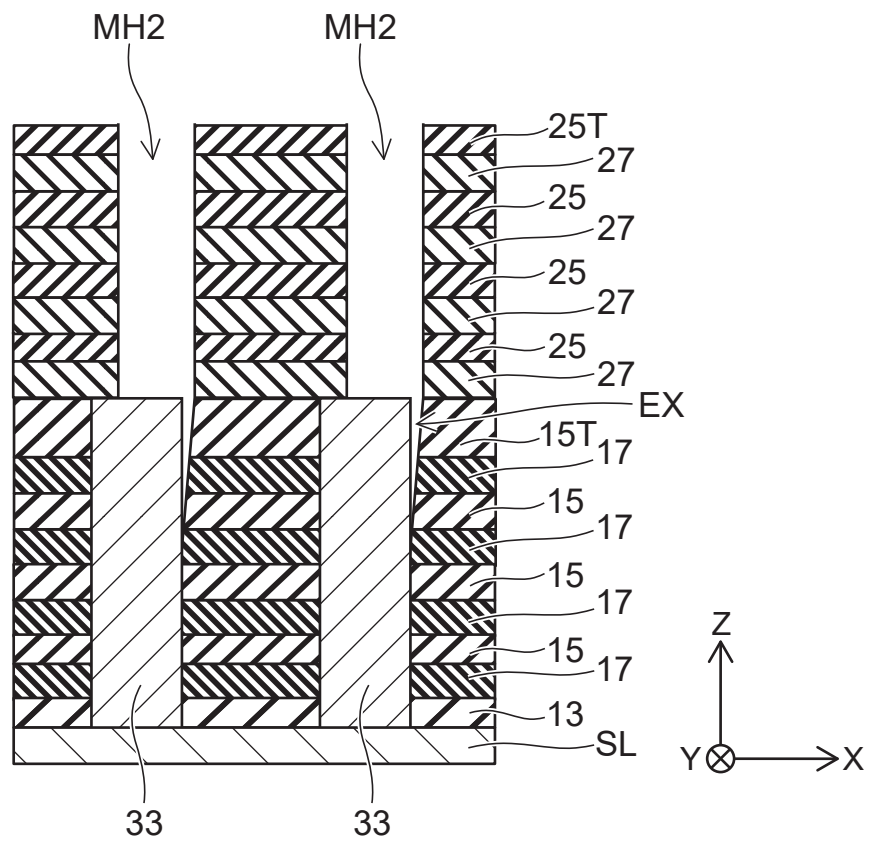


FIG. 15B

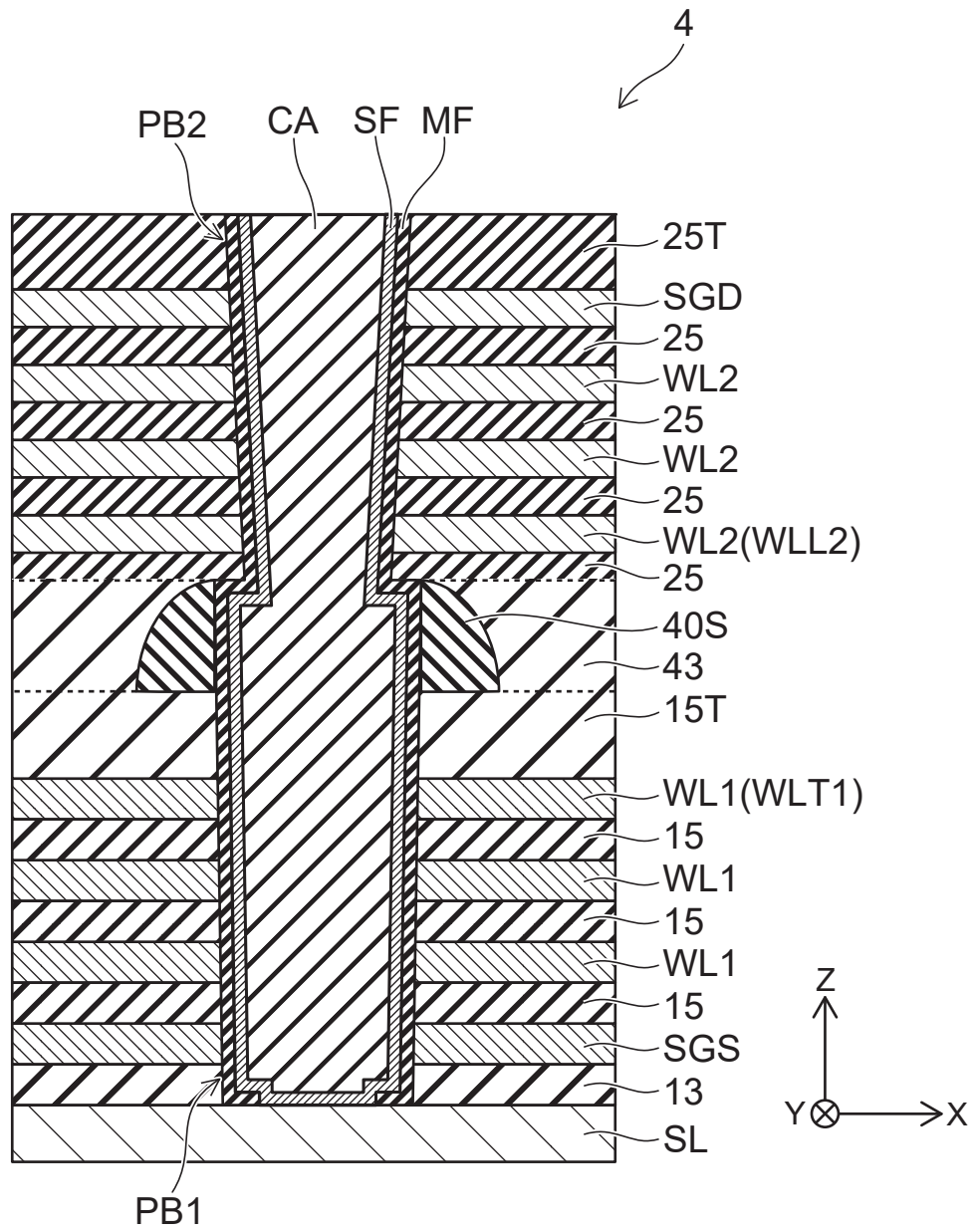


FIG. 16

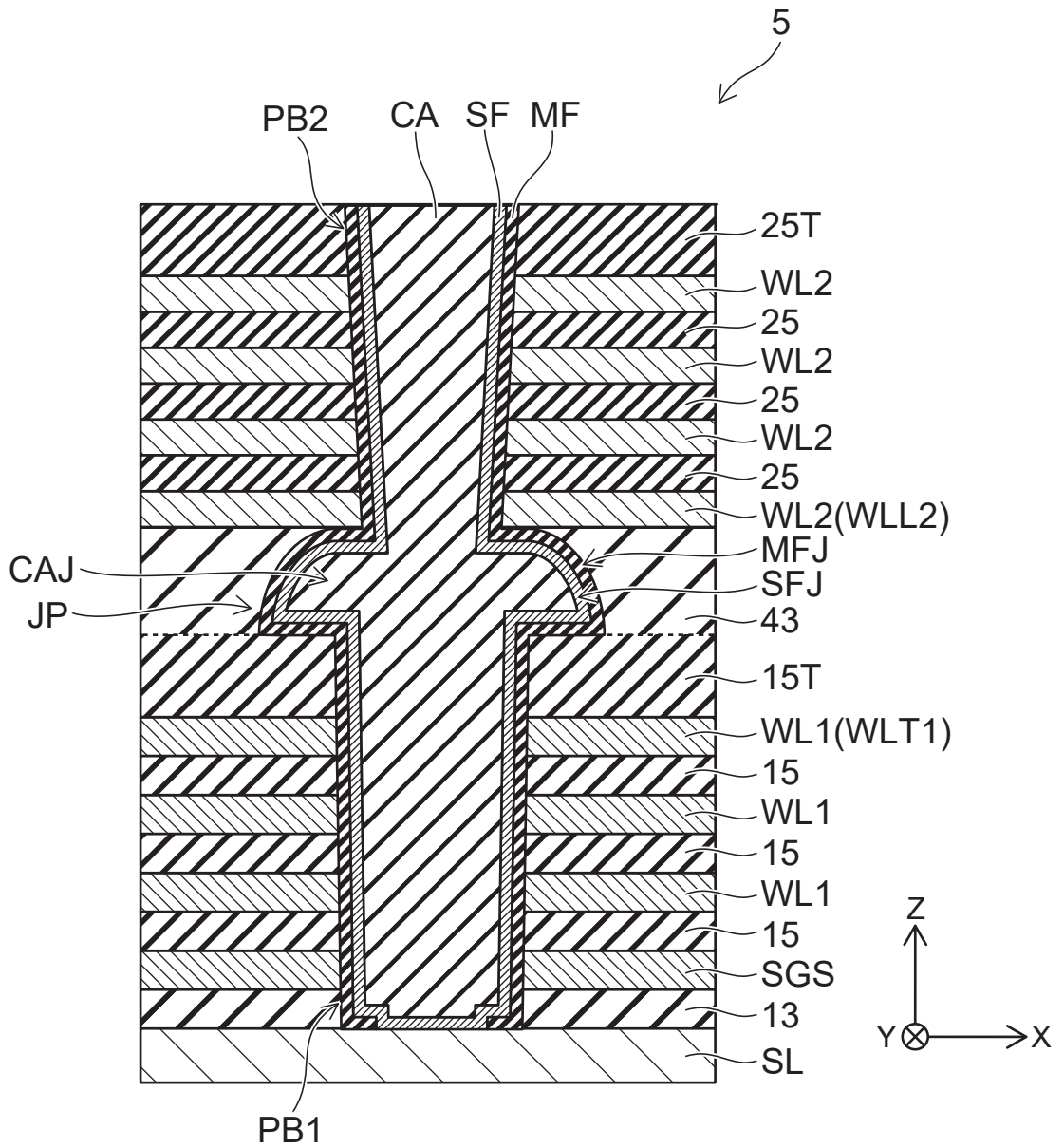


FIG. 17

18/28

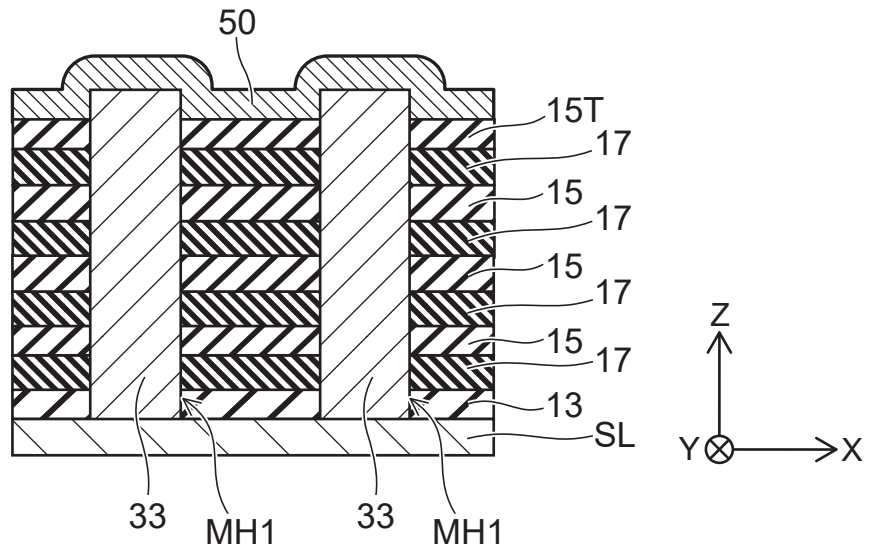


FIG. 18A

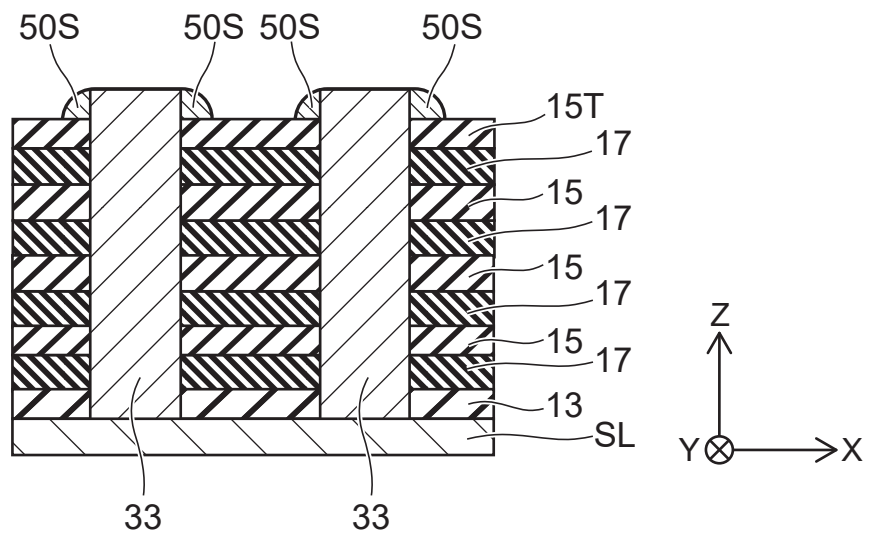


FIG. 18B

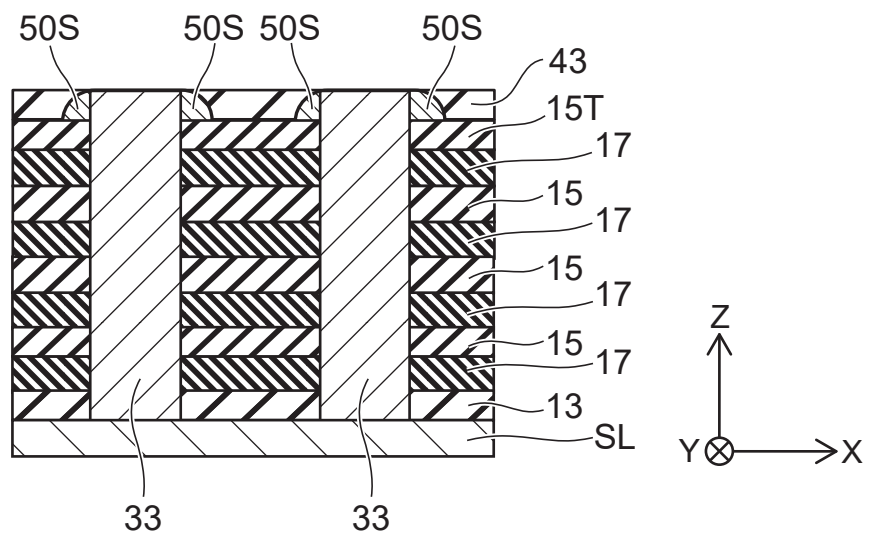


FIG. 18C

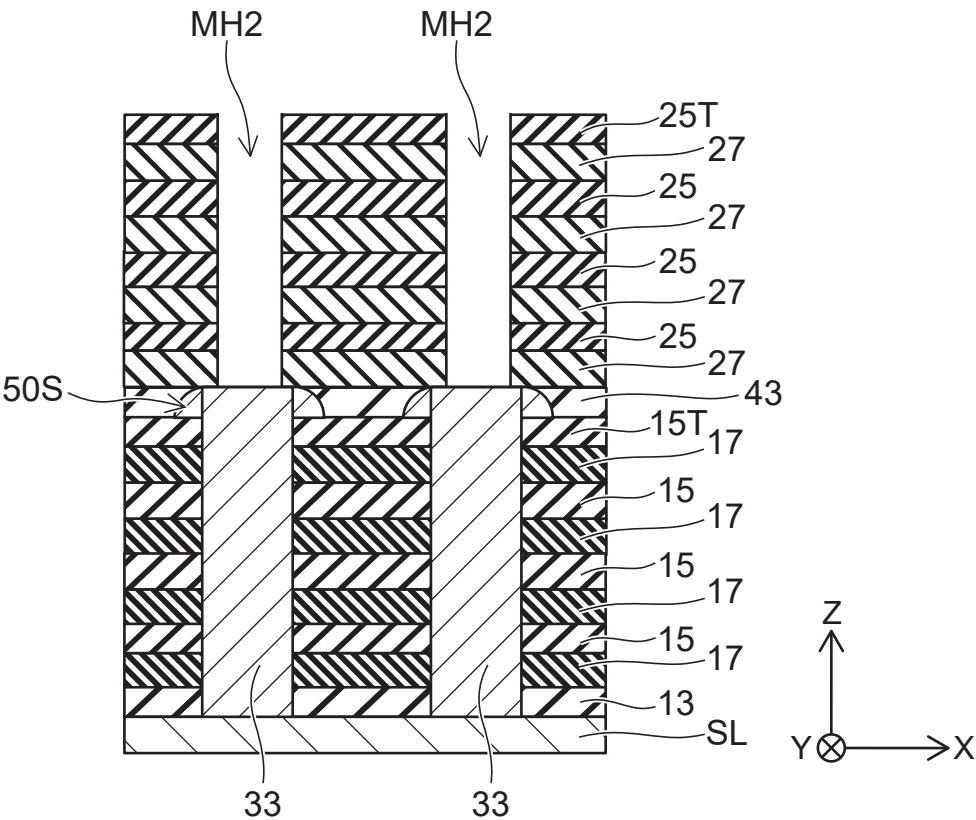


FIG. 19A

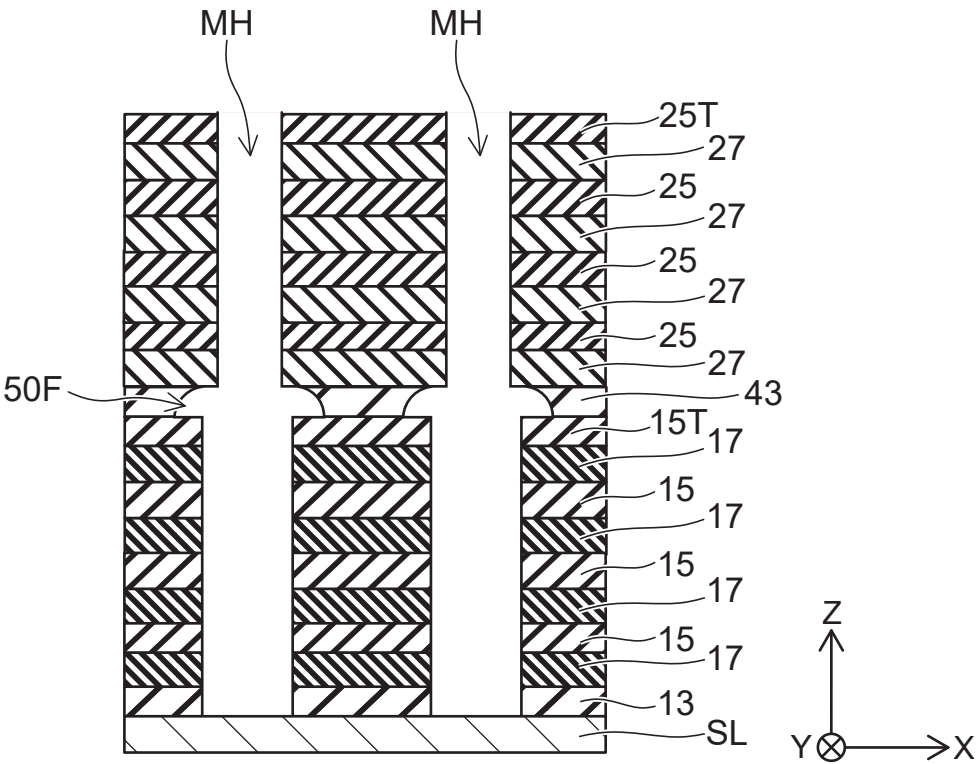
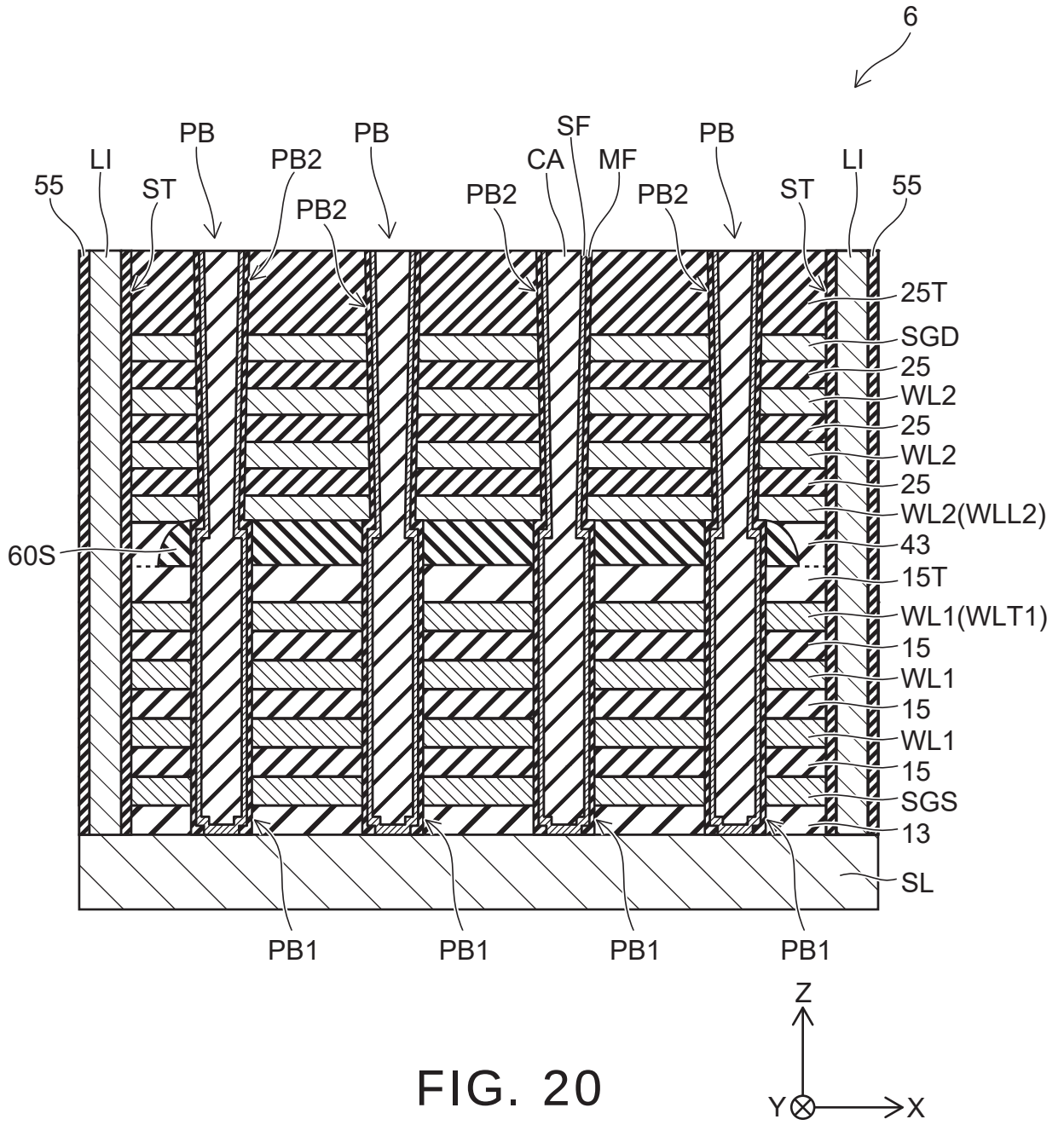


FIG. 19B



21/28

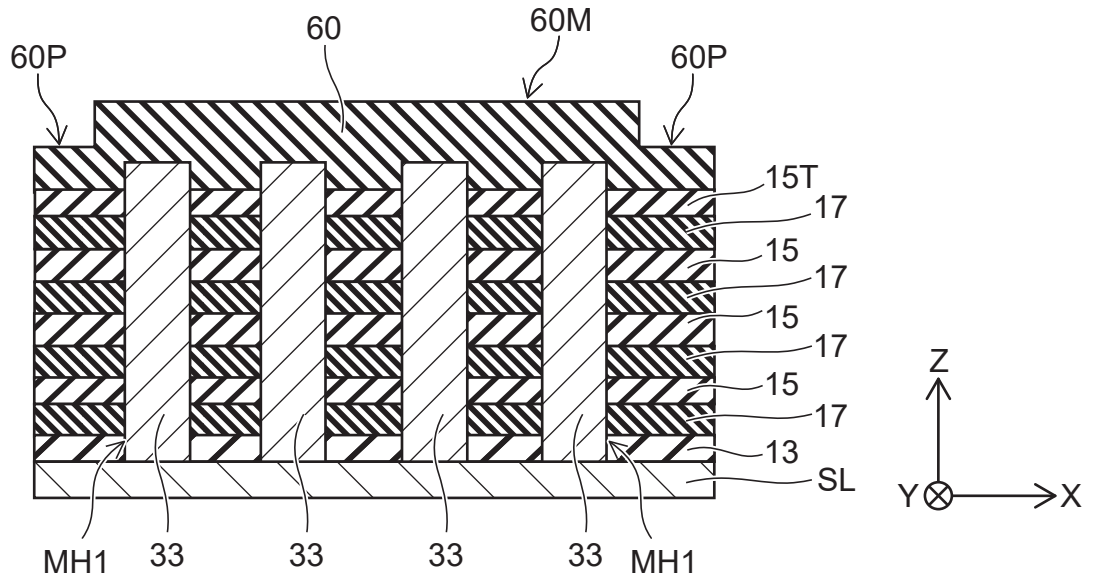


FIG. 21A

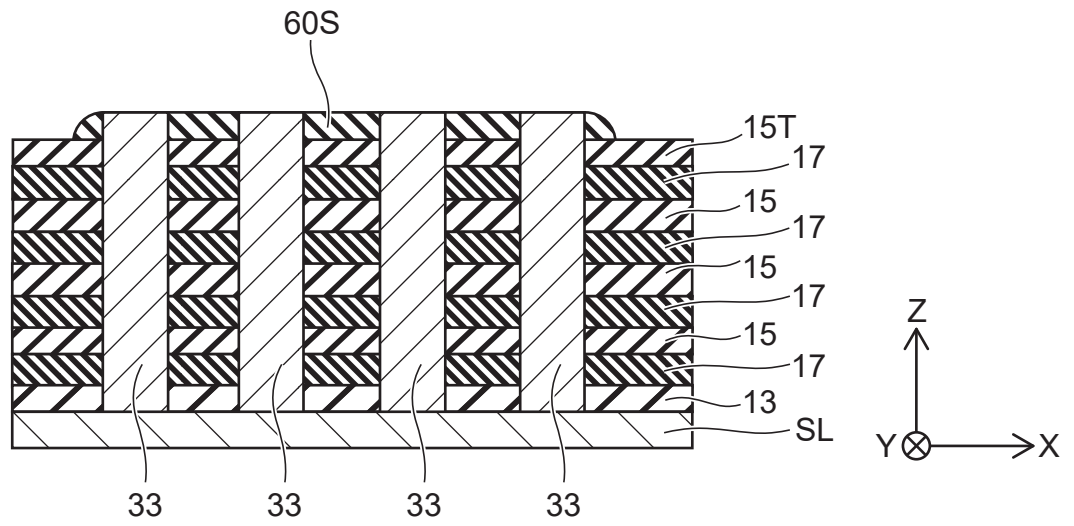


FIG. 21B

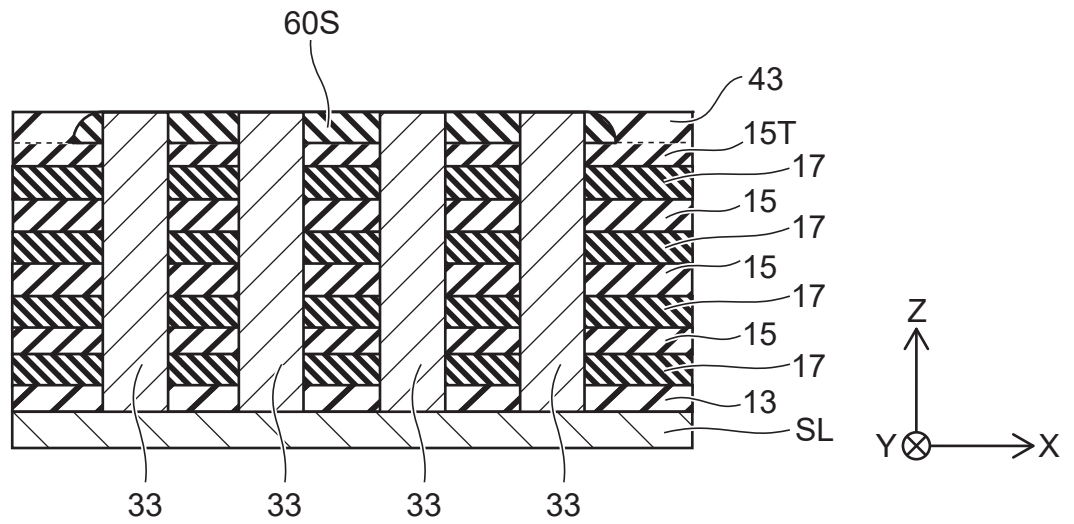


FIG. 21C

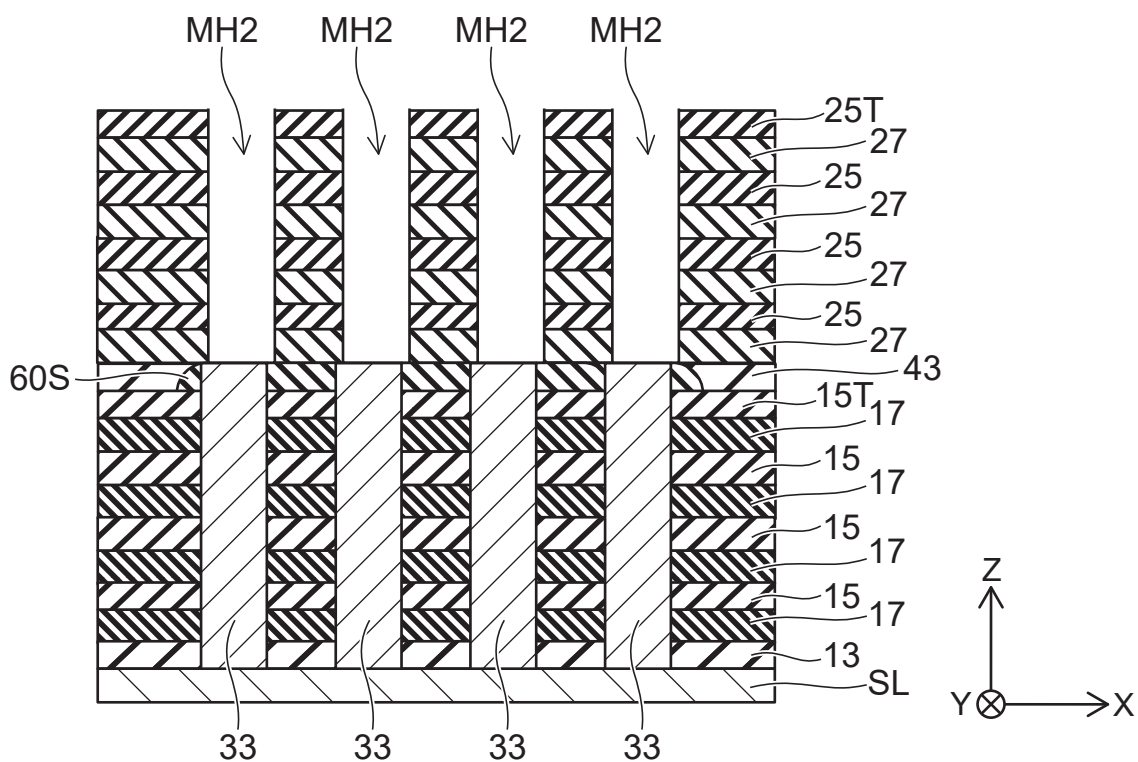


FIG. 22A

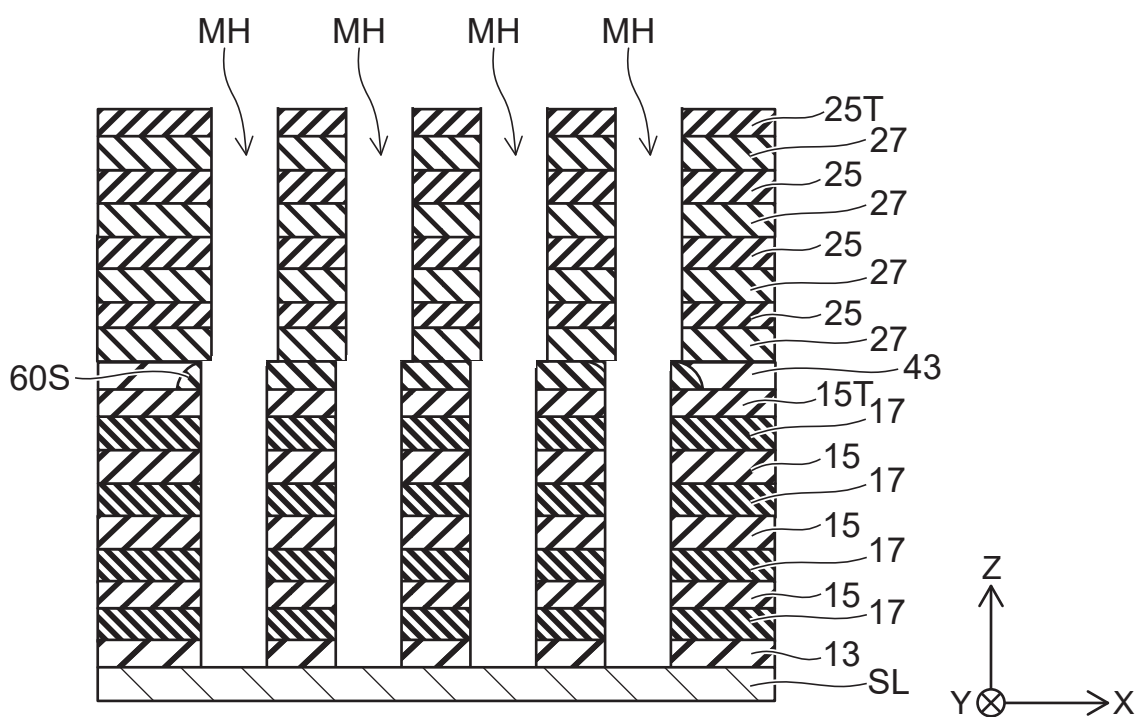
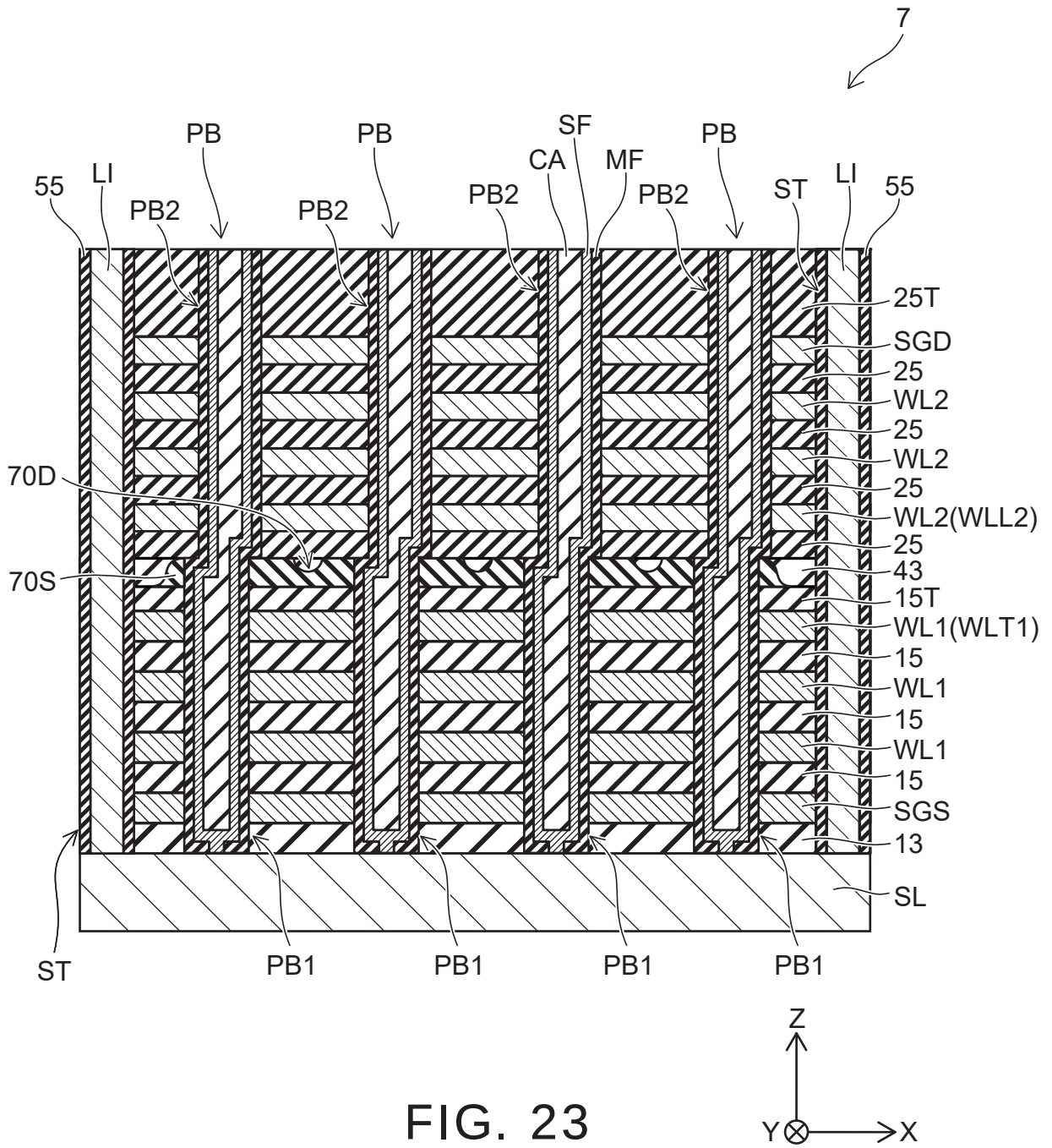


FIG. 22B



24/28

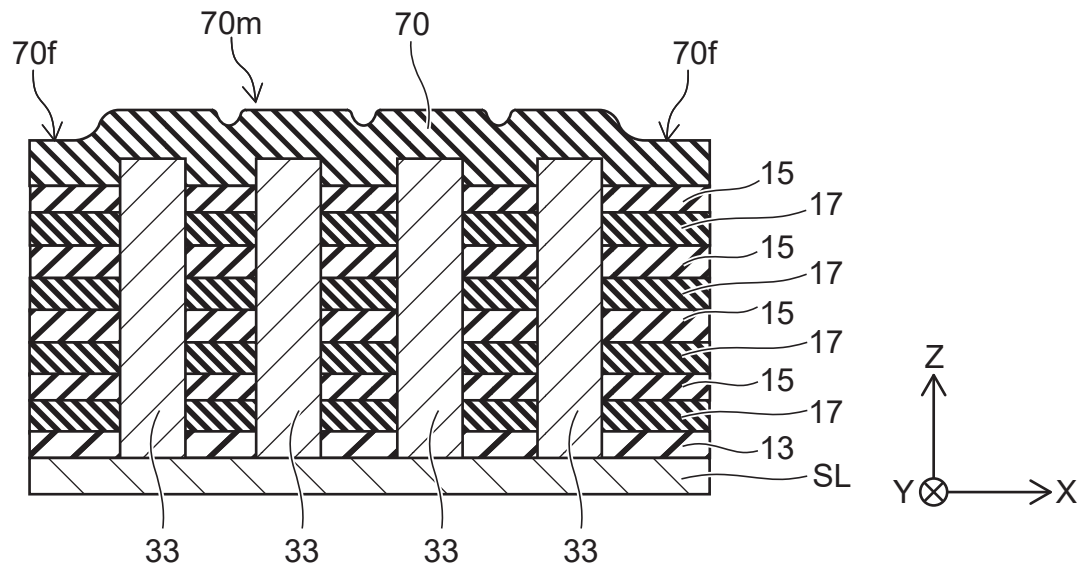


FIG. 24A

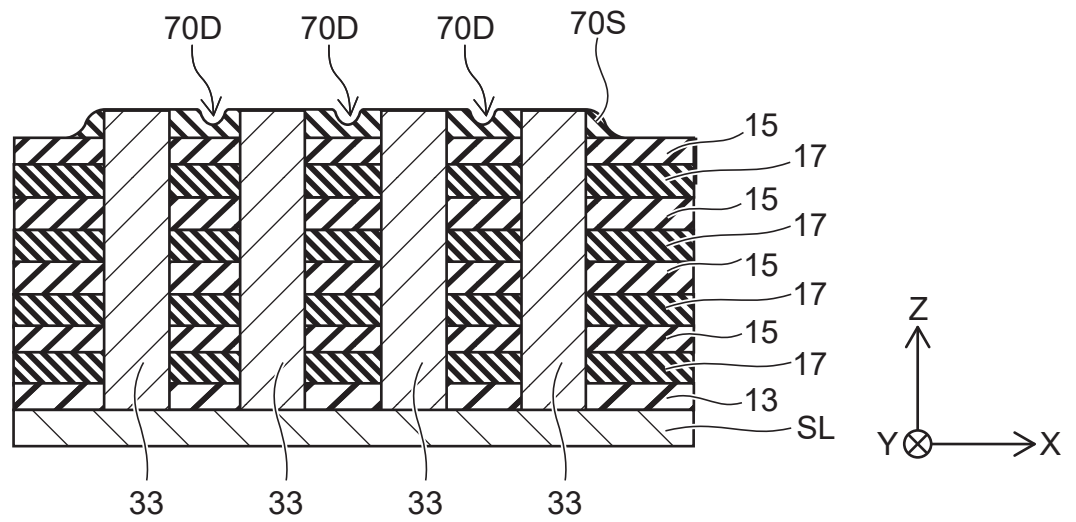


FIG. 24B

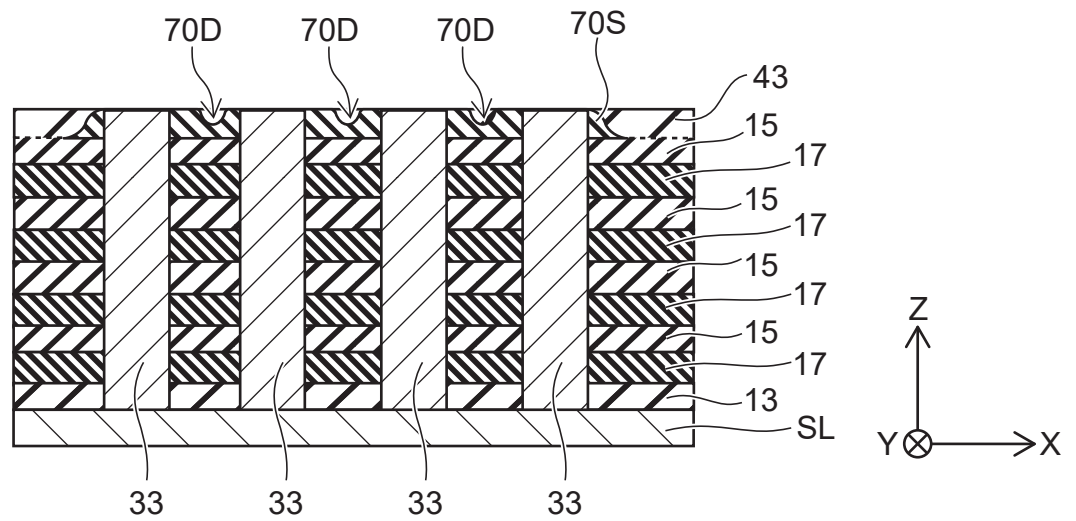
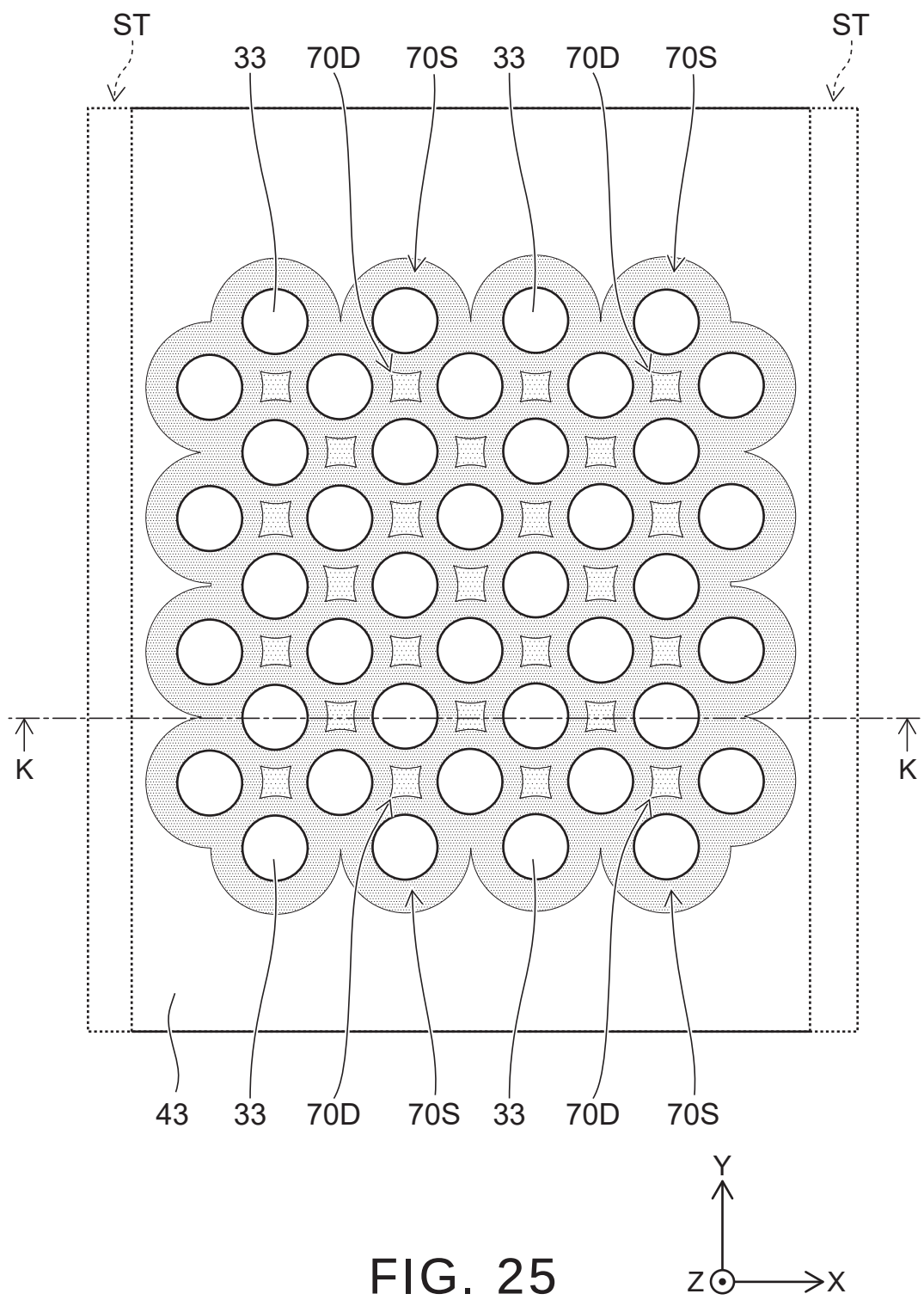


FIG. 24C



26/28

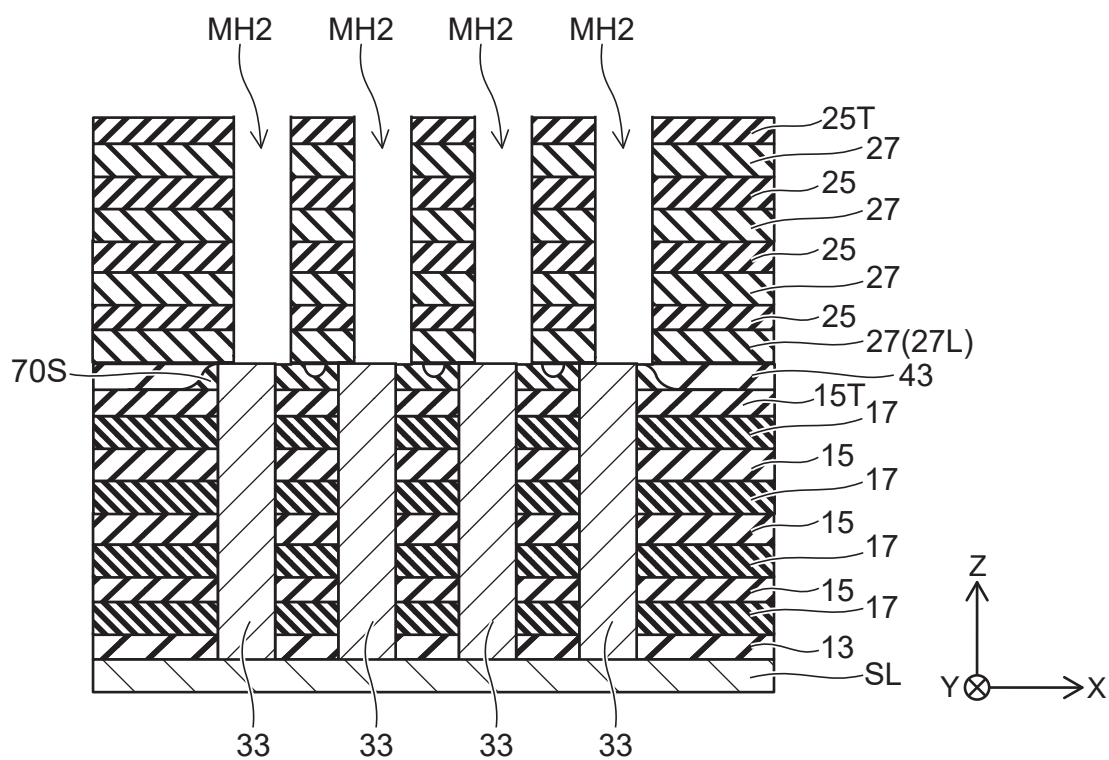


FIG. 26A

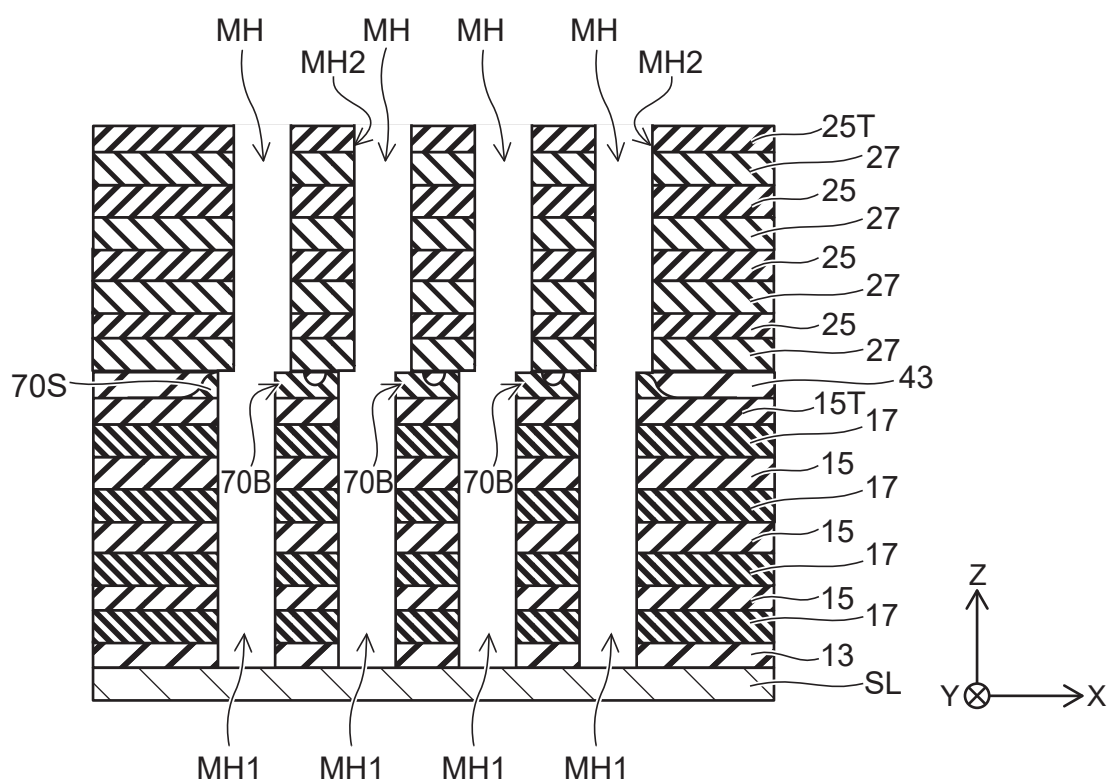


FIG. 26B

27/28

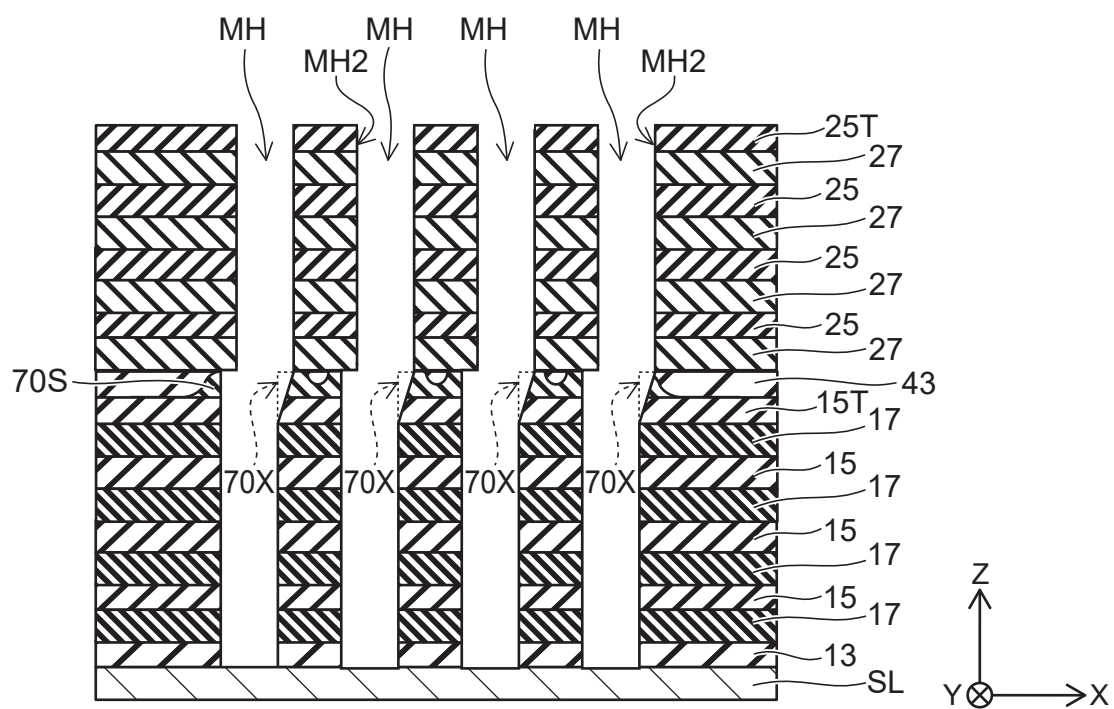


FIG. 27

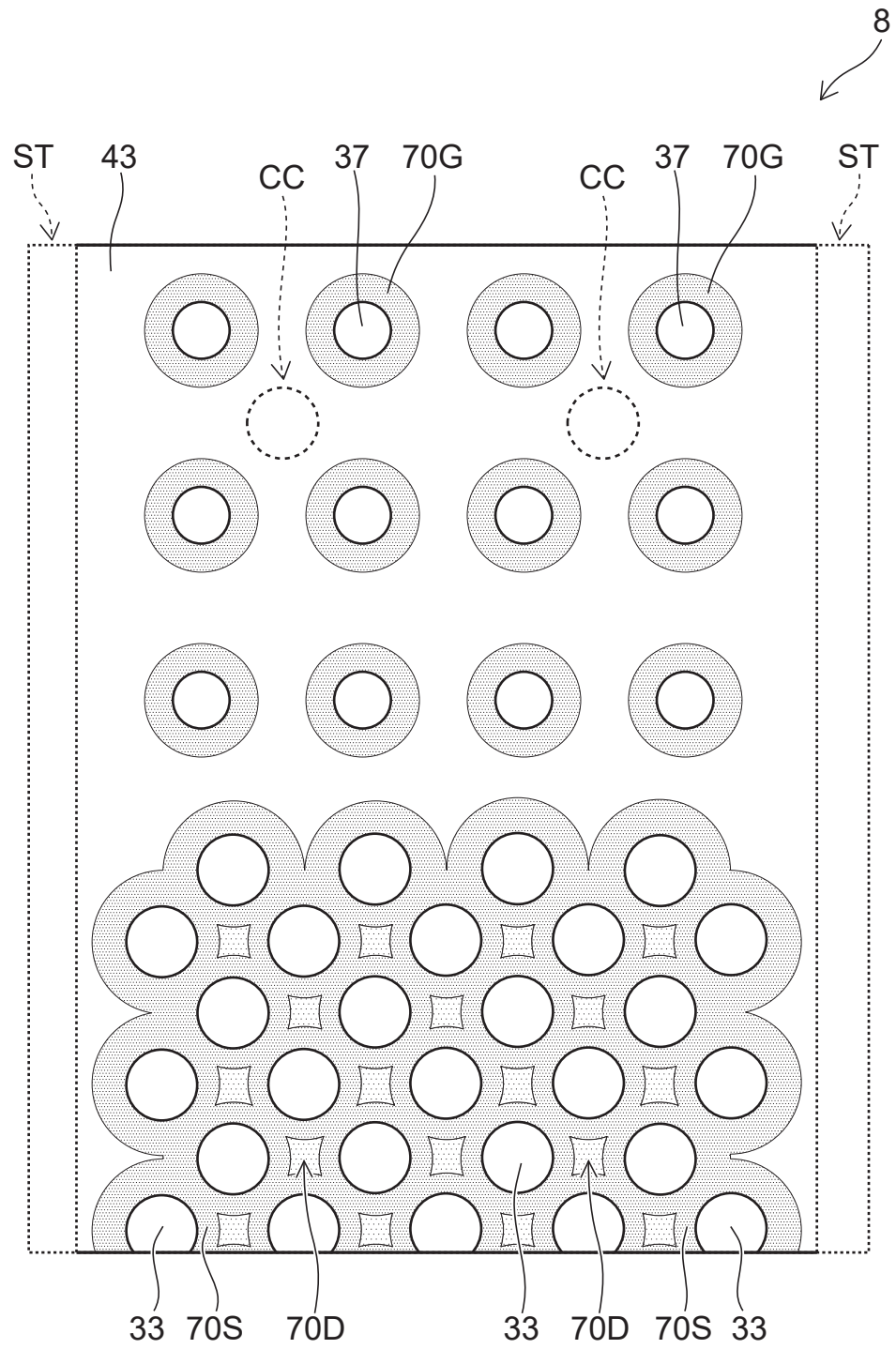


FIG. 28