

METHOD TO CONTROL THE CHANNEL LENGTH OF A VERTICAL TRANSISTOR BY
FIRST FORMING CHANNEL USING SELECTIVE EPI AND SOURCE /DRAIN
USING IMPLANTATION

Abstract

A method for a vertical MOS transistor whose vertical channel width can be accurately defined and controlled. Isolation regions are formed in a substrate. The isolation regions defining an active area. Then, we form a source region in the active area. A dielectric layer is formed over the active area and the isolation regions. We form a barrier layer over the dielectric layer. We form an opening in the barrier layer. A gate layer is formed in the opening. We form an insulating layer over the conductive layer and the barrier layer. We form a gate opening through the insulating layer, the gate layer and the dielectric layer to expose the source region. Gate dielectric spacers are formed over the sidewalls of the gate layer. Then, we form a conductive plug filling the gate opening. The insulating layer is removed. We form a drain region in top and side portions of the conductive plug and form doped gate regions in the gate layer. The remaining portions of the conductive plug comprise a channel region. A channel length is between the top of the source region and the drain region. We form an interlevel dielectric layer over the barrier layer, the gate layer, and the conductive plug. Contacts are formed through the interlevel dielectric layer to the doped gate regions, the drain region and the source region.

Figure 8