THRESHOLD VOLTAGE IMPROVEMENT EMPLOYING FLUORINE IMPLANTATION AND ADJUSTMENT OXIDE LAYER

Abstract of the Disclosure

An epitaxial semiconductor layer may be formed in a first area reserved for p-type field effect transistors. An ion implantation mask layer is formed and patterned to provide an opening in the first area, while blocking at least a second area reserved for n-type field effect transistors. Fluorine is implanted into the opening to form an epitaxial fluorine-doped semiconductor layer and an underlying fluorine-doped semiconductor layer in the first area. A composite gate stack including a high-k gate dielectric layer and an adjustment oxide layer is formed in the first and second area. P-type and n-type field effect transistors (FET's) are formed in the first and second areas, respectively. The epitaxial fluorine-doped semiconductor layer and the underlying fluorine-doped semiconductor layer compensate for the reduction of the decrease in the threshold voltage in the p-FET by the adjustment oxide portion directly above.

Fig. 8