

## ABSTRACT

Disclosed is a three-dimensional semiconductor device comprising channel regions that penetrate the stack structure and extend in a direction perpendicular to a top surface of the first substrate, a first interlayer dielectric layer on the stack structure, and a peripheral circuit structure on the first interlayer dielectric layer. The peripheral circuit structure includes peripheral circuit elements on a first surface of a second substrate. The peripheral circuit elements are electrically connected to the channel regions and at least one of the gate electrodes. The first substrate has a first crystal plane parallel to the top surface thereof. The second substrate has a second crystal plane parallel to the first surface thereof. An arrangement direction of atoms of the first crystal plane intersects an arrangement direction of atoms of the second crystal plane.

FIG. 6