~~What is claimed is:~~

CLAIMS

1. A method of forming a device comprising:

providing a substrate having a device region, wherein the device region comprises a source region, a gate region and a drain region defined thereon, the substrate is prepared with gate layers on the substrate;

patterning the gate layers to form a gate in the gate region and a field structure surrounding the drain region;

forming a source and a drain in the source region and drain region, wherein the drain is separated from the gate on a second side of the gate and the source is adjacent to a first side of the gate; and

forming an interconnection to the field structure, the interconnection is coupled to a potential, wherein the potential distributes the electric field across the substrate between the second side of the gate and the drain.

2. The method of claim 1 comprises forming an internal device isolation region along a channel width direction in the substrate between the gate and drain.

3. The method of claim 2 comprises forming a drift well in the substrate between the gate and drain region, underlapping a portion of the gate.

4. The method of claim 2 wherein the drift well encompasses the drain and internal device isolation region.

5. The method of claim 1 comprises forming an isolation region, wherein the isolation region isolates the device region from other regions of the device.

6. The method of claim 5 comprises forming a device well disposed within the isolation region.

7. The method of claim 6 wherein the device well encompasses the source, drain, drift well and internal device isolation region.

8. The method of claim 1 wherein the device is an NMOS transistor.

9. The method of claim 8 wherein the potential to which the interconnection is coupled is lower than the drain potential.

10. The method of claim 1 wherein the device is a PMOS transistor.

11. The method of claim 10 wherein the potential to which the interconnection is coupled is higher than the drain potential.

12. The method of claim 1 wherein the field structure comprises a conductive material.

13. The method of claim 1 wherein the field structure comprises a gate electrode.

14. The method of claim 13 wherein the field structure comprises a gate dielectric over the gate electrode.

15. The method of claim 1 comprises forming salicide contacts on the source and drain regions.

16. A method of forming a device comprising:

providing a substrate having a device region, wherein the device region comprises a source region, a gate region and a drain region defined thereon;

forming a drift well in the substrate between the gate and drain region;

depositing gate layers on the substrate;

patterning the gate layers to form a gate in the gate region and a field structure surrounding the drain region;

forming a source and a drain in the source region and drain region, wherein the drain is separated from the gate on a second side of the gate and the source is adjacent to a first side of the gate; and

forming an interconnection to the field structure, the interconnection is coupled to a potential, wherein the potential distributes the electric field across the substrate between the second side of the gate and the drain.

17. The method of claim 16 wherein the drift well underlaps a portion of the gate.

18. The method of claim 16 wherein the device is an NMOS transistor, and wherein the potential to which the interconnection is coupled is lower than the drain potential.

19. The method of claim 16 wherein the device is a PMOS transistor, and wherein the potential to which the interconnection is coupled is higher than the drain potential.

20. A device comprising:

a substrate having a device region, wherein the device region comprises a source region, a gate region and a drain region defined thereon;

a field structure surrounding the drain region;

a source and a drain in the source region and drain region, wherein the drain is separated from the gate on a second side of the gate and the source is adjacent to a first side of the gate; and

an interconnection to the field structure, the interconnection is coupled to a potential, wherein the potential distributes the electric field across the substrate between the second side of the gate and the drain.

What is claimed is:

CLAIMS

1. A method of forming a device comprising:

providing a substrate having a device region, wherein the device region comprises a source region, a gate region and a drain region defined thereon, the substrate is prepared with gate layers on the substrate;

patterning the gate layers, wherein patterning the gate layers forms both a gate in the gate region and a field structure surrounding the drain region;

forming a source and a drain in the source region and drain region, wherein the drain is separated from the gate on a second side of the gate and the source is adjacent to a first side of the gate; and

forming an interconnection to the field structure, the interconnection is coupled to a potential, wherein the potential distributes the electric field across the substrate between the second side of the gate and the drain.

2. The method of claim 1 comprises forming an internal device isolation region along a channel width direction in the substrate between the gate and drain.

3. The method of claim 2 comprises forming a drift well in the substrate between the gate and drain region, underlapping a portion of the gate.

4. The method of claim 3 wherein the drift well encompasses the drain and internal device isolation region.

5. The method of claim 1 comprises forming an isolation region, wherein the isolation region isolates the device region from other regions of the device.

6. The method of claim 5 comprises forming a device well disposed within the isolation region.

7. The method of claim 6 wherein the device well encompasses the source, drain, drift well and internal device isolation region.

8. The method of claim 1 wherein the device is an NMOS transistor.

9. The method of claim 8 wherein the potential to which the interconnection is coupled is lower than the drain potential.

10. The method of claim 1 wherein the device is a PMOS transistor.

11. The method of claim 10 wherein the potential to which the interconnection is coupled is higher than the drain potential.

12. The method of claim 1 wherein the gate layers comprise a gate electrode layer over a gate dielectric layer.

13. The method of claim 1 wherein the field structure comprises a gate electrode.

14. The method of claim 13 wherein the field structure comprises a gate dielectric under the gate electrode.

15. The method of claim 1 comprises forming salicide contacts on the source and drain regions.

16. A method of forming a device comprising:

providing a substrate having a device region, wherein the device region comprises a source region, a gate region and a drain region defined thereon;

forming a drift well in the substrate between the gate and drain region;

depositing gate layers on the substrate;

patterning the gate layers, wherein patterning the gate layers forms both a gate in the gate region and a field structure surrounding the drain region;

forming a source and a drain in the source region and drain region, wherein the drain is separated from the gate on a second side of the gate and the source is adjacent to a first side of the gate; and

forming an interconnection to the field structure, the interconnection is coupled to a potential, wherein the potential distributes the electric field across the substrate between the second side of the gate and the drain.

17. The method of claim 16 wherein the drift well underlaps a portion of the gate.

18. The method of claim 16 wherein the device is an NMOS transistor, and wherein the potential to which the interconnection is coupled is lower than the drain potential.

19. The method of claim 16 wherein the device is a PMOS transistor, and wherein the potential to which the interconnection is coupled is higher than the drain potential.

20. A method of forming a device comprising:

providing a substrate having a device region, wherein the device region comprises a source region, a gate region and a drain region defined thereon;

forming a gate in the gate region and a field structure surrounding only the drain region simultaneously;

forming a gate, a source and a drain in the gate, source and drain regions, wherein the drain is separated from the gate on a second side of the gate and the source is adjacent to a first side of the gate; and

forming an interconnection to the field structure, the interconnection is coupled to a potential, wherein the potential distributes the electric field across the substrate between the second side of the gate and the drain.