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METHOD FOR FORMING A MIM (METAL-INSULATOR-METAL) CAPACITOR

TECHNICAL FIELD

The present writing relates to the fabrication of integrated circuits.

5 More specifically, the present writing pertains to photolithography techniques for forming metal-insulator-metal (MIM) capacitors.

BACKGROUND ART

Photolithography techniques are used for fabricating components used
10 in integrated circuits, such as metal-insulator-metal (MIM) capacitors (referred to also as metal-intermetal-metal capacitors). In the photolithography process, a pattern mask that defines the size and shape of a component (e.g., an electrode) in one layer of a MIM capacitor is applied to a photosensitive layer (e.g., photoresist) that has been applied over a metal layer. A stepper holds the
15 pattern mask over the photoresist and projects the pattern image onto the photoresist through a lens. The pattern is imprinted into the photoresist; for example, the irradiated regions (e.g., the regions exposed through the pattern mask) are soluble in a specific solvent known as developer. The unexposed portions remain and thus the pattern is reproduced in the photoresist on the
20 surface of the metal layer.

The portion of the metal layer not underlying the photoresist is then removed, usually by etching. The portion of the metal layer not removed will be in the shape of the component(s) defined by the pattern. This process is



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repeated as needed to build each layer of the MIM capacitor. A dielectric layer is present to separate the MIM capacitor electrodes.

Thus, the MIM capacitor is essentially built-up by forming a multitude of components in a number of layers, one layer on top of another. Because the components in one layer interconnect with components in other layers, it is necessary to ensure that the components are accurately positioned and formed. As components get even smaller, it is necessary to position and form components to increasingly finer tolerances.

Conventional techniques rely on accurate alignment of the stepper and its target in order to accurately form components. For geometries of 0.18 microns and less, accuracy is improved by applying an inorganic anti-reflective coating (ARC) such as silicon-oxy-nitride (SiON) to the metal layer prior to a stepper or scanner shot. The inorganic ARC reduces reflection from the metal layer, allowing the stepper or scanner to more accurately acquire the marks that are used to align the stepper (or scanner) and the target.

In the prior art, the inorganic ARC is not removed after the stepper or scanner shot because it cannot be easily removed by a post-masking etch or clean. The inorganic ARC thus remains a part of the MIM capacitor. However, the presence of the inorganic ARC in the MIM capacitor degrades the electrical performance of the capacitor. Specifically, the presence of the inorganic ARC

reduces breakdown voltage and increases leakage current. For example, the breakdown voltage of a 400 Angstrom silane dioxide dielectric, using SiON as the inorganic ARC layer for the bottom electrode of a MIM capacitor, ranges from 26-32 volts.

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Accordingly, what is needed is a method and/or system that can be used for fabricating MIM capacitors with improved electrical performance. For example, it is desirable to be able to fabricate MIM capacitors that have higher breakdown voltages and reduced leakage currents. It is also desirable to be
10 able to fabricate MIM capacitors for which the variability of these parameters is reduced; that is, it is desirable for the range of values of breakdown voltage and leakage current to fall within a tighter tolerance band. The present invention provides a novel solution to these needs.

DISCLOSURE

The present writing provides methods and systems thereof that can be used for fabricating MIM capacitors with improved electrical performance. For example, the present writing provides methods and systems for fabricating
5 MIM capacitors that have higher breakdown voltages and reduced leakage currents. The present writing also provides methods and systems for fabricating MIM capacitors for which the variability of these parameters is reduced; that is, the range of values of breakdown voltage and leakage current falls within a tighter tolerance band.

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The present embodiment of the present writing pertains to methods, and systems thereof, for forming a metal-insulator-metal (MIM) capacitor using an organic anti-reflective coating (ARC). The first electrode of the MIM capacitor is formed from a first metal layer. The organic ARC is applied, and the second
15 electrode of the MIM capacitor is formed from a second metal layer. The organic ARC is then removed using a nominal clean technique. It is believed that removal of the organic ARC improves the performance of the MIM capacitor in that the breakdown voltage of the MIM capacitor increases and the leakage current decreases.

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According to the present invention, different types or brands of organic ARC can be used. In one embodiment, the organic ARC is AR2, and in another embodiment, the organic ARC is AR3. These or other types of organic ARC can

be used interchangeably.

In one embodiment, the first and second metal layers are aluminum, and the dielectric separating the first and second electrodes is either silicon-nitride or silicon-oxy-nitride. In addition, a barrier layer can be disposed between the dielectric and each of the first and second metal layers. In one embodiment, the barrier layers are comprised of Ti-nitride (TiN).

In one embodiment of a method for forming a MIM capacitor using organic ARC, a laminate that includes a first metal layer and a second metal layer separated by a dielectric and respective barrier layers is received by, for example, a stepper. A portion of the first metal layer and a portion of the dielectric (as well as the respective barrier layer) are removed to form the first electrode of the MIM capacitor. An organic ARC is applied to the first electrode and to the portion of the laminate exposed when the first metal layer and the dielectric were removed. A portion of the second metal layer and the respective barrier layer are removed to form the second electrode of the MIM capacitor. The remaining organic ARC is then removed (e.g., by cleaning).

In another embodiment of a method for forming a MIM capacitor using organic ARC, a first metal layer and a respective barrier layer are deposited on a substrate. A portion of the first metal layer (and the barrier layer) is removed to form the first electrode of the MIM capacitor. The dielectric and a second

metal layer (and a respective barrier layer) are deposited on at least the first electrode. An organic ARC is applied to the resultant laminate, and a portion of the dielectric, the second metal layer and the respective barrier layer are removed to form the second electrode of the MIM capacitor. The remaining organic ARC is then removed (e.g., by cleaning).

In each of the embodiments described above, organic ARC can also be applied prior to formation of the first electrode.

Because the organic ARC is removed, the performance of the MIM capacitor is improved. Specifically, the breakdown voltage of the MIM capacitor increases and the leakage current decreases. In addition, the range of values for breakdown voltage and for leakage current is reduced, so that these parameters can be controlled within tighter tolerances.

These and other objects and advantages of the present invention will become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiments which are illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

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FIGURE 1 is a side view of one embodiment of an exemplary stepper upon which embodiments of the present invention may be practiced.

FIGURE 2 is a block diagram of one embodiment of a stepper upon
10 which embodiments of the present invention may be practiced.

FIGURES 3A, 3B, 3C, 3D, 3E and 3F illustrate various stages of a process for fabricating a metal-insulator-metal (MIM) capacitor in accordance with one embodiment of the present invention.

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FIGURE 4 is a flowchart of the steps in a process for fabricating a MIM capacitor in accordance with the process of Figures 3A-3F.

FIGURES 5A, 5B, 5C, 5D and 5E illustrate various stages of a process for
20 fabricating a MIM capacitor in accordance with another embodiment of the present invention.

FIGURE 6 is a flowchart of the steps in a process for fabricating a MIM capacitor in accordance with the process of Figures 5A-5E.

5 FIGURE 7A compares breakdown voltage for a MIM capacitor fabricated in accordance with one embodiment of the present invention versus breakdown voltage for a MIM capacitor fabricated according to the prior art.

10 FIGURE 7B compares leakage current for a MIM capacitor fabricated in accordance with one embodiment of the present invention versus leakage current for a MIM capacitor fabricated according to the prior art.

BEST MODE FOR CARRYING OUT THE INVENTION

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

While the invention will be described in conjunction with the preferred

5 embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

Furthermore, in the following detailed description of the present invention,

10 numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to
15 unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions that follow are presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations for fabricating metal-insulator-metal (MIM)

20 capacitors. These descriptions and representations are the means used by those skilled in the art of MIM capacitor fabrication to most effectively convey the substance of their work to others skilled in the art. In the present application, a procedure, logic block, process, or the like, is conceived to be a self-consistent

sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, although not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system to fabricate a MIM capacitor.

It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present invention, discussions utilizing terms such as "applying," "removing," "forming," "etching," "receiving," "depositing" or the like, refer to actions and processes (e.g., processes 400 and 600 of Figures 4 and 6, respectively) of MIM capacitor fabrication.

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Figure 1 shows a side view of an exemplary stepper 100 upon which embodiments of the present invention may be practiced. Although a stepper is described herein, it is appreciated that lithography (photolithography) techniques can be implemented using other types of apparatus, such as a scanner. That is, embodiments of the present invention may be implemented on devices other than steppers.

In the present embodiment, stepper 100 includes a light source 122, masking blades 124, a pattern mask or reticle 126, a lens 128, and a stage 112. The light source 122 projects light through an opening 124a of masking blades 124, through the transparent portion of a pattern on reticle 126, through lens 128 and onto a metal layer 133 located on the stage 112. By doing so, the pattern of the reticle 126 is reproduced on the metal layer 133.

It is appreciated that the metal layer 133 may reside either directly on a wafer 130, on a passivation layer that has been deposited on the wafer 130, on another layer deposited on the wafer 130, on another component or device built on the wafer 130, or on some other substrate residing on wafer 130.

Figure 2 is a functional block diagram of a stepper 100 upon which embodiments of the present invention may be practiced. As described above, embodiments of the present invention may be implemented on devices other than steppers, such as scanners.

In the present embodiment, stepper 100 includes a stage 208 coupled to a stage movement device 210, a processor 212, a signal transceiver 204, and a memory 214. Substrate 206 is placed on stage 208 for processing in stepper 101; substrate 206 is typically a silicon wafer.

Memory 214 contains program instructions implemented through processor 212. Memory 214 can either be permanent memory, such as read only memory (ROM), or temporary memory, such as random access memory (RAM). Memory 214 can also be any other type of memory storage capable of containing program instructions, such as a hard drive, a CD ROM, or flash memory. Processor 212 can either be an existing system processor or microprocessor, a dedicated digital signal processing (DSP) processor unit, or a dedicated controller or microcontroller. Alternatively, the program instructions may be implemented using an implementation of a state machine.

Signal transceiver 204 is coupled to processor 212. Signal transceiver 204 is a source of an electromagnetic signal, such as a laser. Additionally, signal transceiver 204 is a receiver for an electromagnetic signal, such as the return signal that is reflected from substrate 206.

Figures 3A, 3B, 3C, 3D, 3E and 3F illustrate various stages of a process for fabricating a MIM capacitor in accordance with one embodiment of the present invention. With reference first to Figure 3A, a structure 305 (e.g., a laminate) is either formed on or received by stepper 100 of Figures 1 and 2 (as described above, embodiments of the present invention may be implemented on devices other than steppers, such as scanners). The structure 305 is located (sits on top of) wafer 130 (Figure 1) or substrate 206 (Figure 2), for example.

In this embodiment, structure 305 includes a first metal layer 342, a first barrier layer 350, a dielectric layer 346, a second barrier layer 352, and a second metal layer 344. Photoresist 340 is applied to first metal layer 342 in a particular pattern using a known photolithography technique, such as that
5 illustrated by Figure 1. In the present embodiment, the first metal layer 342 and the second metal layer 344 are comprised of aluminum, the dielectric layer 346 is comprised of a high-k dielectric such as silicon nitride or silicon-oxy-nitride, and the first barrier layer 350 and the second barrier layer 352 are comprised of Ti-nitride (TiN). However, it is appreciated that these elements may be made of
10 other types of materials.

With reference to Figure 3B, a known etching process is used to remove the portions of first metal layer 342 (Figure 3A), first barrier layer 350 and dielectric layer 346 that are not underlying photoresist 340 (Figure 3A). That is,
15 in this embodiment, the etching process removes material up to second barrier layer 352 to form first electrode 360 with underlying first barrier layer 350 and dielectric layer 346.

Now with reference to Figure 3C, in accordance with the present
20 embodiment of the present invention, organic anti-reflective coating (ARC) 370 is applied to first electrode 360 and to the surfaces of structure 315 (e.g., the surfaces of second barrier layer 352) that are exposed by the etching process. The organic ARC 370 functions to reduce reflection from the structure 315,

allowing the stepper 100 (Figures 1 and 2) to more accurately acquire the marks that are used to align the stepper 100 and the target (e.g., structure 315). Accordingly, the components that make up the finished MIM capacitor will be accurately positioned and formed.

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According to the present invention, different types or brands of organic ARC can be used. One factor to consider when selecting an organic ARC to be used is the thickness to be applied, which in turn is dependent on the optimum process conditions associated with the lithography (e.g., photolithography) technique being employed. In one embodiment, the organic ARC 370 is AR2, and in another embodiment, the organic ARC 370 is AR3. These or other types of organic ARC can be used interchangeably depending, for instance, on the factors described above.

15 With reference next to Figure 3D, photoresist 340 is applied to structure 320. In Figure 3E, a known etching process is used to remove the portions of second metal layer 342 (Figure 3D) and second barrier layer 352 that are not underlying photoresist 340 (Figure 3D). That is, in this embodiment, the etching process removes material up to the underlying substrate to form second
20 electrode 362. A component 380 also formed in the etching process is shown.

Now with reference to Figure 3F, structure 330 comprising a MIM capacitor and other components is shown. The second electrode 362 is

coupled to line 382a through region 390 by via 384a, first electrode 360 is similarly coupled to line 382b by via 384b, and component 380 is coupled to line 382c by via 384c. Region 390 may comprise deposited low-k material such as silicon-dioxide (SiO_2), SOG (spin on glass), USG (undoped spin on glass), or
5 other types of material used in the fabrication of MIM capacitors.

Significantly, in accordance with the present invention, organic ARC 370 is removed using, for example, a known nominal cleaning technique. As a result, the MIM capacitor fabricated in accordance with the present invention
10 does not incorporate ARC, thereby improving the electrical performance of the MIM capacitor. Specifically, in accordance with the present invention, breakdown voltage is increased and leakage current is decreased. Furthermore, the variation in these parameters is reduced; that is, the range of values associated with these parameters fits within a tighter tolerance. For
15 example, the breakdown voltage for a MIM capacitor fabricated according to the present invention increases to 40-43 volts.

It is appreciated that, in another embodiment, organic ARC 370 can be applied to first metal layer 342 of Figure 3A, prior to forming first electrode 360
20 of Figure 3B, and then removed (cleaned).

Figure 4 is a flowchart of the steps in a process 400 for fabricating a MIM capacitor in accordance with the process of Figures 3A-3F. In step 410, a

laminate such as structure 305 of Figure 3A is received by, or formed on, stepper 100 (Figures 1 and 2). A photoresist 340 is applied to the laminate.

5 In step 420 of Figure 4, with reference to Figures 3A and 3B, a first electrode 360 is formed by removing at least a portion of the material not underlying photoresist 340. In one embodiment, an organic ARC (e.g., organic ARC 370 of Figure 3C) is applied to first metal layer 342 prior to formation of first electrode 360.

10 In step 430 of Figure 4, with reference also to Figures 3C and 3D, organic ARC 370 is applied to first electrode 360 as well as to the surfaces of structures 315 and 320 that were exposed when first electrode 360 was formed in step 420.

15 In step 440 of Figure 4, with reference to Figure 3E, second electrode 362 is formed by removing the material not underlying photoresist 340 of Figure 3D.

20 In step 450 of Figure 4, in accordance with the present invention, the organic ARC 370 (Figures 3C and 3D) is removed using, for example, a nominal cleaning technique.

Figures 5A, 5B, 5C, 5D and 5E illustrate various stages of a process for fabricating a MIM capacitor in accordance with another embodiment of the present invention. This embodiment differs from the embodiment of Figures 3A-3F in the order in which the electrodes of the MIM capacitor are formed.

- 5 Relatively speaking, in the process of Figures 3A-3F, the first electrode is formed from the top metal layer, while in the process of Figures 5A-5E, the first electrode is formed from the bottom metal layer.

With reference to Figure 5A, in the present embodiment, a first metal
10 layer 542 and a first barrier layer 550 are deposited on some type of substrate 545. As described in conjunction with Figure 1 above, substrate 545 may be a wafer 130, a passivation layer that has been deposited on the wafer 130, another type of layer deposited on the wafer 130, another component or device built on the wafer 130, or some other type of substrate residing on wafer 130.

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Photoresist 540 is applied to first metal layer 542 in a particular pattern using a known photolithography technique, such as that illustrated by Figure 1. In the present embodiment, the first metal layer 542 is comprised of aluminum, and the first barrier layer 550 is comprised of Ti-nitride (TiN). However, it is
20 appreciated that these elements may be made of other types of materials.

With reference next to Figure 5B, a known etching process is used to remove the portions of first metal layer 542 (Figure 5A) and first barrier layer

550 that are not underlying photoresist 540 (Figure 5A). That is, in this embodiment, the etching process removes material up to substrate 545 to form first electrode 560. Another component 580 formed in the etching process is also shown.

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Now with reference to Figure 5C, a dielectric layer 546 is deposited over first barrier layer 550 (first electrode 560 and component 580), a second barrier layer 552 is deposited over dielectric layer 546, and a second metal layer 544 is deposited over second barrier layer 552. In accordance with the present
10 embodiment of the present invention, organic anti-reflective coating (ARC) 570 is applied to second metal layer 544. Photoresist 540 is also applied to structure 515.

The organic ARC 570 functions to reduce reflection from the structure
15 515, allowing the stepper 100 (Figures 1 and 2) to more accurately acquire the marks that are used to align the stepper 100 and the target (e.g., structure 515). Accordingly, the components that make up the finished MIM capacitor will be accurately positioned and formed. In one embodiment, the organic ARC 570 is AR2, and in another embodiment, the organic ARC 570 is AR3.

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In Figure 5D, a known etching process is used to remove the portions of second metal layer 544 (Figure 5C), second barrier layer 552, and dielectric layer 546 that are not underlying photoresist 540 (Figure 5C). That is, in this

embodiment, the etching process removes material up to the underlying first barrier layer 550 to form second electrode 562. Second electrode 562 is separated from first electrode 560 by second barrier layer 552, dielectric layer 546, and first barrier layer 550.

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Significantly, in accordance with the present invention, organic ARC 570 is removed using, for example, a known nominal cleaning technique. As a result, the MIM capacitor fabricated in accordance with the present invention does not incorporate ARC, thereby improving the electrical performance of the MIM capacitor. Specifically, in accordance with the present invention, breakdown voltage is increased and leakage current is decreased. Furthermore, the variation in these parameters is reduced; that is, the range of values associated with these parameters fits within a tighter tolerance.

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Now with reference to Figure 5E, structure 525 comprising a MIM capacitor and other components is shown. The second electrode 562 is coupled to line 582b through region 590 by via 584b, first electrode 560 is similarly coupled to line 582a by via 584a, and component 580 is coupled to line 582c by via 584c. Region 590 may comprise deposited material such as SiO₂ or other types of low-k materials used in the fabrication of an inter-metal dielectric layer (IMD).

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It is appreciated that, in another embodiment, organic ARC 570 can be applied to first metal layer 542 of Figure 5A, prior to forming first electrode 560 of Figure 5B, and then removed (cleaned).

5 Figure 6 is a flowchart of the steps in a process 600 for fabricating a MIM capacitor in accordance with the process of Figures 5A-5E. In step 610, with reference also to Figure 5A, first metal layer 542 is deposited on a substrate 545. In one embodiment, first barrier layer 550 is also deposited on first metal layer 542. A photoresist 540 is also applied.

10 In step 620 of Figure 6, with reference also to Figure 5B, a first electrode 560 is formed by removing the material (the portion of first metal layer 542) not underlying photoresist 540. In one embodiment, an organic ARC (e.g., organic ARC 570 of Figure 5C) is applied to first metal layer 542 prior to formation of first
15 electrode 560. Other components such as component 580 can also be formed.

 In step 630 of Figure 6, with reference also to Figure 5C, a dielectric layer 546 and a second metal layer 544 are deposited to form a laminate such as structure 515. In one embodiment, a second barrier layer 552 is also deposited
20 between second metal layer 544 and dielectric layer 546.

In step 640 of Figure 6, with reference again to Figure 5C, in accordance with the present invention, organic ARC 570 is applied. A photoresist 540 is then also applied.

5 In step 650 of Figure 6, with reference to Figure 5D as well, second electrode 562 is formed by removing the materials (e.g., portions of second metal layer 544, second barrier layer 552, and dielectric layer 546) not underlying photoresist 540 (Figure 5C).

10 In step 660 of Figure 6, in accordance with the present invention, the organic ARC 570 (Figure 5C) is removed using, for example, a nominal cleaning technique.

Figures 7A and 7B compares breakdown voltage and leakage current, respectively, for a MIM capacitor fabricated in accordance with one embodiment of the present invention versus a MIM capacitor fabricated according to the prior art. Figure 7A shows that the breakdown voltage for a MIM capacitor fabricated in accordance with the present invention increases and is more tightly controlled when the organic ARC is removed. Figure 7B shows that the leakage current for a MIM capacitor fabricated in accordance with the present invention can decrease and is more tightly controlled when the organic ARC is removed.

The present writing thus provides methods and systems thereof that can be used for fabricating MIM capacitors with improved electrical performance. For example, MIM capacitors fabricated according to the present writing have higher breakdown voltages and reduced leakage currents, and
5 these parameters can also be controlled within a tighter tolerance band.

The preferred embodiment of the present writing, method for forming a MIM capacitor, is thus described. While the present writing has been described in particular embodiments, it should be appreciated that the present
10 writing should not be construed as limited by such embodiments, but rather construed according to the following claims.

CLAIMS

1. A method of fabricating a metal-insulator-metal (MIM) capacitor
5 comprising the steps of:
- a) forming a first electrode of said MIM capacitor from a first metal layer in a structure;
 - b) applying an organic anti-reflective coating (ARC) to a surface of said structure;
 - 10 c) forming a second electrode of said MIM capacitor from a second metal layer; and
 - d) removing remaining organic ARC.
- 15 2. The method of Claim 1 wherein said second electrode is separated from said first electrode by a dielectric layer and said organic ARC is removed after said step of forming said second electrode is performed.
3. A method of fabricating a metal-insulator-metal (MIM) capacitor,
20 said method comprising the steps of:
- a) receiving a laminate comprising a first metal layer separated from a second metal layer by a dielectric layer;

b) removing a portion of said first metal layer and a portion of said dielectric layer to form a first electrode of said MIM capacitor and a surface of said laminate exposed by said step of removing;

5 c) applying an anti-reflective coating to said first electrode and to said surface exposed in said step b), wherein said ARC is an organic ARC;

d) removing a portion of said second metal layer to form a second electrode of said MIM capacitor; and

e) removing organic ARC remaining after said step d) is performed.

10 4. A method of fabricating a metal-insulator-metal (MIM) capacitor, said method comprising the steps of:

a) depositing a first metal layer on a substrate;

b) removing a portion of said first metal layer to form a first electrode of said MIM capacitor;

15 c) depositing a dielectric layer on said first electrode and a second metal layer on said dielectric layer to form a laminate;

d) applying an anti-reflective coating (ARC) to said laminate, wherein said ARC is an organic ARC;

20 e) removing a portion of said dielectric layer and said second metal layer to form a second electrode of said MIM; and

f) removing organic ARC remaining after said step e) is performed.

5. The method as recited in Claim 1 or 2 wherein said second metal layer is also separated from said first electrode by a barrier layer.

6. The method as recited in Claim 1 or 2 wherein said step of forming
5 said first electrode and said step of forming said second electrode comprise the
step of:
etching said first metal layer and said second metal layer.

7. The method as recited in Claim 3 further comprising the step of:
10 applying an organic ARC to said laminate prior to said step b).

8. The method as recited in Claim 1, 2, 3, or 4 wherein said organic
ARC is AR2.

15 9. The method as recited in Claim 1, 2, 3, or 4 wherein said ARC is AR3.

10. The method as recited in Claim 4 wherein said step c) further
comprises the steps of:

c1) depositing a first barrier layer between said dielectric layer and said
20 first electrode; and

c2) depositing a second barrier layer between said second metal layer
and said dielectric layer.

11. The method as recited in Claim 3 wherein said laminate further comprises a first barrier layer separating said first metal layer from said dielectric layer and a second barrier layer separating said dielectric layer from said second metal layer.

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12. The method as recited in Claim 5, 10 or 11 wherein said first metal layer and said second metal layer are comprised of aluminum and said barrier layer or layers are comprised of Ti-nitride (TiN), and wherein said dielectric layer comprises a dielectric selected from the group
10 consisting of silicon-nitride and silicon-oxy-nitride.

13. The method as recited in Claim 3 wherein said step b) and said step d) further comprise the steps of:

applying a photoresist to said laminate; and

15 removing portions of said laminate not underlying said photoresist.

14. The method as recited in Claim 4 further comprising the step of:
applying an organic ARC to said first metal layer prior to said step b).

20 15. The method as recited in Claim 3 wherein said step b) and said step e) further comprise the steps of:

applying a photoresist to said laminate; and

removing portions of said first metal layer and of said second metal layer not underlying said photoresist.

16. The method as recited in Claim 1 or 2 further comprising the step of:
applying an organic ARC to a surface of said structure prior to said step
of forming said first electrode.

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