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AN INTEGRATED CIRCUIT DEVICE AND SUB-ASSEMBLY THEREFOR

The present invention relates to integrated circuit (IC) devices, particularly IC devices utilised as memory circuits, and a sub-assembly therefor.

5 The use of IC devices particularly as components of memory circuits in computers and like applications is widespread. As pointed out in U.S. Patent Application Serial No. 224,127, a frequent source of computer error occurs when one or more of the switching circuit
10 elements of an IC are activated, with the creation of current and voltage transients. Such transients are injected into the power supply circuit or circuits as pulses, which in many instances may approach the characteristics of a functional signal. The
15 generation of such functional signal renders it

possible to obtain a false reading or transmission of inaccurate information resulting in what is know in the industry as "soft error".

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Conventionally, the transmission of pulses of error creating magnitude in the power supply circuit is avoided by placing in parallel with the circuit input a capacitor which dampens the pulses.

As noted in U.S. Patent Application Serial No. 224,127, the length of the conductor running from the external dampening capacitor to the power supply terminals of the IC device is directly related to the amount of capacitance required for effective dampening. Where long external leads are utilised between the IC device and the dampening capacitor, the amount of capacitance necessary is far greater than is the case where, as per the above-mentioned

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application, the capacitor is physically embodied within the IC device and hence the leads between power supply terminals and the capacitor may be maintained at a very short length.

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Other structures wherein attempts have been made to provide an IC device having an associated capacitor include, by way of example, U.S. Patents Nos.

4,023,198; 4,105,475; 4,168,507; 4,208,698 and
10 4,249,196 and Japanese Specification No. 53-121329.

An aim of the present invention is to provide an IC device and a lead frame sub-assembly for making the same wherein the internal power supply dampening of a plurality of power supply circuits connected to the IC
15 may be effected without the provision of external power supply dampening capacitors for a plurality of circuits.

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According to one aspect of the invention there is provided a ~~an IC~~ sub assembly ^{for an IC} comprising a lead frame

including a plurality of conductor members, a pair of
said conductors having spaced ends; a dielectric body
portion having end terminations mechanically supported
by said spaced ends and having internal spaced
5 electrodes electrically connected to said spaced ends
to form a capacitor therebetween; and a layer of
conductive material disposed on a surface of the
dielectric body portion to define a second capacitor
with an outermost one of said internal electrodes.

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According to another aspect of the invention there
is provided an integrated circuit device comprising:-

a mass of polymeric insulating material;

15 a lead frame including a plurality of conductor
members having portions disposed in coplanar alignment
and embedded within said mass, said conductor members
including contact portions extending outwardly of said
mass, a pair of said conductor members within said mass
having spaced inner terminal ends with mounting portions
20 displaced from the plane of said portions; a capacitor
having a pair of electrode terminations supported
respectively on said spaced mounting portions and in

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electrical contact therewith, said capacitor having a generally planar upper surface layer portion formed of dielectric material, the exposed face of said layer portion defining a mounting area, said capacitor including an internal outermost electrode in parallel spaced relation to said mounting area and connected to one of said electrode terminations whereby it is electrically connected to the associated mounting portion; a conductive layer member provided on said exposed face in registry with at least a part of said outermost electrode, an integrated chip of semi-conductive material provided on said conductive layer, said chip including a first and second pair of power supply inputs for connection to first and second power supplies respectively; a first pair of circuit conductor means respectively electrically connecting each of said first pair of power supply inputs with a respective one of said pair of conductor members, whereby said capacitor is shunted across said first power supply inputs, another pair of circuit conductor means electrically connecting said second pair of power supply inputs respectively with said conductive

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layer member and said one of said electrode terminations whereby there is formed in shunting relation of said second pair of power supply inputs a capacitive load defined by said outermost electrode, 5 said surface layer of said capacitor and said conductive layer.

In an embodiment of the invention, a ceramic capacitor is connected to the lead frame both 10 electrically and mechanically, the capacitor providing a mechanical mounting support for the IC chip. The ceramic capacitor is shunted across the power supply terminals using leads of minimal length. In order to provide pulsation dampening for a secondary power 15 supply circuit, a second capacitor is formed by depositing a conductive electrode layer on the outer surface of the ceramic forming the casing of the capacitor, the external conductive additional electrode layer being in registry at least in part

with the uppermost internal electrode of the capacitor. It will thus be seen that a secondary capacitor is created, with the uppermost internal electrode of the main capacitor and the externally deposited conductive layer defining the electrodes thereof and the casing or ceramic outer face of the capacitor defining the dielectric component thereof. The secondary capacitor, by virtue of the small lead length necessary to shunt the secondary power supply input of the IC device, is effective to dampen pulses in the secondary power supply not withstanding the relatively low capacitance generated.

The invention will now be described by way of example only with particular reference to the accompanying drawings wherein :

Figure 1 is a perspective view of an IC device of the invention which is externally indistinguishable from conventional devices;

Figure 2 is a magnified plan view of a section of a length of metal web material adapted to be fabricated into a lead frame for supporting the capacitor and IC chip;

Figure 3 is a fragmentary perspective

view showing an IC device of the invention at an intermediate stage of production, namely prior to encapsulation;

5 Figure 4 is a vertical sectional view through the lead frame assembly and mounted IC chip, and

Figure 5 is a schematic view of the circuit incorporating the IC chip and capacitor.

10 There is shown in Figure 2 a short section from an elongate web or band 10 of thin metal which has been punched or etched in a manner known per se to provide a plurality of blanked out areas B, the metal components M remaining between the blanked out portions B being employed to form conductors 15
15 for attachment at their innermost end to the contacts C of the circuitry formed within a semi-conductive silicon IC chip 11 known per se.

20 The finished IC chip which is conventional in appearance as is seen in Figure 1 is encapsulated within a polymeric molded mass 12 and includes a plurality of outwardly and downwardly extending conductor portions 13, the distal ends of which are, in end use, electrically connected to complementally spaced receptor sockets formed in a

printed circuit board.

Referring to Figure 2 and, as more particularly pointed out in said above-mentioned U.S. Patent application, the conductive portions 15 are initially
5 integrally formed with a central metal pallet 16 which when severed along the lines 17-17 and subsequently folded as shown in Figures 3 and 4 forms support members 18, 19 upon which may be mounted the ceramic capacitor member 20.

10 The ceramic capacitor member 20, as is conventional, is formed with end terminations 21, 22 which terminations are respectively connected to the alternate electrode layers 23, 24 of the capacitor. As seen in Figures 3 and 4 solder
15 termination portions 25, 26 mechanically and electrically secure the terminations 21, 22 respectively to the platforms 19 and 18 respectively.

As best seen from the Figures 3 and 4 the capacitor 20 includes an uppermost cover layer 27
20 which forms a portion of the encapsulation of the electrodes 23, 24. It will be understood that the layer 27 is formed of the same ceramic as the main body portion of the capacitor, and thus has a high dielectric coefficient. A conductive

layer 28 of silver or like material is deposited atop the upper ceramic layer 27, the layer 28 being in at least partial registry with the uppermost electrode 24' within the body of the capacitor.

5 It will thus be seen that the layer 24' within the capacitor and the silver or like conductive coating 28 define with the interposed ceramic layer 27 of the capacitor 20, a secondary capacitor of lower value than the capacitance provided by the capacitor 20. It will further be perceived that 10 electrode 24' is connected via termination 21 and solder connection 25 to the support member 19 leading to conductor 15 a. The capacitor formed by electrode 24', layer 27 and electrode 28 (such 15 secondary capacitance being hereinafter referred to by the reference numeral 30) may be shunted across a second lower value power supply connected to the IC device to provide dampening against the transmission of pulses through the secondary power 20 supply.

A preferred manner of effecting connection to the secondary capacitor 30 will be described hereinbelow, it being understood that alternate

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means for introducing the capacitance into the circuit will occur to those skilled in the art.

The IC chip member 11 which is formed of a semi-conductive material illustratively silicon, is bonded to the conductive layer 28 forming the upper electrode of the capacitor 30 by a conductive bonding compound layer 31 illustratively a metal filled epoxy adhesive or the like. It will thus be perceived that the electrode 28 is electrically connected to the body of the semi-conductive chip 11, or, as desired, to a circuit component formed on the chip and exposed at the lower surface of the chip and hence in electrical contact with the layer 31.

Conductor 15b forming a part of the lead frame assembly is, by way of example, representative of the negative voltage of the secondary power supply. A jumper conductor 33 connects terminal 15b with contact C', the latter being the secondary input power supply contact to the chip 11. The ground source to the internal circuit in the IC serviced by the secondary power supply is from ground conductor 15a of the lead frame assembly connected by jumper 34 to contact C''. As previously noted, contact between the electrode 24'

of the auxiliary capacitor 30 is effected to ground terminal 15 a through end termination 21 and member 19. The conductive layer 28 which forms an electrode of capacitor 30 is connected by a direct internal circuit path within the chip to contact C'. It will be thus observed that the auxiliary capacitor 30 is shunted across the secondary power supply input connected between conductor 15 b of the lead frame assembly and ground conductor 15 a. The main capacitor 20 has its end termination 22 connected to platform 18 of the lead frame assembly which has a conductor member 15 c connected to the positive side of the main power supply and by jumper 40 to positive contact C''' of the IC chip 11. The end termination 21 of the main capacitor is connected to platform 19 which has ground conductor member 15 a connected thereto. Thus the main capacitor 20 is shunted across the IC chip and the main power supply.

The remaining jumper connections are in the usual manner effected between the various lead frame conductors 15 and contacts C of the IC chip device.

After the desired connections have been effected and in the usual manner, the blank

portions S connecting adjacent conductor members 15 are severed, so as to electrically isolate the various conductor members 15. After the conductor members have been isolated and the boundary portions of the lead frame removed, the conductors are bent to the final configuration as illustrated at 13 in Figure 1 and encapsulated in polymeric mass 12.

The completed IC assembly is now ready for use. It will be recognised from the preceding description that the IC assembly incorporates a capacitor member which forms a support platform for the semi-conductor chip. The upper dielectric surface of the capacitor is used in combination with a deposited external electrode layer to define a secondary capacitance with the uppermost internal electrode layer of the capacitor. There is thus provided at no consequential increase in expense an IC chip device having two capacitive components namely a major capacitor adapted to be shunted across the main power supply terminals to the device and a secondary or minor capacitor defined by the dielectric upper layer of the capacitor, the uppermost internal electrode of the capacitor and the deposited external metallic electrode layer.

As will be apparent from the preceding description numerous variations in the described structure may be made. More particularly the principle contribution of one embodiment of, the present invention is considered to reside in an IC

5 sub assembly comprising the combination of lead frame, a ceramic capacitor embodied in the lead frame as a support for an IC chip, and in the utilisation of the upper dielectric surface of the supporting capacitor in combination with a deposited electrode deposited

10 thereon and an outermost internal electrode of the capacitor to provide two distinct capacitances for shunting two power supply inputs to prevent the transmission of switching transients throughout the circuit. The specific means of effecting

15 electrical connection to the capacitances which have been illustrated should be viewed as examples only and should not be considered limitative of the manner in which such connections may be effected. Similarly, it is within the pervue of the present invention to

20 provide additional capacitances by electrically isolating the deposited external metallic layer whereby each isolated portion of the deposited layer forms a separate capacitance with the registering

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components of the underlying uppermost electrode
of the main capacitor.

CLAIMS

1. A ~~An IC~~ ^{for an IC} sub assembly comprising a lead frame including a plurality of conductor members, a pair of
5 said conductors having spaced ends; a dielectric body portion having end terminations mechanically supported by said spaced ends and having internal spaced electrodes electrically connected to said spaced ends to form a capacitor therebetween; and a layer of conductive
10 material disposed on a surface of the dielectric body portion to define a second capacitor with an outermost one of said internal electrodes.
2. A sub assembly as claimed in claim 1 wherein an
15 integrated circuit chip member of semi-conductive material is provided on said layer of conductive material, said chip member having at least two pairs of power supply inputs and means to connect each of said pairs of input to a respective one of said capacitors to be shunted
20 thereby.
3. An integrated circuit device comprising:-
a mass of polymeric insulating material;
a lead frame including a plurality of conductor
25 members having portions disposed in coplanar alignment



and embedded within said mass, said conductor members including contact portions extending outwardly of said mass, a pair of said conductor members within said mass having spaced inner terminal ends with mounting portions displaced from the plane of said portions; a capacitor having a pair of electrode terminations supported respectively on said spaced mounting portions and in electrical contact therewith, said capacitor having a generally planar upper surface layer portion formed of dielectric material, the exposed face of said layer portion defining a mounting area, said capacitor including an internal outermost electrode in parallel spaced relation to said mounting area and connected to one of said electrode terminations whereby it is electrically connected to the associated mounting portion; a conductive layer member provided on said exposed face in registry with at least a part of said outermost electrode, an integrated chip of semi-conductive material provided on said conductive layer, said chip including a first and second pair of power supply inputs for connection to first and second power supplies respectively; a first pair of circuit conductor means respectively electrically connecting each of said first pair of power supply inputs with a respective one of said pair of conductor members, whereby said capacitor is



shunted across said first power supply inputs, another pair of circuit conductor means electrically connecting said second pair of power supply inputs respectively with said conductive layer member and said one of said electrode terminations whereby there is formed in shunting relation of said second pair of power supply inputs a capacitive load defined by said outermost electrode, said surface layer of said capacitor and said conductive layer.

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4. A ^{for an IC} ~~An IC~~ sub assembly substantially as herein described with reference to the accompanying drawings.

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5. An integrated circuit device substantially as herein described with reference to the accompanying drawings.

