

ABSTRACT

A non-volatile memory device includes a first semiconductor layer and a second semiconductor layer arranged in the vertical direction. A first semiconductor layer includes a plurality of memory cells, and a plurality of metal lines extending in a first direction, and including first bit lines, second bit lines, and a common source line tapping wire between the first bit lines and the second bit lines. A second semiconductor layer includes a page buffer circuit connected to the first bit lines and the second bit lines, and the page buffer circuit includes first transistors arranged below the first bit lines and electrically connected to the first bit lines, second transistors arranged below the second bit lines and electrically connected to the second bit lines, and a first guard ring arranged below and overlapped the common source line tapping wire in the vertical direction and extending in the first direction.

FIG. 10