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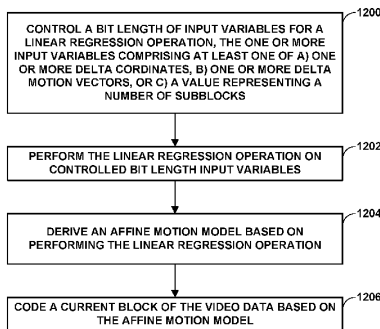
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(54) Title: BIT-LENGTH CONTROL FOR LINEAR REGRESSION-BASED AFFINE MERGE CANDIDATE DERIVATION



(57) Abstract: An example device for coding video data includes memory configured to store the video data and one or more processors communicatively coupled to the memory. The one or more processors are configured to reduce a bit length of one or more input variables for a linear regression operation to generate one or more reduced bit length input variables, the input variables including at least one of a) one or more delta coordinates, b) one or more delta motion vectors, or c) a value representing a number of subblocks. The one or more processors are configured to perform the linear regression operation and derive an affine motion model based on the performing the linear regression on the one or more reduced bit length input variables. The one or more processors are configured to code a current block of the video data based on the affine motion model.

FIG. 12

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