

REGISTRATION AND SCANNING IN A ROAMING SELECTIVE CALL SYSTEM

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FIELD OF THE INVENTION

The present invention relates generally to the field of selective call communications, and more particularly to a method and apparatus in a selective call system for prioritizing channels available to communicate with a roaming communication receiver and for scanning selective call system channels in response thereto.

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BACKGROUND OF THE INVENTION

A selective call system provides transmission of selective call messages from a message originator to a communication receiver such as a selective call receiver. The originator contacts a selective call terminal and provides the content of the message and information identifying the intended receiver thereto. The selective call terminal encodes the message into one of several known protocols, such as the POCSAG signaling code or the FLEX™ high speed paging protocol. In addition, the terminal appends an address assigned to the communication receiver to the message. The address and message are then modulated onto a selective call signal and transmitted from the selective call terminal. When the communication receiver recognizes its address within the selective call signal, the message therefollowing is demodulated and decoded.

As communication receiver users travel more, it is preferable to have a communication receiver which can operate in one or more selective call systems, or roam among selective call systems. Many techniques for frequency scanning are known, and these could be implemented in a communication receiver. However, a communication receiver while monitoring one channel could

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miss a message intended for that communication receiver broadcast on another channel. This is particularly true in overlap coverage areas where the communication receiver is receiving selective call signals from more than one system.

5 Thus what is needed is a registration and scanning process which would improve the communication receivers chance of receiving messages intended for it.

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SUMMARY OF THE INVENTION

In accordance with the objects of the present invention, there is provided communication receiver comprising:

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a memory for storing a plurality of channel identifiers corresponding to a plurality of channels and for storing at least one address assigned to the communication receiver;

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a frequency synthesizer for generating a channel signal corresponding to one of said plurality of channels; receiver circuitry coupled to the frequency synthesizer for receiving and demodulating selective call signals on one of
25 said plurality of channels in response to the channel signal;

a decoder coupled to said receiver circuitry for decoding the selective call signals to generate selective
30 call messages;

a controller coupled to the memory and the decoder for comparing the at least one address to address information within the selective call messages to determine whether the
35 selective call messages are intended for the communication receiver;

wherein the controller further determines whether the selective call messages are registration messages comprising channel registration information intended for the communication receiver and, if the selective call
5 messages are registration messages, stores the channel registration information in the memory in association with one of the plurality of channel identifiers; and

wherein the controller is coupled to the frequency
10 synthesizer and generates a channel synthesizing signal corresponding to one of the plurality of channel identifiers to supply to the frequency synthesizer and the frequency synthesizer generates the channel signal in response thereto, the one of the plurality of channel
15 identifiers determined in response to the channel registration information associated with the one of the plurality of channel identifiers.

Suitably, the communication receiver may further
20 comprise a signal strength detector coupled to the receiver circuitry and the controller for providing the controller a channel strength signal associated with the one of the plurality of channels being received in response to determining whether the receiver is receiving a signal
25 having a strength above a predetermined threshold, wherein the controller generates a channel synthesizing signal corresponding to one of the plurality of channel identifiers to supply to the frequency synthesizer and the frequency synthesizer generates the channel signal in
30 response thereto, the one of the plurality of channel identifiers determined in response to the channel registration information and the channel strength signal associated with the one of the plurality of channel identifiers.

According to another aspect of this invention there is provided a communication receiver comprising:

a controller;

5 a receiver means for both receiving messages and scanning to detect transmitted channel frequencies;

frequency generating means coupled to said controller and said receiver means;

wherein said controller is adapted to control said
10 frequency generating means to thereby effect scanning of channel frequencies by said receiver to determine a channel frequency for monitoring messages, said scanning being dependent upon priorities associated with said
15 channel frequencies, and wherein at least some of said channel frequencies have a priority dependent upon one or more received registration messages identifying a change of one or more said priorities.

Suitably, said communication receiver may be adapted
20 such that at least some of said channels have a default priority that is changeable by said one or more received registration messages.

Suitably, said communication receiver may be adapted
25 to change a priority of one or more channels at a predetermined time. Suitably, said communication receiver may be adapted to allow a priority of a changed said one or more channels to last for a predetermined time before returning to an associated default priority.

30 Preferably, said communication receiver can be adapted to scan said channels in an order associated with said priorities.



Suitably, said communication receiver may have a threshold level detection means for detecting if a received channel strength is above a threshold level.

5 Preferably, said communication receiver may be adapted to control said frequency generating means to scan channels of a higher priority than said channel frequency for monitoring messages.

10 According to another aspect of this invention there is provided a method for identifying channels available to communicate with a communication receiver, said method comprising the steps of:

15 receiving a registration message comprising channel identification data identifying one or more priority channels and timing information;

20 changing priorities of at least some of said channels at a time dependent on said timing information;

 scanning said channels in accordance with said priorities to determine a channel for receiving message;

25 monitoring said channel.

 Preferably, the the step of scanning may be characterised by scanning channels of a higher priority than said channel.

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 Preferably, said step of scanning may also include the step of comparing channel strengths against a threshold value.

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BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is an electrical block diagram of a data transmission system in accordance with the preferred
5 embodiment of the present invention.

FIG. 2 is an electrical block diagram of a paging terminal and transmitter for processing and transmitting message information in accordance with the preferred
10 embodiment of the present invention.

FIGS. 3 and 4 are flow charts of the operation of the terminal of FIG. 2 in accordance with the preferred
15 embodiment of the present invention.

FIGS. 5, 6, and 7 are timing diagrams illustrating the transmission format of the signaling protocol utilized in accordance with the preferred embodiment of the present
20 invention.

FIGS. 8 and 9 are timing diagrams illustrating the synchronization signals utilized in accordance with the preferred embodiment of the present invention.

FIG. 10 is a diagram of a registration message to a communication receiver for registration confirmation in accordance with the preferred embodiment of the present
25 invention.

FIG. 11 is an electrical block diagram of a data communication receiver in accordance with the preferred
30 embodiment of the present invention.

FIG. 12 is an electrical block diagram of a threshold
35 level extraction circuit utilized in the data communication receiver of FIG. 11.

FIG. 13 is an electrical block diagram of a 4-level decoder utilized in the data communication receiver of FIG. 11.

5 FIG. 14 is an electrical block diagram of a symbol synchronizer utilized in the data communication receiver of FIG. 11.

10 FIG. 15 is an electrical block diagram of a 4-level to binary converter utilized in the data communication receiver of FIG. 11.

15 FIG. 16 is an electrical block diagram of a synchronization correlator utilized in the data communication receiver of FIG. 11.

20 FIG. 17 is an electrical block diagram of a phase timing generator utilized in the data communication receiver of FIG. 11.

25 FIG. 18, is a flow chart illustrating synchronization of the data communication receiver to system messages in accordance with the preferred embodiment of the present invention.

FIG. 19 is a flow chart illustrating processing of the registration message of FIG. 10.

30 FIG. 20 is a flow chart further illustrating processing of the registration message of FIG. 10.

35 FIGS. 21 to 23 are flow charts illustrating a method for identifying channels that are available to communicate with the data communication receiver of FIG. 11.

FIG. 24 illustrates a scan list in accordance with the preferred embodiment of the present invention.

FIG. 25 illustrates a status table in accordance with
5 the preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

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FIG. 1 is an electrical block diagram of a data transmission system 100, such as a paging system, in accordance with the preferred embodiment of the present invention. In such a data transmission system 100,
15 messages originating either from a phone or from a message entry device, such as an alphanumeric data terminal, are routed through the public switched telephone network (PSTN) to a paging terminal 102 which processes the numeric or alphanumeric message information for transmission by one or
20 more transmitters 104 provided within the system. When multiple transmitters are utilized, the transmitters 104 preferably simulcast transmit the message information to data communication receivers 106. Processing of the numeric and alphanumeric information by the paging terminal
25 102, and the protocol utilized for the transmission of the messages is described below.

FIG. 2 is an electrical block diagram of the paging terminal 102 utilized for processing and controlling the
30 transmission of the message information in accordance with the preferred embodiment of the present invention. Short messages, such as tone-only and numeric messages which can be readily entered using a Touch-Tone telephone are coupled to the paging terminal 102 through a telephone interface
35 202 in a manner well known in the art. Longer messages, such as alphanumeric messages which require the use of a data entry device are coupled to the paging terminal 102 through a modem 206 using any of a number of well known

modem transmission protocols. When a call to place a message is received, a controller 204 handles the processing of the message.

5 The controller 204 is preferably a microcomputer, such as an MC68000, which is manufactured by Motorola Inc., or equivalent, and which runs various pre-programmed routines for controlling such terminal operations as voice prompts to direct the caller to enter the message, or the
10 handshaking protocol to enable reception of messages from a data entry device. When a call is received, the controller 204 references information stored in the subscriber database 208 to determine how the message being received is to be processed. The subscriber database 208 includes, but
15 is not limited to such information as addresses assigned to the data communication receiver, message type associated with the address, and information related to the status of the data communication receiver, such as active or inactive for failure to pay the bill. A data entry terminal 240 is
20 provided which couples to the controller 204, and which is used for such purposes as entry, updating and deleting of information stored in the subscriber database 208, for monitoring system performance, and for obtaining such information as billing information.

25 The subscriber database 208 also includes such information as to what transmission frame and to what transmission phase the data communication receiver is assigned, as will be described in further detail below.

30 In accordance with the present invention, the paging terminal 102 further comprises a registration memory 209 for storing a listing of addresses indicating receivers registered to the data transmission system 100. The
35 receivers are normally registered to the data transmission system 100, and their appearance in the registration memory

209 indicates that they are also temporarily registered to another system (or will be temporarily registered to another system).

5 The preferred embodiment of the present invention stores along with each address, an indication of the other system to which the receiver is registered known as a system for registration (SYS), a time start when (or time interval when) the receiver becomes registered (TS) and the
10 time registered interval during which the receiver will be registered (TR). The TS and TR indicate when the receiver will be temporarily registered to another system. The controller 204 is coupled to the memory 209 to forward messages to the appropriate systems (SYS) when the receiver
15 is temporarily registered to that system as described in further detail below.

 The received message is stored in an active page file 210 which stores the messages in queues according to the
20 transmission phase assigned to the data communication receiver. Longer data messages may require fragmentation of the message into several messages for transmission. The several messages are stored in the active page file 210 for transmission in a manner which allows the receiver to
25 reconstruct the long message from the several messages. In the preferred embodiment of the present invention, four phase queues are provided in the active page file 210. The active page file 210 is preferably a dual port, first in first out random access memory, although it will be
30 appreciated that other random access memory devices, such as hard disk drives, can be utilized as well.

 Periodically the message information stored in each of the phase queues is recovered from the active page file 210
35 under control of controller 204 using timing information such as provided by a real time clock 214, or other

suitable timing source. The recovered message information from each phase queue is sorted by frame number and is then organized by address, message information, and any other information required for transmission, and then batched
5 into frames based upon message size by frame batcher 212. The batched frame information for each phase queue is coupled to frame message buffers 216 which temporarily store the batched frame information until a time for further processing and transmission. Frames are batched in
10 numeric sequence, so that while a current frame is being transmitted, the next frame to be transmitted is in the frame message buffer 216, and the next frame thereafter is being retrieved and batched.

15 At the appropriate time, the batched frame information stored in the frame message buffer 216 is transferred to the frame message encoder 218, again maintaining the phase queue relationship. The frame message encoder 218 encodes the address and message information into address and
20 message code words required for transmission, as will be described below. The encoded address and message code words are ordered into blocks and then coupled to a frame message interleaver 220 which interleaves preferably eight code words at a time for transmission in a manner well
25 known in the art. The interleaved code words from each frame message interleaver 220 are then serially transferred to a phase multiplexer 221, which multiplexes the message information on a bit by bit basis into a serial data stream by transmission phase. The controller 204 next enables a
30 frame sync generator 222 which generates the synchronization code which is transmitted at the start of each frame transmission.

The synchronization code is multiplexed with address
35 and message information under the control of controller 204 by serial data splicer 224, and generates therefrom a

message stream which is properly formatted for transmission. The message stream is next coupled to a transmitter controller 226, which under the control of controller 204 transmits the message stream over a
5 distribution channel 228. The distribution channel 228 may be any of a number of well known distribution channel types, such as wire line, an RF or microwave distribution channel, or a satellite distribution link. The distributed message stream is transferred to one or more transmitter
10 stations 104, depending upon the size of the communication system. The message stream is first transferred into a dual port buffer 230 which temporarily stores the message stream prior to transmission. At an appropriate time determined by timing and control circuit 232, the message
15 stream is recovered from the dual port buffer 230 and coupled to the input of preferably a 4-level FSK modulator 234. The modulated message stream is then coupled to the transmitter 236 for transmission via antenna 238.

20 FIGS. 3 and 4 are flow charts of the registration routine of the controller 204 in accordance with the preferred embodiment of the present invention. The registration routine 300 begins by examining the input from the telephone interface 202 and the modem 206 to determine
25 if a registration request has been received at step 302.

When a registration request is received at step 302, the controller 204 at a request step 304 requests for the caller a pager address (ADDR), a time start (TS), a time
30 registered interval (TR), and a system for registration (SYS). When the requested information is received at step 306, it is stored at step 308 in the registration memory 209 without overwriting any information that hasn't been used. If the requested information is not received at step
35 306 in a timely manner, processing returns to check if a registration request has been received at step 302. After

storing at step 308 the requested information in the registration memory 209, the requested information (i.e., registration info) is forwarded to the other system at step 310 along with an ID of the data transmission system 100.

5 The systems are coupled together in a manner well known in the art, such as through the PSTN, which facilitates the passing of information from one system to another. After forwarding the information steps 318, 320 and 322 are effected as described below. Processing then determines

10 whether selective call information has been received at step 312 via the phone 202 or the modem 206.

If no selective call information is received at step 312, processing will continue to look for a registration

15 request at step 302, registration information from another system at step 314 or selective call information at step 312. When registration information is received at step 314 from another system, the pertinent information (ADDR, SYS, TS, TR) is stored at step 316 in the registration memory

20 209 and a registration confirmation message is composed at step 318 for broadcast to the appropriate receiver. When the frame assigned to the receiver is being transmitted at step 320, the composed registration confirmation message is stored at step 322 in the active page file 210 along with

25 other paging messages. The controller 204 retrieves each message from the active page file 210 and processes it for transmission as described above.

If instead of a registration request at step 302 or

30 registration info from another system at step 314, selective call information is received at step 312, the selective call message routine 324 is performed as shown in FIG. 4. Controller 204 determines the frame assigned for the selective call message at step 402. The selective call

35 message is then composed at step 404 and stored into an active page file at step 406. When the assigned frame is

being transmitted at step 408, controller 204 stores at step 410 the selective call message in the active page file 210.

5 In accordance with the present invention, the controller 204 also examines the registration memory 209 to determine if the pager address is present at step 412. If the pager address is not in the registration memory at step 412, the routine goes to step 414 which returns to step 302
10 to await the next information received from the phone 202 or the modem 204. If the pager address is found at step 412, the real time clock is compared with the time information stored in association with the pager address and it is determined whether the pager is not yet
15 registered at step 416 or the registration time has expired at step 418. If either condition is true, the routine goes to step 414 which returns to step 302 to await the next information received from the phone 202 or the modem 204. If it is determined that the pager is
20 registered to another system at steps 416 or 418, the selective call information is forwarded at step 420 to the system indicated (SYS) in the registration memory 209 and then returns at step 414 to the registration routine of FIG.3.

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 Thus, it can be seen that in accordance with the preferred embodiment of the present invention, registration information is passed to the terminal through PSTN interfaces and a registration confirmation message is
30 received by the pager to confirm the registration. Then, when the pager is registered to the other system, selective call messages intended for that pager are broadcast in the data transmission system 100 and appropriate information is also forwarded to the registered system for broadcast
35 therein.

FIGs. 5, 6 and 7 are timing diagrams illustrating the transmission format of the signaling protocol utilized in accordance with the preferred embodiment of the present invention. Though the present invention is useful in several known protocols, the preferred embodiment utilizes the signaling protocol described below for dynamic group calling in accordance with the present invention resulting in substantial air time savings for the service provider. As shown in FIG. 5, the signaling protocol enables message transmission to data communication receivers, such as pagers, assigned to one or more of 128 frames which are labeled frame zero through frame 127. It then will be appreciated that the actual number of frames provided within the signaling protocol can be greater or less than described above. The greater the number of frames utilized, the greater the battery life that may be provided to the data communication receivers operating within the system. The fewer the number of frames utilized, the more often messages can be queued and delivered to the data communication receivers assigned to any particular frame, thereby reducing the latency, or time required to deliver messages.

As shown in FIG. 6, the frames comprise a synchronization code (sync) followed preferably by a block info field, an address field, a message field and idle blocks. As shown in FIG. 7, each block information field comprises information indicating the start of the address field (AF), start of the vector field (VF), a simulcast system ID (SSID) and a frame offset value (FOV).

FIGs. 8 and 9 are timing diagrams illustrating the synchronization code utilized in accordance with the preferred embodiment of the present invention. In particular, as shown in FIG. 8, the synchronization code comprises preferably three parts, a first synchronization

code (sync 1), a frame information code word (frame info) and a second synchronization code (sync 2). As shown in FIG. 9, the first synchronization code comprises first and third portions, labeled bit sync 1 and BS1, which are alternating one,zero bit patterns which provides bit synchronization, and second and fourth portions, labeled "A" and its complement "A bar", which provide frame synchronization. The second and fourth portions are preferably single 32,21 BCH code words which are predefined to provide high code word correlation reliability, and which are also used to indicate the data bit rate at which addresses and messages are transmitted. The table below defines the data bit rates which are used in conjunction with the signaling protocol.

15	<u>Bit Rate</u>	<u>"A" Value</u>
	1600 bps	A1 and A1 bar
	3200 bps	A2 and A2 bar
	6400 bps	A3 and A3 bar
20	Not defined	A4 and A4 bar

As shown in the table above, three data bit rates are predefined for address and message transmission, although it will be appreciated that more or less data bit rates can be predefined as well, depending upon the system requirements. A fourth "A" value is also predefined for future use. The frame information code word is preferably a single 32,21 BCH code word which includes within the data portion a predetermined number of bits reserved to identify the frame number, such as 7 bits encoded to define frame number zero to frame number 127.

The structure of the second synchronization code is preferably similar to that of the first synchronization code described above. However, unlike the first synchronization code which is preferably transmitted at a fixed data symbol rate, such as 1600 bps (bits per second),

the second synchronization code is transmitted at the data symbol rate at which the address and messages are to be transmitted in any given frame. Consequently, the second synchronization code allows the data communication receiver to obtain "fine" bit and frame synchronization at the frame transmission data bit rate.

In summary the signaling protocol utilized with the preferred embodiment of the present invention comprises 128 frames which include a predetermined synchronization code followed by a block information field, an address field, a message field and idle blocks. The synchronization code enables identification of the data transmission rate, and insures synchronization by the data communication receiver with the data code words transmitted at the various transmission rates.

FIG. 10 is a diagram of a registration message 1009 composed for transmission to the data communication receiver 106 (ie a selective call receiver) to confirm registration. The registration message comprises an address 1010 indicating the receiver intended to receive the paging message, a registration message identifier 1030 (in the FLEXTM protocol this would comprise a secure vector and registration opcode) and a registration data frame 1020. Each message can contain, for example in the FLEXTM protocol, up to eight data frames 1020. When the data communication receiver detects the address 1010, registration message identifier 1030 is then read to determine the message type and if appropriate the data frames 1020 are then received and decoded. Each data frame 1020 comprises information identifying a system identifier and associated channel desired to be registered 1040 (system channel identifier), channel frequency 1045 of the associated system channel identifier 1040, a wait time (TS) 1050 before the required registration commences, and a length of time the receiver requires to be registered known

as a registration time (TR) 1060. Further, in this embodiment System channel identifier 1040 can be either an Network Identifier (NID) or System Simulcast Identifier (SSID) as defined in the FLEXTM protocol.

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When the paging messages are composed 318 (FIG. 3), the message portion is encoded to define the information 1030, 1040, 1050, 1060. The registration message identification code 1030 identifies the message as a
10 registration confirmation message. The system channel identifier 1040, wait time (TS) 1050, and time registered (TR) 1060 are then stored in the data communication receiver for handling as described below. Further, each of the data frames 1020 to be transmitted are sequentially
15 ordered depending on wait times (TS), thereby the data frames 1020 with the shortest wait times (TS) are ordered first.

FIG. 11 is an electrical block diagram of the data
20 communication receiver 106 in accordance with the preferred embodiment of the present invention. The heart of the data communication receiver 106 is a controller 1116, which is preferably implemented using an MC68HC11 microcomputer, such as manufactured by Motorola, Inc. The controller
25 1116, receives and processes inputs from a number of peripheral circuits, as shown in FIG. 11, and controls the operation and interaction of the peripheral circuits using software subroutines. The use of a microcomputer controller for processing and control functions is well
30 known to one of ordinary skill in the art.

The data communication receiver 106 is capable of receiving address, control and message information, hereafter called "data" which is modulated using preferably
35 2-level and 4-level frequency modulation techniques. The transmitted data is intercepted by an antenna 1102 which

couples to the input of a receiver section 1104. Receiver section 1104 processes the received data in a manner well known in the art, providing at the output an analog 4-level recovered data signal, hereafter called a recovered data signal. The recovered data signal is coupled to one input of a threshold level extraction circuit 1108, and to an input of a 4-level decoder 1110.

The threshold level extraction circuit 1108 is best understood by referring to FIG. 12, and as shown comprises two clocked level detector circuits 1202, 1204 which have as inputs the recovered data signal. Level detector 1202 detects the peak signal amplitude value and provides a high peak threshold signal which is proportional to the detected peak signal amplitude value, while level detector 1204 detects the valley signal amplitude value and provides a valley threshold signal which is proportional to the detected valley signal amplitude value of the recovered data signal. The level detectors 1202, 1204 signal outputs are coupled to terminals of resistors 1206, 1212, respectively. The opposite resistor terminals 1206, 1212 provide the high threshold output signal (Hi), and the low threshold output signal (Lo), respectively. The opposite resistor terminals 1206, 1212 are also coupled to terminals of resistors 1208, 1210, respectively. The opposite resistor 1208, 1210 terminals are coupled together to form a resistive divider which provides an average threshold output signal (Avg) which is proportional to the average value of the recovered data signal. Resistors 1206, 1212 have resistor values preferably of $1R$, while resistors 1208, 1210 have resistor values preferably of $2R$, realizing threshold output signal values of 17%, 50% and 83%, and which are utilized to enable decoding the 4-level data signals as will be described below.

When power is initially applied to the receiver portion, as when the data communication receiver is first turned on, a clock rate selector 1214 is preset through a control input (center sample) to select a 128X clock, i.e.

5 a clock having a frequency equivalent to 128 times the slowest data bit rate, which as described above is 1600 bps. The 128X clock is generated by 128X clock generator 1144, as shown in FIG. 11, which is preferably a crystal controlled oscillator operating at 204.8 KHz (kilohertz).

10 The output of the 128X clock generator 1144 couples to an input of frequency divider 1146 which divides the output frequency by two to generate a 64X clock at 102.4 KHz. Returning to FIG. 12, the 128X clock allows the level detectors 1202, 1204 to synchronously detect in a very

15 short period of time the peak and valley signal amplitude values, and to therefore generate the low (Lo), average (Avg) and high (Hi) threshold output signal values required for modulation decoding. After symbol synchronization is achieved with the synchronization signal, as will be

20 described below, the controller 1116 generates a second control signal (Center Sample) to enable selection of a 1X symbol clock which is generated by symbol synchronizer 1112 as shown in FIG. 11.

25 Returning to FIG. 11, the 4-level decoder 1110 operation is best understood by referring to FIG. 13. As shown, the 4-level decoder 1110 comprises three voltage comparators 1310, 1320, 1330 and a symbol decoder 1340. The recovered data signal couples to an input of the three

30 comparators 1310, 1320, 1330. The high threshold output signal (Hi) couples to the second input of comparator 1310, the average threshold output signal (Avg) couples to the second input of comparator 1320, and the low threshold output signal (Lo) couples to the second input of

35 comparator 1330. The outputs of the three comparators 1310, 1320, 1330 couple to inputs of symbol decoder 1340.

The symbol decoder 1340 decodes the inputs according to the table provided below.

5	Threshold					Output	
	Hi	Avg	Lo	MSB	LSB		
	RC _{in} <	RC _{in} <		RC _{in} <		0	0
	RC _{in} <	RC _{in} <		RC _{in} >		0	1
	RC _{in} <	RC _{in} >		RC _{in} >		1	1
	RC _{in} >	RC _{in} >		RC _{in} >		1	0

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As shown in the table above, when the recovered data signal (RC_{in}) is less than all three threshold values, the symbol generated is 00 (MSB = 0, LSB = 0). Thereafter, as each of the three threshold values is exceeded, a different
15 symbol is generated, as shown in the table above.

The MSB output from the 4-level decoder 1110 is coupled to an input of the symbol synchronizer 1112 and provides a recovered data input generated by detecting the
20 zero crossings in the 4-level recovered data signal. The positive level of the recovered data input represents the two positive deviation excursions of the analog 4-level recovered data signal above the average threshold output signal, and the negative level represents the two negative
25 deviation excursions of the analog 4-level recovered data signal below the average threshold output signal.

The operation of the symbol synchronizer 1112 is best understood by referring to FIG. 14. The 64X clock at 102.4
30 KHz which is generated by frequency divider 1146, is coupled to an input of a 32X rate selector 1420. The 32X rate selector 1420 is preferably a divider which provides selective division by one or two to generate a sample clock which is thirty-two times the symbol transmission rate. A
35 control signal (1600/3200) is coupled to a second input of the 32X rate selector 1420, and is used to select the

sample clock rate for symbol transmission rates of 1600 and 3200 symbols per second.

5 The selected sample clock is coupled to an input of
32X data oversampler 1410 which samples the recovered data
signal (MSB) at thirty-two samples per symbol. The symbol
samples are coupled to an input of a data edge detector
1430 which generates an output pulse when a symbol edge is
detected. The sample clock is also coupled to an input of
10 a divide-by-16/32 circuit 1440 which is utilized to
generate 1X and 2X symbol clocks synchronized to the
recovered data signal. The divided-by-16/32 circuit 1440 is
preferably an up/down counter.

15 When the data edge detector 1430 detects a symbol
edge, a pulse is generated which is gated by AND gate 1450
with the current count of divide-by-16/32 circuit 1440.
Concurrently, a pulse is generated by the data edge
detector 1430 which is also coupled to an input of the
20 divide-by-16/32 circuit 1440. When the pulse coupled to
the input of AND gate 1450 arrives before the generation of
a count of thirty-two by the divide-by-16/32 circuit 1440,
the output generated by AND gate 1450 causes the count of
divide-by-16/32 circuit 1440 to be advanced by one count in
25 response to the pulse which is coupled to the input of
divide-by-16/32 circuit 1440 from the data edge detector
1430, and when the pulse coupled to the input of AND gate
1450 arrives after the generation of a count of thirty-two
by the divide-by-16/32 circuit 1440, the output generated
30 by AND gate 1450 causes the count of divide-by-16/32
circuit 1440 to be retarded by one count in response to the
pulse which is coupled to the input of divide-by-16/32
circuit 1440 from the data edge detector 1430, thereby
enabling the synchronization of the 1X and 2X symbol clocks
35 with the recovered data signal. The symbol clock rates
generated are best understood from the table below.

	InputControl		Rate		Rate	2X	1X
	Clock Input		Selector		Selector	Symbol	Symbol
			Divide		Output	Clock	Clock
5	(Relative)	(sps)	Ratio			(bps)	(bps)
	64X	1600	by	2	32X	3200	1600
	64X	3200	by	1	64X	6400	3200

As shown in the table above, the 1X and 2X symbol
 10 clocks are generated at 1600, 3200 and 6400 bits per second
 and are synchronized with the recovered data signal.

The 4-level binary converter 1114 is best understood
 by referring to FIG. 15. The 1X symbol clock is coupled to
 15 a first clock input of a clock rate selector 1510. A 2X
 symbol clock also couples to a second clock input of the
 clock rate selector 1510. The symbol output signals (MSB,
 LSB) are coupled to inputs of an input data selector 1530.
 A selector signal (2L/4L) is coupled to a selector input of
 20 the clock rate selector 1510 and the selector input of the
 input data selector 1530, and provides control of the
 conversion of the symbol output signals as either 2-level
 FSK data, or 4-level FSK data. When the 2-level FSK data
 25 conversion (2L) is selected, only the MSB output is
 selected which is coupled to the input of a parallel to
 serial converter 1520. The 1X clock input is selected by
 clock rate selector 1510 which results in a single bit
 binary data stream to be generated at the output of the
 parallel to serial converter 1520. When the 4-level FSK
 30 data conversion (4L) is selected, both the LSB and MSB
 outputs are selected which are coupled to the inputs of the
 parallel to serial converter 1520. The 2X clock input is
 selected by clock rate selector 1510 which results in a
 serial two bit binary data stream to be generated at 2X the
 35 symbol rate, which is provided at the output of the
 parallel to serial converter 1520.

Returning to FIG. 11, the serial binary data stream generated by the 4-level to binary converter 1114 is coupled to inputs of a synchronization word correlator 1118 and a demultiplexer 1120. The synchronization word correlator is best understood with reference to FIG. 16. Predetermined "A" word synchronization patterns are recovered by the controller 1116 from a code memory 1122 and are coupled to an "A" word correlator 1610. When the synchronization pattern received matches one of the predetermined "A" word synchronization patterns within an acceptable margin of error, an "A" or "A-bar" output is generated and is coupled to controller 1116. The particular "A" or "A-bar" word synchronization pattern correlated provides frame synchronization to the start of the frame ID word, and also defines the data bit rate of the message to follow, as was previously described.

The serial binary data stream is also coupled to an input of the frame word decoder 1620 which decodes the frame word and provides an indication of the frame number currently being received by the controller 1116. During sync acquisition, such as following initial receiver turn-on, power is supplied to the receiver portion by battery saver circuit 1148, shown in FIG. 11, which enabled the reception of the "A" synchronization word, as described above, and which continues to be supplied to enable processing of the remainder of the synchronization code.

The controller 1116 compares the frame number currently being received with a list of assigned frame numbers stored in code memory 1122. After receipt of a temporary assignment of a group call address in accordance with the present invention, the frame assigned for receipt of the group call message becomes an assigned frame of the receiver temporarily, and is accessed along with the list of assigned frame numbers stored in the code memory 1122 as described hereinbelow. Should the currently received frame

number differ from an assigned frame numbers, the controller 1116 generates a battery saving signal which is coupled to an input of battery saver circuit 1148, suspending the supply of power to the receiver portion.

5 The supply of power will be suspended until the next frame assigned to the receiver, at which time a battery saver signal is generated by the controller 1116 which is coupled to the battery saving circuit 1148 to enable the supply of power to the receiver portion to enable reception of the

10 assigned frame. As the receiver is a roaming receiver, the controller 1116 supplies a signal to a frequency synthesizer 1149 which is coupled to the receiver 1104 to allow the receiver to receive signals on multiple channels under the control of the frequency synthesizer 1149.

15

Returning to the operation of the synchronization correlator shown in FIG. 16, a predetermined "C" word synchronization pattern is recovered by the controller 1116 from a code memory 1122 and is coupled to a "C" word

20 correlator 1630. When the synchronization pattern received matches the predetermined "C" word synchronization pattern with an acceptable margin of error, a "C" or "C-bar" output is generated which is coupled to controller 1116. The particular "C" or "C-bar" synchronization word correlated

25 provides "fine" frame synchronization to the start of the data portion of the frame.

Returning to FIG. 11, the start of the actual data portion is established by the controller 1116 generating a

30 block start signal (Blk Start) which is coupled to inputs of a word de-interleaver 1124 and a data recovery timing circuit 1126. The data recovery timing circuit 1126 is best understood by referring to FIG. 17. A control signal ($2L / 4L$) is coupled to an input of clock rate selector

35 1710 which selects either 1X or 2X symbol clock inputs. The selected symbol clock is coupled to the input of a

phase generator 1730 which is preferably a clocked ring counter which is clocked to generate four phase output signals (Ø1-Ø4). A block start signal is also coupled to an input of the phase generator 1730, and is used to hold
5 the ring counter in a predetermined phase until the actual decoding of the message information is to begin. When the block start signal releases the phase generator 1730, the phase generator 1730 begins generating clocked phase signals which are synchronized with the incoming message
10 symbols.

Referring back to FIG. 11, the clocked phase signal outputs are coupled to inputs of a phase selector 1128. During operation, the controller 1116 recovers from the
15 code memory 1122, the transmission phase number to which the data communication receiver is assigned. The phase number is transferred to the phase select output (Ø Select) of the controller 1116 and is coupled to an input of phase selector 1128. A phase clock, corresponding to the
20 transmission phase assigned, is provided at the output of the phase selector 1128 and is coupled to clock inputs of the demultiplexer 1120, block de-interleaver 1124, and address and data decoders 1130 and 1132, respectively. The demultiplexer 1120 is used to select the binary bits
25 associated with the assigned transmission phase which are then coupled to the input of block de-interleaver 1124, and clocked into the de-interleaver array on each corresponding phase clock. The de-interleaver array is an 8x32 bit array which de-interleaves eight interleaved address, control or
30 message code words, corresponding to one transmission block. The de-interleaved address code words are coupled to the input of address correlator 1130. The controller 1116 recovers the address patterns assigned to the data communication receiver from the code memory 1122, and
35 couples the patterns to a second input of the address correlator 1130.

A table of the predetermined group call addresses (GCA0-GCA7) may be stored in the code memory 1122. The controller 1116 would then additionally recover the address patterns of any activated group call addresses for provision to the second input of the address correlator 1130. When any of the de-interleaved address code words matches any of the address patterns assigned to the data communication receiver within an acceptable margin of error, the message information associated with the address is then decoded by the data decoder 1132 and stored in a message memory 1150 in a manner well known to one of ordinary skill in the art. Following the storage of the message information, a sensible alert signal is generated by the controller 1116. The sensible alert signal is preferably an audible alert signal, although it will be appreciated that other sensible alert signals, such as tactile alert signals, and visual alert signals can be generated as well. The audible alert signal is coupled by the controller 1116 to an alert driver 1134 which is used to drive an audible alerting device, such as a speaker or a transducer 1136. The user can override the alert signal generation through the use of user input controls 1138 in a manner well known in the art.

25

Following the detection of an address associated with the data communication receiver, the message information is coupled to the input of data decoder 1132 which decodes the encoded message information into preferably a BCD or ASCII format suitable for storage and subsequent display. The stored message information can be recalled by the user using the user input controls 1138 whereupon the controller 1116 recovers the message information from memory, and provides the message information to a display driver 1140 for presentation on a display 1142, such as an LCD display.

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In accordance with the preferred embodiment of the present invention, the receiver 106 further comprises a channel memory 1151 which stores various channels which the receiver can receive and indicates whether those the receiver has been registered to the system utilizing those channels, whether the proper signal has been identified on those channels (active or inactive), whether the signal received on those channels is strong or weak, and whether the channel is a home channel or not.

10

FIG. 18, is a flow chart describing the synchronization of the data communication receiver of FIG. 11 to system messages. At step 1802, when the data communication receiver is turned on, the controller operation 1116 is initialized, at step 1804. Power is periodically applied to the receiver portion to enable receiving information present on the assigned RF channel. When data is not detected on the channel in a predetermined time period, battery saver operation is resumed, at step 1808. When data is detected on the channel, at step 1806, the synchronization word correlator begins searching for bit synchronization at step 1810. When bit synchronization is obtained, at step 1810, the "A" word correlation begins at step 1812. When the non-complemented "A" word is detected, at step 1814, the message transmission rate is identified as described above, at step 1816, and because frame synchronization is obtained, the time (T1) to the start of the frame identification code word is identified, at step 1818.

30

When the non-complemented "A" word is not detected, at step 1814, indicating the non-complemented "A" word may have been corrupted by a burst error during transmission, a determination is made whether the complemented "A" bar" is detected, at step 1820. When the "A bar" word is not detected at step 1812, indicating that the "A-bar" word may

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also have been corrupted by a burst error during transmission, battery saver operation is again resumed, at step 1808. When the "A-bar" word is detected, at step 1820, the message transmission rate is identified as
5 described above, at step 1822, and because frame synchronization is obtained, the time (T2) to the start of the frame identification code word is identified, at step 1824.

10 At the appropriate time, decoding of the frame identification word occurs, at step 1826. When the frame ID detected is not one assigned to the data communication receiver, at step 1828, battery saving is resumed, at step 1808, and remains so until the next assigned frame is to be
15 received. When the decoded frame ID corresponds to an assigned frame ID, at step 1828, the message reception rate is set, at step 1830. An attempt to bit synchronize at the message transmission rate is next made at step 1832. When bit synchronization is obtained, at step 1832, the "C" word
20 correlation begins at step 1834. When the non-complemented "C" word is detected, at step 1836, frame synchronization is obtained, and the time (T3) to the start of the message information is identified, at step 1838.

25 When the non-complemented "C" word is not detected, at step 1836, indicating the non-complemented "C" word may have been corrupted by a burst error during transmission, a determination is made whether the complement "C bar" is detected, at step 1840. When the "C bar" word is not
30 detected at step 1840, indicating that the "C-bar" word may also have been corrupted by a burst error during transmission, battery saver operation is again resumed, at step 1808. When the "C-bar" word is detected, at step 1840, frame synchronization is obtained, and the time (T4)
35 to the start of the message information is identified, at step 1842. At the appropriate time, message decoding can

begin at step 1844 in a conventional manner as will be apparent to a person skilled in the art.

In FIG. 19 there is illustrated how controller 1116 of data communication receiver 106 processes a registration message 1009. At test step 2010 the controller 1116 conducts a test to determine if a message and associated address is received and matches one of the address patterns assigned to the data communication receiver from the code memory 1122. If a message and associated address is received and matches one of the address patterns assigned to the data communication receiver test step 2011 is effected. At test step 2011 a test is conducted to determine if the received message contains the registration message identifier 1030 which identifies the message as a registration message 1009. If the message identifier 1030 identifies the message as not being a registration message 1009, a step 2015 processes the message in a conventional manner. At the completion of step 2015 test step 2010 is effected.

Alternatively, if at test step 2011 the received message is determined to be a registration message 1009 by examining the message identifier 1030, then each message contents 1020 of the message are stored in message memory 1150. At step 2022 the Registration Timer is initialized with the wait time (TS) 1050. The Registration Timer is a general purpose countdown timer which used to count down the wait time (TS) 1050 and the registration time (TR) 1060 and is implemented in the controller 1116. The implementation of the Registration Timer in controller 1116 is well known to those skilled in the art. At the completion of step 2022 test step 2010 is effected.

In FIG. 20 there is illustrated how controller 1116 processes the Registration Timer. At test step 2080 the

controller 1116 conducts a test to determine if the wait time (TS) 1050 stored in a Registration Timer has expired. If the wait time (TS) 1050 in Registration Timer has expired test step 2082 is effected. At test step 2082 the
5 controller 1116 conducts a test to determine whether the Registration Timer has expired due to the wait time (TS) 1050 expiring or alternatively the registration time (TR) 1060 expiring. If the wait time 1050 has expired then step 2084 is effected. In step 2084 the controller 1116
10 initializes the Registration Timer with the registration time (TR) 1060 and then step 2086 is effected. In step 2086 the controller 1116 then marks channels of relevant system channel identifier(s) 1040 from the stored registration message 1009 as a priority A+ by marking the registration
15 field 4011 (described later with reference to FIG. 25). At the completion of step 2086 step 2080 is effected.

Alternatively, if at test step 2082 the Registration Timer expired due to the registration time (TR) 1060
20 expiring then step 2088 is effected. At step 2088, the priority A+ assigned to the relevant system channels identified by identifier(s) 1040 is then removed (unregistered) by unmarking the registration field 4011 and if appropriate the priority of these channels reverts to a
25 default priority. At the completion of step 2088 test step 2090 is effected. Test step 2090 tests for the existence of further registration data frames 1020 in the stored registration message 1009. If test step 2090 detects no further registration data frames 1020 need processing then
30 step 2080 is effected. If test step 2090 detects more registration data frames 1020 to be processed step 2092 is effected and the wait time (TS) 1050 for the corresponding registration data frame 1020 is used to initialize the Registration Timer. At the completion of step 2092 step
35 2080 is effected.

Referring to FIGs. 21 to 23, there is illustrated how the data communication receiver 106 scans channels in a scan list 4000 contained in both channel memory 1151 and code memory 1122. The channels are categorized into 4 priority levels three of which are default categories permanently stored in code memory 1122. More specifically, in Fig. 24 there is illustrated a scan list 4000 comprising a channel index 4001 of channel identifiers 1 to n+m, the channel identifiers are partitioned into preprogrammed scan list portion 4112 corresponding to channel index identifiers 1 to n that are stored in code memory 1122.

The other portion of scan list 4000 is a dynamic scan list portion 4113 corresponding to channel index identifiers n+1 to n+m stored in channel memory 1151. Further, scan list 4000 also comprises fields associated with each channel index 4001, these fields are: a frequency identifier 4002; a system channel identifier 4003 which corresponds to system channel identifier 1040 of registration message 1009; home identifier 4004 that identifies whether or not the associated channel is usually in a reception range of receiver 106 and when true this field is a logic 1; and an always transmitted field 4005 that identifies whether or not paged messages are transmitted on the associated channel for reception by receiver 106, when true this field is a logic 1.

In Fig 25 there is illustrated a status table 4006 stored in channel memory 1151. Status table 4006 comprises channel index 4001 and the following fields: a valid channel field 4007 for indicating whether or not system channel identifier 4003 matches a system channel identifier transmitted by a received channel (i.e. data contained in an SSID or NID field of the FLEXTM protocol); a signal strength field 4008 which indicates a relative received signal strength of the associated channel; and a

registration field 4011 which indicates whether or not the associated channel is registered and when true this field is a logic 1.

5 Before describing FIGs 21 to 23 in detail the following terms are defined:

- 1) **Monitor or Monitoring Process** comprises:
 - 10 a) sampling one or more channels in the scan list 4000 for paged information in assigned frames in which the receiver 106 expects to receive paged information;
 - b) updating data in channel signal strength field 4008; and
 - 15 c) updating data in valid channel field 4007.

 The controller 1116 of data communication receiver 106 controls the processing of the Monitor process with respect to FIGs. 21, 22, and 23. The
20 Monitor process is enabled and disabled by steps contained in FIGs. 21, 22, and 23. The **Channel input** to the Monitor process specifies which channels should be monitored. The steps in FIGs. 21, 22, and 23 will specify the Channel input to the Monitor process. The
25 Monitor process when disabled will stop monitoring all channels.

- 2) **Channel acquisition Process** comprises:
 - 30 a) updating data in channel signal strength field 4008; and
 - b) updating data in valid channel field 4007.

 The controller 1116 of data communication receiver 106 controls the processing of the Channel acquisition process with respect to FIGs. 21, 22, and
35 23. The Channel acquisition process is enabled and

disabled by steps contained in FIGs. 21, 22, and 23. The **Channel input** to the Channel acquisition process specifies which channels should be sampled for acquisition. The steps in FIGs. 21, 22, and 23 will specify the Channel input to the Channel acquisition process. The steps in FIGs. 20, 21, and 22 will specify the Channel input to the Channel acquisition process. The Channel acquisition process when disabled will stop acquiring all channels.

Note for the FLEXTM protocol the channel acquisition process would be effected in frames 0 to 3 for channels with SSID or frames 0 to 7 for channels with NID when the data communication receiver 106 is synchronized to the received signal.

3) **Channel default priorities** in priority order are:

a) priority A in which channels have a home field 4004 is set to logic 1 and the always transmitted field 4005 is set to logic 1;

b) priority B in which channels have a home field 4004 is set to logic 0 and the always transmitted field 4005 is set to logic 1;

c) priority C in which channels have the always transmitted field 4005 is set to logic 0.

4) **Priority A+ channels:**

is the highest priority which identifies a channel that is desired to be registered and used by the data communication receiver 106. Priority A+ channels are channels that are identified by system channel identifier(s) 1040 of a received registration message 1009. Thus, if a received registration message 1009 identifies a default priority channel in the

preprogrammed scan list portion 4112, this channel is given an upgraded priority of A+ which sets the corresponding registration field 4011 to a logic 1 for a time after wait time (TS) 1050 and length of time (TR) 1060 associated with message 1009. However, a received registration message 1009 may also include a system channel identifier(s) 1040 that is identifying a channel(s) that is not in preprogrammed scan list portion 4112 and is therefore stored in dynamic scan list portion 4113.

In view of the above definitions, and referring to FIGs. 21 to 23, at step 3100 the data communication receiver 106 determines, by scanning using frequency synthesizer 1149 and receiver 1104, if there are any strong A+ channels that are valid 4007. Further, in this specification, strong when associated with channels means channels detected by communication receiver 106 that have a received signal strength greater than a predefined threshold value.

If at step 3100 a strong valid 4007 A+ channel is detected, then at step 3200 the Channel acquisition process is disabled and at step 3300 the Monitor process is enabled with the channel input to the Monitor process being the strong valid 4007 A+ channel with the lowest channel identifier number 4001 in the scan list 4000. However, if step 3100 does not detect a strong valid 4007 A+ channel then at step 3101 a test is conducted to determine if only one single weak valid 4007 A+ channel is detected. In this regard, and in this specification, weak when associated with channels means channels detected by communication receiver 106 that have a signal strength less than the predefined threshold value. If only one weak valid 4007 A+ channel is detected then at step 3201 the Channel acquisition process is enabled with the channel input to

the Channel acquisition process being all other A+ channels in the scan list 4000 and then at step 3301 the Monitor process is enabled with the channel input to the Monitor process being the weak valid 4007 A+ channel detected in
5 step 3101. At the completion of step 3301 step 3100 is effected.

If step 3101 results in a No, then at step 3102 a test is conducted to determine if two or more weak valid 4007 A+
10 channels are detected. If two or more weak valid 4007 A+ channels are detected then at step 3202 the Channel acquisition process is enabled with the channel input to the Channel acquisition process being all other A+ channels in scan list 4000 and then at step 3302 the Monitor process
15 is enabled with the channel input to the Monitor process being the strongest valid 4007 A+ channel channel detected in step 3102. In this regard and for the remainder of this specification strongest refers to a channel with the largest received signal strength.

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If at step 3102 it is determined that there are no weak valid 4007 A+ channels then there are no valid 4007 registration channels A+ available and therefore test step 3103 is effected. Step 3103 determines if there are any
25 strong valid 4007 A channels. If at step 3103 a strong valid 4007 A channel is detected, at step 3203 the Channel acquisition process is enabled with the channel input to the Channel acquisition process being all other A+ channels in the scan list 4000 and at step 3303 the Monitor process
30 is enabled with the channel input to the Monitor process being the strong valid 4007 A channel with the lowest channel identifier number 4001 detected in step 3103. However, if step 3103 does not detect a strong valid 4007 A channel then at step 3104 a test is conducted to determine
35 if only one single weak valid 4007 A channel is detected. If only one weak valid 4007 A channel is detected then at

step 3204 the Channel acquisition process is enabled with the channel input to the Channel acquisition process being all other A+ and A channels in the scan list 4000 and at step 3304 the Monitor process is enabled with the channel
5 input to the Monitor process being the valid 4007 weak A channel detected in step 3104. At the completion of step 3304 step 3100 is effected.

If step 3104 results in a No, then at step 3105 a test
10 is conducted to determine if two or more weak valid 4007 A channels are detected. If two or more weak valid 4007 A channel are detected then at step 3205 the Channel acquisition process is enabled with the channel input to the Channel acquisition process being all other A+ and A
15 channels in the scan list 4000 and at step 3305 the Monitor process is enabled with the channel input to the Monitor process being the strongest valid 4007 A channel detected in step 3105. At the completion of step 3305 step 3100 is effected.

20

If at step 3105 it is determined that there are no weak valid 4007 A channels then there are no valid 4007 A channels available and therefore test step 3106 is effected. Step 3106 determines if there are any strong
25 valid 4007 B channels. If at step 3106 a strong valid 4007 B channel is detected then at step 3206 the Channel acquisition process is enabled with the channel input to the Channel acquisition process being all other A+ and A channels in the scan list 4000 and at step 3306 the Monitor
30 process is enabled with the channel input to the Monitor process being then the strong valid 4007 B channel with the lowest channel identifier number 4001 detected in step 3106. However, if step 3106 does not detect a strong valid 4007 B channel then at step 3107 a test is conducted to determine
35 if only one weak valid 4007 B channel is detected. If a weak valid 4007 B channel is detected then at step 3207 the

Channel acquisition process is enabled with the channel input to the Channel acquisition process being all other A+, A, and B channels in the scan list 4000 and then at step 3307 the Monitor process is enabled with the channel
5 input to the Monitor process being the weak valid 4007 B channel detected in step 3107. At the completion of step 3307 step 3100 is effected.

If step 3107 results in a No, then at step 3108 a test
10 is conducted to determine if two or more weak valid 4007 B channel are detected. If two or more weak valid 4007 B channels are detected then at step 3208 the Channel acquisition process is enabled with the channel input to the Channel acquisition process being all other A+, A and B
15 channels in the scan list 4000 and then at step 3308 the Monitor process is enabled with the channel input to the Monitor process being the strongest valid 4007 B channel detected in step 3108. At the completion of step 3308 step 3100 is effected.

20

If at step 3108 it is determined that there are no weak valid 4007 B channels then there are no valid 4007 B channels available and therefore test step 3109 is effected. Step 3109 determines if there is only one valid
25 4007 C channel. If at step 3109 only one valid 4007 C channel is detected, at step 3209 the Channel acquisition process is enabled with the channel input to the Channel acquisition process being all channels of priorities A+, A, B and C in the scan list 4000 and then at step 3309 the
30 Monitor process is enabled with the channel input to the Monitor process being the valid C channel detected in step 3109. At the completion of step 3309 step 3100 is effected. However, if step 3109 does not detect only one C channel then at step 3110 a test is conducted to determine if more
35 than one valid 4007 C channel has been detected. If more than one valid 4007 C channel has been detected then at

step 3210 the Channel acquisition process is enabled with the channel input to the Channel acquisition process being all channels from all priorities A+, A, B and C from scan list 4000 and then at step 3310 3309 the Monitor process is
5 enabled with the channel input to the Monitor process being all the valid 4007 C channels detected in step 3110. At the completion of step 3310 step 3100 is effected. When monitoring at step 3310 a frame offsetting technique can be used as described in the FLEXTM protocol and in US patent
10 No. US 4914649, therefore allowing the monitoring of multiple channels during a FLEXTM cycle.

If step 3110 results in a No, then the Channel acquisition process is enabled with the
15 channel input to the Channel acquisition process being all channels from the scan list 4000 and at step 3311 the Monitor process is disabled. At the completion of step 3311 step 3100 is effected.

20 The present invention allows for receiving a registration message 1009 comprising channel identification data identifying one or more priority channels and timing information 1050, 1060. The priorities of the channels can be changed from their default category at time
25 dependent on the timing information 1050, 1060. Scanning the channels for channel acquisition, as illustrated in Figs 20 to 22, in accordance with the priorities therefore determines the most suitable channel that is then monitored for messages until a more suitable channel is identified.

30 Advantageously, the present invention allows for battery saving due to there being no need to scan for channels with lower priorities. In addition to battery saving the chance of the communication receiver 106
35 receiving valid messages are improved. Accordingly, the invention offers benefits when used in a system using

numerous coverage areas that may have overlapping coverage areas.

5 When monitoring two or more C channels with frame
offsetting, one channel can block reception of another
channel's data due to information services usually having a
common address that is not offset. Hence, a further
advantage of the present invention is that when the
receiver is in range of an A+, A or B channel, messages are
10 transmitted and received in assigned frames as only a
single channel needs to be monitored. Accordingly, the
problem associated with a channel blocking reception of
another channel's data is reduced.

15 Although the invention has been described with
reference to a preferred embodiment it is to be understood
that the invention is not restricted to the embodiment
described herein. For example, protocols other than FLEXTM
can be used to transmit registration messages 1009.
20 Further, it will be apparent that controller 1116 allows
for multitasking of processes so that for example
monitoring of channels is executed as a foreground task
whereas scanning and monitoring of channels runs as a
background task.

25



CLAIMS

1. A communication receiver comprising:
 - a memory for storing a plurality of channel
5 identifiers corresponding to a plurality of channels and
for storing at least one address assigned to the
communication receiver;
 - a frequency synthesizer for generating a channel
10 signal corresponding to one of said plurality of channels;
receiver circuitry coupled to the frequency synthesizer for
receiving and demodulating selective call signals on one of
said plurality of channels in response to the channel
signal;
 - 15 a decoder coupled to said receiver circuitry for
decoding the selective call signals to generate selective
call messages;
 - 20 a controller coupled to the memory and the decoder for
comparing the at least one address to address information
within the selective call messages to determine whether the
selective call messages are intended for the communication
receiver;
 - 25 wherein the controller further determines whether the
selective call messages are registration messages
comprising channel registration information intended for
the communication receiver and, if the selective call
30 messages are registration messages, stores the channel
registration information in the memory in association with
one of the plurality of channel identifiers; and
 - wherein the controller is coupled to the frequency
35 synthesizer and generates a channel synthesizing signal
corresponding to one of the plurality of channel
identifiers to supply to the frequency synthesizer and the



frequency synthesizer generates the channel signal in response thereto, the one of the plurality of channel identifiers determined in response to the channel registration information associated with the one of the
5 plurality of channel identifiers.

2. A communication receiver as claimed in Claim 1 further comprising a signal strength detector coupled to the receiver circuitry and the controller for providing the
10 controller a channel strength signal associated with the one of the plurality of channels being received in response to determining whether the receiver is receiving a signal having a strength above a predetermined threshold, wherein the controller generates a channel synthesizing signal
15 corresponding to one of the plurality of channel identifiers to supply to the frequency synthesizer and the frequency synthesizer generates the channel signal in response thereto, the one of the plurality of channel identifiers determined in response to the channel
20 registration information and the channel strength signal associated with the one of the plurality of channel identifiers.

3. A communication receiver comprising:
25 a controller;
a receiver means for both receiving messages and scanning to detect transmitted channel frequencies;
frequency generating means coupled to said controller and said receiver means;
30 wherein said controller is adapted to control said frequency generating means to thereby effect scanning of channel frequencies by said receiver to determine a channel frequency for monitoring messages, said scanning being dependent upon priorities associated with said
35 channel frequencies, and wherein at least some of said channel frequencies have a priority dependent upon one or



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more received registration messages identifying a change of one or more said priorities.

4. A communication receiver as claimed in claim 3,
5 wherein said communication receiver is adapted such that at least some of said channels have a default priority that is changeable by said one or more received registration messages.
- 10 5. A communication receiver as claimed in claim 3 or claim 4, wherein said communication receiver is adapted to change a priority of one or more channels at a predetermined time.
- 15 6. A communication receiver as claimed in any one of claims 3 to 5, wherein said communication receiver is adapted to allow a priority of a changed said one or more channels to last for a predetermined time before returning to an associated default priority.
- 20 7. A communication receiver as claimed in any one of claims 3 to 6, wherein said communication receiver is adapted to scan said channels in an order associated with said priorities.
- 25 8. A communication receiver as claimed in any one of claims 3 to 7, wherein said communication receiver has a threshold level detection means for detecting if a received channel strength is above a threshold level.
- 30 9. A communication receiver as claimed in any one of claims 3 to 8, wherein said communication receiver is adapted to control said frequency generating means to scan channels of a higher priority than said channel frequency
35 for monitoring messages.

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10. A method for identifying channels available to communicate with a communication receiver, said method comprising the steps of:

5 receiving a registration message comprising channel identification data identifying one or more priority channels and timing information;

changing priorities of at least some of said channels
10 at a time dependent on said timing information;

scanning said channels in a accordance with said priorities to determine a channel for receiving message;

15 monitoring said channel.

11. A method as claimed in claim 10, wherein said step of scanning also includes the step of comparing channel strengths against a threshold value.
20

12. A method as claimed in claim 10 or claim 11, wherein the step of scanning is characterised by scanning channels of a higher priority than said channel.

25 13. A communication receiver substantially as described herein with reference to and as illustrated by the accompanying drawings.

14. A method for identifying channels available to
30 communicate with a communication receiver substantially as described herein with reference to and as illustrated by the accompanying drawings.

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