WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of layers sequentially stacked on a substrate in a vertical direction, each of the plurality of layers comprising a bit line extending in a first direction and a semiconductor pattern extending from the bit line in a second direction that traverses the first direction;

a gate electrode extending through the plurality of layers, the gate electrode comprising a vertical portion extending through the semiconductor patterns and a first horizontal portion extending from the vertical portion and facing a first surface of one of the semiconductor patterns; and

a data storing element electrically connected to the one of the semiconductor patterns,

wherein the data storing element comprises:

a first electrode electrically connected to the one of the semiconductor patterns;

a second electrode on the first electrode; and

a dielectric layer between the first electrode and the second electrode,

wherein the one of the semiconductor patterns comprises:

a first impurity region electrically connected to one of bit lines;

a second impurity region electrically connected to the first electrode; and

a channel region between the first and second impurity regions,

wherein the vertical portion extends through the channel region, and

wherein the channel region surrounds the vertical portion.

2. The semiconductor memory device of claim 1, wherein the gate electrode further comprises a second horizontal portion extending from the vertical portion and facing a second surface of the one of the semiconductor patterns, and the second surface of the one of the semiconductor patterns is opposite to the first surface of the one of the semiconductor patterns.

3. The semiconductor memory device of claim 2, wherein the first surface is a top surface of the one of the semiconductor patterns, and

the second surface is a bottom surface of the one of the semiconductor patterns.

4. The semiconductor memory device of any one of claims 1 to 3, wherein the first horizontal portion overlaps the one of the semiconductor patterns.

5. The semiconductor memory device of any one of claims 1 to 4, further comprising:

a first silicide pattern between the one of the semiconductor patterns and one of the bit lines; and

a second silicide pattern between the one of the semiconductor patterns and the first electrode.

6. The semiconductor memory device of any one of claims 1 to 5, further comprising a gate insulating layer between the one of the semiconductor patterns and the gate electrode.

7. The semiconductor memory device of any one of claims 1 to 6, wherein the plurality of layers comprise a first layer comprising a first semiconductor pattern and a second layer comprising a second semiconductor pattern, and the first layer is between the substrate and the second layer, and

a first width of the first semiconductor pattern in the first direction is wider than a second width of the second semiconductor pattern in the first direction.

8. The semiconductor memory device of claim 7, wherein a third width of the vertical portion adjacent to the first semiconductor pattern is narrower than a fourth width of the vertical portion adjacent to the second semiconductor pattern.

9. A semiconductor memory device comprising:

a plurality of layers sequentially stacked on a substrate in a vertical direction, each of the plurality of layers comprising a bit line extending in a first direction and a semiconductor pattern extending from the bit line in a second direction that traverses the first direction;

a gate electrode extending through the plurality of layers; and

a data storing element electrically connected to one of the semiconductor patterns,

wherein the gate electrode comprises:

a vertical portion extending through the semiconductor patterns;

a first horizontal portion extending from the vertical portion and facing a first surface of the one of the semiconductor patterns; and

a second horizontal portion extending from the vertical portion and facing a second surface of the one of the semiconductor patterns, wherein the second surface of the one of the semiconductor patterns is opposite to the first surface of the one of the semiconductor patterns,

wherein the one of the semiconductor patterns comprises:

a first impurity region electrically connected to one of bit lines;

a second impurity region electrically connected to the data storing element; and

a channel region between the first and second impurity regions,

wherein the vertical portion extends through the channel region, and

wherein the channel region surrounds the vertical portion.

10. The semiconductor memory device of claim 9, wherein the data storing element comprises:

a first electrode electrically connected to the one of the semiconductor patterns;

a second electrode on the first electrode; and

a dielectric layer between the first electrode and the second electrode.

11. The semiconductor memory device of claim 9 or claim 10, wherein the first horizontal portion overlaps the one of the semiconductor patterns that overlaps the second horizontal portion.

12. The semiconductor memory device of any one of claims 9 to 11, wherein the first surface is a top surface of the one of the semiconductor patterns, and

the second surface is a bottom surface of the one of the semiconductor patterns.

13. A semiconductor memory device comprising:

a bit line extending on a substrate in a first direction;

a semiconductor pattern extending in a second direction that traverses the first direction, the semiconductor pattern comprising a first impurity region, a second impurity region, and a channel region between the first and second impurity regions, the first impurity region being electrically connected to the bit line;

a gate electrode comprising a vertical portion extending through the channel region of the semiconductor pattern and a first horizontal portion extending from the vertical portion and facing a first surface of the semiconductor pattern; and

a data storing element electrically connected to the second impurity region of the semiconductor pattern,

wherein the channel region surrounds the vertical portion of the gate electrode.

14. The semiconductor memory device of claim 13, wherein the semiconductor pattern is spaced apart from the substrate, and

the semiconductor pattern has a bar-shape extending in the second direction, when viewed in a plan view.

15. The semiconductor memory device of claim 13 or claim 14, wherein the gate electrode further comprises a second horizontal portion extending from the vertical portion and facing a second surface of the semiconductor pattern opposite to the first surface of the semiconductor pattern.

16. The semiconductor memory device of any one of claims 13 to 15, further comprising:

a first silicide pattern between the first impurity region and the bit line; and

a second silicide pattern between the second impurity region and the data storing element.

17. The semiconductor memory device of any one of claims 13 to 16, wherein the data storing element comprises:

a first electrode electrically connected to the second impurity region;

a second electrode on the first electrode; and

a dielectric layer between the first electrode and the second electrode.