

PROTECTION DAM FOR A POWER MODULE WITH SPACERS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent application claims the benefit of U.S. Non-Provisional Patent Application No. 18/172,904, filed on February 22, 2023, and titled “Protection Dam for a Power Module with Spacers,” which is incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] This description relates to assembling and packaging semiconductor device modules, e.g., semiconductor device assemblies, semiconductor device module assemblies, etc. More specifically, this description relates to semiconductor device modules with improved thermal performance and mechanical stress reduction.

BACKGROUND

[0003] Semiconductor device modules, such as modules including power semiconductor devices, can be implemented using multiple semiconductor dies, multiple substrates (e.g., direct-bonded metal (DBM) substrates, die attach pads (DAPs)), electrical interconnections, and a molding compound. Power transistors can include, for example, insulated-gate bipolar transistors (IGBTs) or power metal-oxide-semiconductor field effect transistors (MOSFETs). Electrical interconnections within a high-power semiconductor device module can include, for example, bond wires, conductive spacers, and conductive clips. A polymer molding compound can serve as an encapsulant to protect components of the device assembly. Such power transistor devices can be used in various applications, including automotive and/or industrial applications.

SUMMARY

[0004] In some aspects, the techniques described herein relate to an apparatus, including: a substrate; a chip assembly coupled to the substrate where the chip assembly includes: a semiconductor die, a heat sink, and a molding material coupled to the heat sink; and a protection dam surrounding at least a portion of a perimeter of the chip assembly.

[0005] In some aspects, an apparatus includes a protection dam configured to absorb mechanical stress from expansion of the heat sink.

- [0006] In some aspects, an apparatus includes a protection dam made of a flexible material.
- [0007] In some aspects, an apparatus includes a protection dam that having a barrier configured to block a flow of solder.
- [0008] In some aspects, an apparatus includes a protection dam that forms a seal against the substrate.
- [0009] In some aspects, an apparatus includes a protection dam made of copper.
- [0010] In some aspects, an apparatus includes a direct bonded metal (DBM) substrate, having a first metal layer, a second metal layer, and an insulating layer disposed between the first and second metal layers, the protection dam being a recessed copper layer integrated in the first metal layer.
- [0011] In some aspects, an apparatus includes a first chip assembly and a second chip assembly coupled to the substrate, the protection dam encompassing both chip assemblies.
- [0012] In some aspects, an apparatus includes a first chip assembly and a second chip assembly coupled to the substrate, the second chip assembly being disposed outside the protection dam.
- [0013] In some aspects, an apparatus includes a semiconductor die coupled to the copper heat sink by a sintered layer of silver (Ag).
- [0014] In some aspects, an apparatus includes a chip assembly that is a component of a high-power module configured for use in an automotive system.
- [0015] In some aspects, an apparatus includes a substrate; a die assembly coupled to the substrate, the die assembly including copper components in contact with a polymer layer; and a protection dam disposed around the die assembly.
- [0016] In some aspects, an apparatus includes a protection dam attached to the substrate.
- [0017] In some aspects, an apparatus includes a protection dam integrated into the substrate.
- [0018] In some aspects, an apparatus includes a protection dam that includes a recessed area of the substrate.
- [0019] In some aspects, an apparatus includes a protection dam having an extension configured as a solder barrier.
- [0020] In some aspects, the techniques described herein relate to a method that includes forming a chip assembly having a semiconductor die and a copper spacer; forming a protective dam around the chip assembly; coupling a substrate to a lead frame; coupling the chip assembly

to the substrate; forming a direct bond metal (DBM) layer above the chip assembly; forming wire bonds to leads of the lead frame; and filling remaining space around the chip assembly with a molding compound.

[0021] In some aspects, forming the protective dam around the chip assembly includes attaching the protective dam to the substrate.

[0022] In some aspects, the protective dam is flexible and attaching the protective dam to the substrate includes applying pressure to the protective dam.

[0023] In some aspects, attaching the protective dam to the substrate includes applying an adhesive.

[0024] In some aspects, the protective dam is metallic and attaching the protective dam to the substrate includes soldering.

[0025] In some aspects, forming the protective dam includes forming a solder barrier integral to the protective dam.

[0026] In some aspects, the techniques described herein relate to a method that includes fabricating a chip assembly that includes a semiconductor die and a copper spacer; etching a recessed area in a surface metal layer of a substrate to form a protective dam; coupling the chip assembly to the substrate inside the protective dam; forming a direct bond metal (DBM) layer above the chip assembly; and filling remaining space around the chip assembly with a molding compound.

[0027] In some aspects, a method further includes coupling additional chip assemblies to the substrate, wherein etching the recessed area forms a protective dam around at least one of the additional chip assemblies.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] FIG. 1 is a high-level, simplified block diagram, shown in cross-section, that illustrates a high-power semiconductor device module, according to an implementation of the present disclosure.

[0029] FIG. 2 is a detailed cross-sectional view of the high-power semiconductor device module shown in FIG. 1, according to an implementation of the present disclosure.

[0030] FIG. 3 is a top-side plan view of a high-power semiconductor device module attached to a lead frame, according to an implementation of the present disclosure.

[0031] FIGs 4A, 4B, and 4C show a top-side plan view, a magnified view, and a cross-sectional view, respectively, of a high-power semiconductor device module configured with a high profile flexible protective dam, according to an implementation of the present disclosure.

[0032] FIGs 5A, 5B, and 5C show a top-side plan view, a magnified view, and a cross-sectional view, respectively, of a high-power semiconductor device module configured with a low profile flexible protective dam, according to an implementation of the present disclosure.

[0033] FIGs 6A, 6B, and 6C show a top-side plan view, a magnified view, and a cross-sectional view, respectively, of a high-power semiconductor device module configured with a metallic protective dam, according to an implementation of the present disclosure.

[0034] FIGs 7A, 7B, and 7C show a top-side plan view, a magnified view, and a cross-sectional view, respectively, of a high-power semiconductor device module configured with an integral protective dam, according to an implementation of the present disclosure.

[0035] FIGs 8A, 8B, and 8C show a top-side plan view, a magnified view, and a cross-sectional view, respectively, of a high-power semiconductor device module configured with an integral protective dam, according to an implementation of the present disclosure.

[0036] FIG. 9 is a flow diagram of a method for fabricating a high-power semiconductor device module configured with a protection dam, according to an implementation of the present disclosure.

[0037] FIG. 10 is a plot of computer simulation data showing the benefits of implementing various types of protective dams, according to an implementation of the present disclosure.

[0038] In the drawings, which are not necessarily drawn to scale, like reference symbols may indicate like and/or similar components (elements, structures, etc.) in different views. The drawings illustrate generally, by way of example, but not by way of limitation, various implementations discussed in the present disclosure. Reference symbols shown in one drawing may not be repeated for the same, and/or similar elements in related views. Reference symbols that are repeated in multiple drawings may not be specifically discussed with respect to each of those drawings but are provided for context between related views. Also, not all like elements in the drawings are specifically referenced with a reference symbol when multiple instances of an element are illustrated.

DETAILED DESCRIPTION

[0039] This disclosure relates to implementations of high-power semiconductor device assemblies and modules with improved thermal performance and reduced mechanical stresses.

[0040] In an assembly process for a semiconductor device module, a semiconductor die assembly, e.g., a chip assembly, including a semiconductor die containing one or more electronic devices, is first attached to a substrate. Contact or bond pads of the semiconductor die can then be attached by wire bonding to contact pads at ends of the leads of a lead frame. In some implementations, double sided cooling can be applied to the semiconductor die, in which case wire bonding may not be needed. After attaching the semiconductor die assembly, the lead frame is placed in a mold. The mold is provided with a reservoir for containing a quantity of an insulating molding compound. The molding compound is then injected into the mold to encapsulate the die attach pad(s) and the semiconductor die(s).

[0041] In some applications, power transistor devices can be used to implement electronic circuits, e.g., inverters or power amplifiers, used in automotive systems such as electrical vehicles (EVs) and/or hybrid electrical vehicles (HEVs). Such applications need reliable heat dissipation. Current implementations of semiconductor device assemblies including such power transistors (e.g., in combination with a fast recovery diode (FRD)) have certain drawbacks regarding thermal management. For example, some assemblies include heat sinks that alter the thermal profile of the assembly. Additionally, or alternatively, some implementations may only allow for cooling of the assembly, e.g., by attaching a thermal dissipation appliance, on a single side of the assembly. Such thermal imbalances can cause and/or exacerbate stresses between components within such an assembly, such as tensile stress and strain energy on the included semiconductor die, which can damage components of the assembly. As power requirements and associated operating temperatures for such devices increase, incidents of such damage may also increase.

[0042] In some implementations, a power transistor assembly can include, in proximity to the semiconductor die, a spacer that acts as a heat sink. In this context, the spacer dissipates heat produced by components on the die that operate at high voltages. Such spacers can be made of various materials, including ceramics, metals, and so forth. Spacers are one way to boost the thermal performance of a high-power semiconductor die. When copper components are used as heat sinks to dissipate heat within a chip assembly, or die assembly, rapid expansion of the copper can induce tensile stress in adjacent materials. Depending on the relative dimensions and material properties in the vicinity of the heat sink, the added stress may cause damage, e.g., cracks, dislocations, or fractures in the surrounding structure. Such damage may result in premature failure of devices within the chip assembly, poor thermal performance, or poor reliability.

[0043] This disclosure relates to implementations of high-power semiconductor device assemblies and modules with improved thermal performance and reduced mechanical stresses that address the issues described above. At least one solution is to introduce a protective element to relieve tensile stress in the structure around the copper spacers. Various types of protective elements are presented herein, in the form of flexible protective dams, metallic protective dams, and integral protective dams designed to surround one or more chip assemblies, within a power module, that experience a high degree of heat dissipation. In some implementations, the protective dam can be in contact with a lower surface of the chip assembly, and the protective dam may have walls that partially extend along sides of the chip assembly. In some implementations, the protective dam can be slightly spaced apart from the chip assembly.

[0044] FIG. 1 shows a simplified example of a high-power semiconductor device module 100, according to some implementations of the present disclosure. A more detailed illustration of the high-power semiconductor device module 100 is provided below in FIG. 2. In some implementations, the high-power semiconductor device module 100 includes, as fundamental elements, a substrate 102, one or more chip assemblies 104 (one shown), and an upper direct bond metal (DBM) structure 106. In some implementations, the substrate 102 can also include a lower DBM structure. In some implementations, the DBM structures are direct bond copper (DBC) type structures or direct bond aluminum (DBA) or direct plating copper (DPC) type structures. The DBM structure 106 can be designed as a three-layer structure that includes a large thermal mass, e.g., a dielectric, disposed between two outer metal layers to draw in and absorb heat. In some implementations, the thermal mass can provide electrical insulation. Use of both upper and lower DBM structures provides dual sided cooling for the chip assembly 104.

[0045] The chip assembly 104 includes at least one semiconductor die 108 and the spacer 110 in contact with the semiconductor die 108 to dissipate, e.g., rapidly dissipate,) heat generated therein. The chip assembly 104 is coupled to, e.g., mounted on, the substrate 102. In some implementations, the upper DBM structure 106 is a multi-layer structure formed on the spacer 110. In some implementations, the upper DBM structure 106 is larger than the spacer 110, which is, in turn, larger than the semiconductor die 108, thus creating a reverse pyramidal (as oriented in FIG. 1), or top-heavy, structure on the substrate 102. After constructing the chip assembly 104 and the DBM structure 106 on the substrate 102, remaining space around the chip assembly 104 can be filled with a molding compound 112.

[0046] The spacer 110, which serves as a heat sink, is made of a material having a high thermal conductivity such as, for example, copper or alloys thereof. One such copper alloy that

can be used as the spacer 110 is a copper-molybdenum (CuMo) alloy. The choice of whether to use pure copper or, for example, CuMo, may be made based on heat dissipation requirements for the type of chip assembly 104 coupled to the spacer 110. For example, an FRD chip assembly, designated below as 104b, may operate at a higher voltage or current than an IGBT chip assembly, designated below as 104a, and therefore may generate more heat and may need more efficient heat dissipation as provided by a spacer 110 made of pure copper. Cost may also be a factor. Pure copper can be less expensive than a copper alloy like CuMo, while providing faster heat dissipation. However, when the spacer 110 is made of pure copper, it may be more likely to cause stress damage to surrounding materials. In particular, the molding compound 112, e.g., a polymer, which is in direct contact with the spacer 110, e.g., a pure copper spacer, is vulnerable to damage from rapid expansion of the spacer 110, especially at exposed corners C of the spacer 110.

[0047] One way of relieving stress on the molding compound 112 is to replace a portion of the molding compound 112 with a material that can absorb stress, e.g., a flexible material such as a polymer or an elastomer that can conform to the chip assembly 104b. Alternatively, a material that can provide further thermal dissipation, e.g., additional copper, can be used. In some implementations, the replacement material can form a protective dam 114 around (e.g., in contact with) the chip assembly 104 (and/or portions thereof). In some implementations, the replacement material can form a protective dam 114 around the lower corners C of the spacer 110 that would otherwise be surrounded by the molding compound 112. Formation of the protective dam 114 can occur after attachment of the chip assembly 104 to the substrate 102, and prior to fabrication of the upper DBM structure 106 on top of the chip assembly 104. In some implementations, the protective dam 114 can be L-shaped so as to wrap around the lower corner C. The protective dam 114 can extend under the lower corner C to abut the semiconductor die 108. The height of the protective dam 114 relative to the spacer 110 can vary, as described below.

[0048] After the upper DBM structure 106 is formed on the chip assembly 104, with the protective dam 114 in place, the molding compound 112 can be injected to be disposed in (e.g., occupy) remaining spaces around the chip assembly 104. In some implementations, the molding compound 112 fills all of the remaining space around the chip assembly. In some implementations, there may be spaces, e.g., air pockets, around the chip assembly that are not completely filled with the molding compound 112. Because the protective dam 114 already occupies space around the chip assembly 104, there will be less remaining space to fill with the molding compound 112. With the addition of the protective dam 114, the injected molding

compound 112 will occupy the open space around the upper part of the chip assembly 104, which does not include exposed corners C. This region is therefore less likely to form cracks than the region around the lower part of the chip assembly 104, which is surrounded by the protective dam 114.

[0049] As shown in FIG. 1, the protective dam 114 can have a first portion closer to and in contact with the semiconductor die 108, and a second portion farther away from the semiconductor die 108 and in contact with the sidewall of the spacer 110. The first portion can have a first thickness t_1 less than a second thickness t_2 of the second portion. The first thickness t_1 of the first portion can be disposed between a bottom surface of the spacer 110 and a top surface of the substrate 102. The second thickness t_2 of the second portion can be disposed between a bottom surface of the molding compound 112 and the top surface of the substrate 102.

[0050] FIG. 2 shows a detailed cross-sectional view of the high-power semiconductor device module 100, according to some implementations of the present disclosure. FIG. 2 includes intermediate layers in addition to the fundamental elements shown in FIG. 1. In FIG. 2, the protective dam 114 is shown in dashed lines. In the example shown, the substrate 102 includes a lower DBM structure. In some implementations, the lower DBM structure can be substantially same as, or similar to, the upper DBM structure 106. For example, both DBM structures can be three-layer structures in which inner layers 102b and 106b, which provide the thermal mass of the DBM structures, are made of an electrically insulating but thermally conductive ceramic material, e.g., aluminum oxide (Al_2O_3) or another ceramic, and top and bottom outer metal layers 102a,c and 106a,c are made of copper or another high conductivity metal. In some implementations, the ceramic inner layers 102b and 106b can be attached to the outer metal layers 102a,c and 106a,c using an adhesive material (not shown), e.g., a thermally conductive epoxy adhesive, or an electrically conductive epoxy adhesive such as a silver-filled epoxy. In some implementations, the ceramic inner layers 102b, 106b can each have a thickness in a range of about 0.3 mm to about 0.35 mm. In some implementations, the outer metal layers 102a,c and 106a,c can have a thickness between about 0.2 mm and about 0.8 mm.

[0051] In some implementations, the chip assembly 104 can be attached to the upper DBM structure 106 and to the substrate 102 by solder layers 116. In forming the solder layer 116 on a top surface of the substrate 102, a solder resist material 118 can be patterned to contain solder to desired areas of the substrate 102. In some implementations, the solder resist material 118 can have a thickness in a range of about 0.01 to about 0.03 mm. Each chip assembly 104, including the semiconductor die 108 and the spacer 110, can be held together by a bonding layer

120. In some implementations, the bonding layer 120 can be made of a layer of sintered silver (Ag) inserted between the semiconductor die 108 and the spacer 110.

[0052] FIG. 2 further illustrates cracks that tend to form in the molding compound 112 surrounding the layers described above, when the protective dam 114 is excluded. In particular, the molding compound 112 located next to a lower corner C of the spacer 110 can be vulnerable to cracking in the absence of the protective dam 114. In the example shown in FIG. 2, a distance d1 of the molding compound between the upper DBM structure 106 and the substrate 102 can be in a range of about 2.0 to about 3.0 mm, and a distance d2 between the lower corner C of the spacer 110 and the lower DBM structure of the substrate 102 can be in a range of about 0.1 mm to about 0.5 mm. Without a protective dam 114 in place, strain on the spacer 110 can accumulate from radial forces R1 and R2 at the upper and lower corners, respectively, of the spacer 110. In some implementations, the radial force R2 can be especially problematic at the lower corner C, which may extend laterally beyond the semiconductor die 108. Stresses in the molding compound 112 arising from such strain on the spacer 110, caused by the various surrounding layers of material, can result in the formation of corner cracks 122 that extend downward from the lower corner C toward the substrate 102, as well as vertical cracks 124 that extend through a region of the molding compound 112 located between the upper and lower DBM structures.

[0053] FIG. 3 shows a top-down view of a packaged high-power semiconductor device module 100 attached to a lead frame, according to some implementations of the present disclosure. The lead frame includes - leads 304 and mounting brackets 306. The leads 304 (six shown on each side of the lead frame) provide signal paths to and from each semiconductor die 108 in the chip assemblies 104. The lead frame can be cut or stamped from a thin sheet of metal, e.g., copper.

[0054] In the example shown, the high-power semiconductor device module 100 includes a total of four chip assemblies that are attached to the substrate 102, e.g., to the top outer metal layer 102a of the lower DBM structure. The four chip assemblies shown are of two types: transistor chip assemblies 104a (two shown) and diode chip assemblies 104b (two shown). In some implementations, the larger transistor chip assemblies 104a contain a die 108a in which power transistors, e.g., IGBTs, are coupled to CuMo copper alloy spacers 110a. In some implementations, the smaller diode chip assembly 104b includes die 108b in which diodes, e.g., FRDs, are coupled to copper spacers 110b. In the example shown, the chip assemblies 104 are attached to a common substrate 102.

[0055] In FIG. 3, the protective dams 114 are represented as dashed-line rectangles. In some implementations, the protective dams can have rounded corners. In some implementations, the protective dams 114 can be square, circular, or irregularly shaped, depending on the shapes of the chip assemblies 104. In the example shown, the protective dams 114 are applied to the diode chip assemblies 104b that are equipped with copper spacers 110b, which can be more vulnerable to cracking than the transistor chip assemblies 104a that are equipped with copper alloy spacers 110a. In some implementations, a protective dam 114 can encompass more than one chip.

[0056] FIGs 4A-4C, 5A-5C, 6A-6C, 7A-7C, and 8A-8C each show top-down, magnified, and cross-sectional views, respectively, of the packaged high-power semiconductor device module 100 with the addition of protective dams 114, according to various implementations of the present disclosure. Each set of figures shows a different example of the protective dam 114 applied to a high-power diode chip assembly 104b that includes, as a heat sink, the copper spacer 110b. It is noted that the upper DBM structures 106 have been omitted from the top-down perspective views shown in FIGs. 4A, 5A, 6A, 7A, and 8A, in the interest of clarity.

[0057] FIGs. 4A-4C and 5A-5C show the packaged high-power semiconductor device module 100 implemented with two types of flexible protective dams 114a and 114b, respectively; FIGs. 6A-6C show the packaged high-power semiconductor device module 100 implemented with a metallic protective dam 114c; and FIGs. 7A-7C and 8A-8C show the packaged high-power semiconductor device module 100 implemented with two types of integral protective dams 114d and 114e, respectively.

[0058] It is noted that, although each set of FIGs. 4A-4C, 5A-5C, 6A-6C, 7A-7C, and 8A-8C illustrates the protective dams 114 applied to a high-power semiconductor device module 100 implemented with dual-sided cooling provided by upper and lower three-layer DBM structures, the same protective dams 114 can be applied to a similar high-power semiconductor device module 100 implemented with single-sided cooling provided by either an upper or a lower DBM structure. Alternatively, the same protective dams 114 can be applied to a high-power semiconductor device module 100 implemented without any DBM structures.

[0059] FIGs. 4A, 4B, and 4C illustrate the high-power semiconductor device module 100 configured with high profile flexible protective dams 114a, according to some implementations of the present disclosure. FIG. 4A shows a top-side plan view of the high-power semiconductor device module 100 during its fabrication. The high profile flexible protective dams 114a have been added to the FRD chip assemblies 104b that have copper spacers 110b. The high profile flexible protective dams 114a are not added to the IGBT transistor chip assemblies 104a, which

have copper alloy spacers 110a, e.g., CuMo spacers. This is because the cracking problem as described above preferentially affects the molding compound 112 around corners of the copper spacers 110b, due to the higher thermal conductivity of copper.

[0060] In the example shown, the high profile flexible protective dams 114a are in the form of rectangular enclosures that have walls. In some implementations, the high profile flexible protective dams 114a are made of an elastic polymer material, similar to a gasket. In some implementations, the high profile flexible protective dams 114a are made of an epoxy material. The high profile flexible protective dams 114a may wrap and/or fit tightly around, e.g., conform to, the perimeters of each of the chip assemblies 104b, so that the high profile flexible protective dams 114a are in physical contact with the lower corners C of the copper spacers 110b.

[0061] FIG. 4B shows a magnified view of an example of the high profile flexible protective dam 114a, according to some implementations of the present disclosure. In the example shown, the dimensions of the high profile flexible protective dam 114a are as follows: inner length and width dimensions L and W of the high profile flexible protective dam 114a can be about 0.5 mm larger than the size of the spacer 110b; a wall thickness t of the high profile flexible protective dam 114a can be about 0.4 mm to about 1.0 mm; and a height h of the high profile flexible protective dam 114a can be in a range of about 1.0 mm to about 2.0 mm such that the high profile flexible protective dam 114a covers at least lower portions of the sides of the copper spacer 110b, as is also shown in FIG. 4C.

[0062] FIG. 4C shows a cross-sectional view of the high-power semiconductor device module 100 along cut 4C-4C, to further illustrate in detail the multi-layer DBM structures and external connections to the chip assemblies 104. In some implementations, both the lower DBM structure of substrate 102 and the upper DBM structure 106 are included as additional heat sinks to dissipate heat from both of the chip assemblies 104a and 104b, thereby providing dual-sided cooling of the high-power semiconductor device module 100. Alternatively, one of the DBM structures (e.g., DBM structure 106) can be used to provide single-sided cooling of the high-power semiconductor device module 100. In the example shown in FIG. 4C, both the upper and lower DBM structures are shared by a pair of chip assemblies 104a and 104b. In some implementations, common upper and lower DBM structures can be shared by all four of the chip assemblies included in the packaged high-power semiconductor device module 100. Alternatively, each chip assembly 104 can be attached to a separate, dedicated DBM structure or structures.

[0063] Referring still to FIG. 4C, the leads 304 provide electrical connections to the chip assemblies 104a and 104b via the top outer metal layer 102a of the lower DBM in the substrate 102. Some connections can be made directly to the top outer metal layer 102a. Other connections can be made via wire bonds 404 that couple the leads 304 to the top outer metal layer 102a of the lower DBM structure in the substrate 102. In some implementations, the top outer metal layer 102a can be patterned, while the bottom outer metal layer 102c can be continuous.

[0064] FIG. 4C also shows the vertical profile of the high profile flexible protective dam 114a relative to the sides and corners of the copper spacer 110b. In the example shown, the wall of the high profile flexible protective dam 114a surrounds the lower corners C, and extends about halfway up the sides, of the copper spacer 110b. In some implementations, the wall of the high profile flexible protective dam 114a can surround larger portions, or all, of the sides of the copper spacer 110b. In some implementations, the wall of the high profile flexible protective dam 114a can surround smaller portions, or none, of the sides of the copper spacer 110b. When the wall of the high profile flexible protective dam 114a surrounds at least some portion of the sides of the copper spacer 110b, the high profile flexible protective dam 114a forms an L-shaped profile around the lower corners C of the copper spacer 110b.

[0065] FIGs. 5A, 5B, and 5C illustrate the high-power semiconductor device module 100 configured with low profile flexible protective dams 114b, according to some implementations of the present disclosure. FIGs. 5A, 5B, and 5C are similar to corresponding views shown in FIGs. 4A, 4B, and 4C, except the low profile flexible protective dams 114b are substituted for the high profile flexible protective dams 114a on the FRD chip assemblies 104b. In the example shown, the low profile flexible protective dam 114b wraps around a lower perimeter of the chip assembly 104b, underneath the spacer 110b, and between the spacer 110b and the top outer metal layer 102a of the lower DBM structure in the substrate 102.

[0066] In some implementations, outer length and width dimensions L and W of the low profile flexible protective dam 114b can be approximately equal to the size of the spacer 110b such that the low profile flexible protective dam 114b is flush with the sides of the spacer 110b and extends out to, but not around, the lower corner C of the spacer 110b; in some implementations, the low profile flexible protective dam 114b can have a thickness T1 in a range of about -0.2 mm to about 0.3 mm, leaving a small gap in a range of about 0.1 mm to about 0.2 mm between the bottom of the low profile flexible protective dam 114b and the top outer metal layer 102a. In some implementations, the low profile flexible protective dam 114b can include an extension, e.g., an inner flange 500 that is integral to the flexible protective dam 114b. The inner

flange 500 can extend inward and below the edges of the semiconductor die 108b attached to the underside of the spacer 110b. In some implementations, the inner flange 500 can have a thickness T in a range of about 0.09 mm to about 0.1 mm.

[0067] In some implementations, the low profile flexible protective dam 114b can be made of a similar elastic material as the high profile flexible protective dam 114a described above. Depending on its elasticity, the inner flange 500 can form a seal against the top surface of the substrate 102, e.g., against a die attach pad area of the substrate 102. In some implementations, such a sealed inner flange 500 may act as a barrier to block a flow of liquid, e.g., a flow of molten solder used in the assembly process. The inner flange 500 can be used together with the solder resist material 118 as an additional protection to control the flow of solder.

[0068] FIGs. 6A, 6B, and 6C illustrate the high-power semiconductor device module 100 configured with metallic protective dams 114c, according to some implementations of the present disclosure. FIGs. 6A, 6B, and 6C are similar to corresponding views shown above in FIGs. 4A, 4B, and 4C, except the metallic protective dams 114c are substituted for the high profile flexible protective dams 114a on the FRD chip assemblies 104b. In some implementations, the metallic protective dam 114c can be in the form of a rectangular frame that surrounds a lower perimeter of the chip assembly 104b. In some implementations, the metallic protective dam 114c can be slightly spaced apart from the spacer 110b to allow for metal expansion during heating, and contraction when the metallic protective dam 114c relaxes. The metallic protective dams 114c can be soldered to the top outer metal layer 102a of the lower DBC structure in the substrate 102 using a solder layer 600 applied to the underside of the metallic protective dam 114c. In some implementations, the metallic protective dams 114c can be made of copper or another high conductivity metal that can provide additional heat dissipation to draw heat away from the copper spacer 110b and conduct the heat through the solder layer 600, into the thermal mass of the lower DBM. The metallic protective dams 114c may also be resilient so as to relieve mechanical stress from around the lower corners C of the copper spacer 110b and prevent cracking in similar fashion as the flexible protective dams 114a provide stress relief.

[0069] FIG. 6B shows a magnified view of an example of a metallic protective dam 114c, according to some implementations of the present disclosure. In the example shown, the dimensions of the metallic protective dam 114c can be as follows: inner length and width dimensions L and W of the metallic protective dam 114c can be about 0.5 mm larger than the size of the spacer 110b; a wall thickness t of the metallic protective dam 114c can be in a range

of about 0.7 mm to about 0.8 mm; a thickness of the solder layer 600 can be in a range of about 0.2 mm to about 0.3 mm; and a height h of the metallic protective dam 114c can be in a range of about 1.2 mm to about 1.3 mm such that the metallic protective dam 114c covers at least lower portions of the sides of the copper spacer 110b, as is also shown in FIG. 6C. In some implementations, the metallic protective dam 114c can surround larger portions, or all, of the sides of the copper spacer 110b.

[0070] FIG. 6C shows a cross-sectional view of the metallic protective dam 114c applied to the high-power semiconductor device module 100, according to some implementations of the present disclosure. FIG. 6C shows the profile of the metallic protective dam 114c is vertical, not L-shaped, and therefore it does not extend underneath the lower surface of the copper spacer 110b.

[0071] FIGs. 7A, 7B, and 7C illustrate the high-power semiconductor device module 100 configured with integral protective dams 114d, according to some implementations of the present disclosure. FIGs. 7A, 7B, and 7C are similar to corresponding views shown above, except the integral protective dams 114 are substituted for the previous types of protective dams 114 around each of the FRD chip assemblies 104b. In some implementations, the integral protective dam 114d can be in the form of a rectangular frame that surrounds a lower perimeter of the chip assembly 104b and can be slightly spaced apart, laterally, from the spacer 110b. The integral protective dam 114d can be integral to the top outer metal layer 102a of the lower DBC structure in the substrate 102. The integral protective dam 114d can be adjacent to a die attach pad (DAP) onto which the neighboring chip assembly 104a is placed. In some implementations, the integral protective dam 114d can be formed by etching the top outer metal layer 102a, prior to attaching the chip assembly 104a, so that the integral protective dam 114d extends vertically upward, in the z -direction, above the plane of the top outer metal layer 102a. Because the integral protective dam 114d is made of the same material as the top outer metal layer 102a from which it is formed, e.g., copper or another high conductivity metal, the integral protective dam 114d provides additional heat dissipation to draw heat away from the copper spacer 110b and to conduct the heat directly into the thermal mass of the lower DBM. The integral protective dam 114d may also be resilient so as to relieve mechanical stress from around the lower corners C of the copper spacer 110b and prevent cracking in similar fashion as the flexible protective dams 114a and 114b, and/or the metallic protective dam 114c provide stress relief.

[0072] FIG. 7B shows a magnified view of an example of an integral protective dam 114d, according to some implementations of the present disclosure. In the example shown, the

dimensions of the integral protective dam 114d can be as follows: inner length and width dimensions L and W of the integral protective dam 114d can be about 0.5 mm larger than the size of the spacer 110b; a wall thickness t of the integral protective dam 114d can be in a range of about 0.5 mm to about 1.0 mm; and a height h of the integral protective dam 114d can be in a range of about 1.0 to about 2.0 mm such that the integral protective dam 114d covers at least lower portions of the sides of the copper spacer 110b, as is also shown in FIG. 7C. In some implementations, the integral protective dam 114d can surround larger portions, or all, of the sides of the copper spacer 110b.

[0073] FIG. 7C shows a cross-sectional view of the integral protective dam 114d applied to the high-power semiconductor device module 100, according to some implementations of the present disclosure. FIG. 7C shows that the profile of the integral protective dam 114d is a vertical extension of the underlying top outer metal layer 102a of the lower DBM structure. FIG. 7C further illustrates that the chip assembly 104b is disposed inside the integral protective dam 114d, while the chip assembly 104a is disposed outside the integral protective dam 114d. The profile of the integral protective dam 114d is not L-shaped, and therefore it does not extend underneath the lower surface of the copper spacer 110b.

[0074] FIGs. 8A, 8B, and 8C illustrate the high-power semiconductor device module 100 configured with integral protective dams 114e, according to some implementations of the present disclosure. FIGs. 8A, 8B, and 8C are similar to corresponding views shown above, except the integral protective dams 114e are substituted for the previous types of protective dams 114 around the FRD chip assemblies 104b. In some implementations, the integral protective dams 114e can be in the form of a partial wall that surrounds a portion of the lower perimeter of the chip assembly 104b and can be slightly spaced apart, laterally, from the copper spacer 110b. The integral protective dams 114e can be integral to the top outer metal layer 102a of the lower DBC structure in the substrate, formed by etching a recess in the top outer metal layer 102a, prior to attaching the chip assembly 104a, so that the integral protective dams 114e extend vertically upward, in the z-direction, above the plane of the top outer metal layer 102a. Because the integral protective dam 114e is made of the same material as the top outer metal layer 102a from which it is formed, e.g., copper or another high conductivity metal, the integral protective dam 114e provides additional heat dissipation to draw heat away from the copper spacer 110b and to conduct the heat directly into the thermal mass of the lower DBM. The integral protective dam 114e may also be resilient so as to relieve mechanical stress from around the lower corners C of

the copper spacer 110b and prevent cracking in similar fashion as the flexible protective dams 114a and 114b, and/or the metallic protective dams 114c provide stress relief.

[0075] FIG. 8B shows a magnified view of an example of an integral protective dam 114e, according to some implementations of the present disclosure. In the example shown, the dimensions of the integral protective dam 114e can be as follows: inner length and width dimensions L and W of the recess forming the integral protective dam 114e can be about 0.5 mm larger than the size of the spacer 110b; a recess depth d of the recess forming the integral protective dam 114e can be in a range of about 0.5 mm to about 1.0 mm; and a total height h of the copper top outer metal layer 102a can be in a range of about 1.0 mm to about 1.5 mm such that the integral protective dam 114e covers at least the bottom corners C of the copper spacer 110b, as is also shown in FIG. 8C. In some implementations, a deeper recess can be etched in the copper top outer metal layer 102a so that the integral protective dam 114e can surround larger portions, or all, of the sides of the copper spacer 110b.

[0076] FIG. 8C shows a cross-sectional view of the integral protective dam 114e applied to the high-power semiconductor device module 100, according to some implementations of the present disclosure. FIG. 8C shows that the profile of the integral protective dam 114e is an asymmetric vertical extension of the underlying top outer metal layer 102a of the lower DBM structure. That is, unlike the integral protective dam 114d, the integral protective dam 114e does not necessarily surround the copper spacer 110b on all sides. For example, as shown in FIG. 8B, the integral protective dam 114e surrounds the copper spacer 110b on three sides. However, in some implementations, the recess formed in the top outer metal layer 102a can be symmetric so that the integral protective dam 114e does surround the copper spacer 110b on all sides. Further, unlike the implementations described above, the recess formed in the upper layer 102a that defines the integral protective dam 114e encompasses both of the chip assemblies 104a and 104b, not just the diode chip assembly 104b. The profile of the integral protective dam 114e is not L-shaped, and therefore it does not extend underneath the lower surface of the copper spacer 110b.

[0077] FIG. 9 is a flow chart illustrating a method 900 for fabricating the high-power semiconductor device module 100, according to some implementations of the present disclosure. Operations of method 900 can be performed in a different order, or not performed, depending on specific applications. It is noted that method 900 may not produce a complete high-power semiconductor device module 100. Accordingly, it is understood that additional processes can be provided before, during, or after method 900, and that some of these additional processes may be briefly described herein. The operations 902-910 can be carried out to form high-power

semiconductor device modules 100 and to apply protective dams 114a, 114b, 114c, 114d, or 114e according to the implementations described above.

[0078] At 902, the method 900 includes forming the chip assemblies 104 by coupling a semiconductor die to a heat sink for each chip assembly 104. For example, transistor chip assemblies 104a can be fabricated by coupling a copper alloy spacer 110a to each IGBT semiconductor die 108a; and diode chip assemblies 104b can be fabricated by coupling a copper spacer 110b to each FRD semiconductor die 108b.

[0079] At 904, the method 900 includes forming the protective dam 114. When flexible protective dams 114a or 114b are used, operation 904 can include fabricating the flexible protective dam 114 separately and then stretching the flexible protective dam 114 around the diode chip assembly 104b. When a metallic protective dam 114c is used, operation 904 can include soldering the metallic dam 114c onto the substrate 102. When an integral protective dam 114d is used, operation 904 can include etching the top surface of the substrate 102, e.g., a thick top outer metal layer 102a, to remove a layer of metal, so as to leave behind the walled structure of the integral protective dam 114d. When an integral protective dam 114e is used, operation 904 can include etching a recess in the top surface of the substrate 102, e.g., top outer metal layer 102a, to create a recessed copper layer, thereby leaving behind the structure of the integral protective dam 114d.

[0080] At 906, the method 900 includes coupling the substrate 102 to the the lead frame In some implementations, the substrate 102 can be a three-layer DBM, and the top outer metal layer 102a can be coupled to the leads 304 and mounting brackets 306

[0081] At 908, the method 900 includes coupling the chip assemblies 104a and 104b to the substrate 102. In some implementations, the chip assemblies 104 can be coupled to the substrate 102 by the solder layer 116, using a soldering reflow process, a sintering process, or other appropriate process. In some implementations, attaching the chip assemblies 104 to the substrate 102 can be accomplished by mounting, or bonding, the chip assemblies 104 to the substrate 102, e.g., using a bonding adhesive, e.g., a conductive bonding adhesive in place of the solder layer 116. In some implementations, attaching the chip assembly 104b with the flexible protective dam 114b to the substrate 102 includes applying pressure to form a seal between the flange 500 and the substrate 102.

[0082] At 910, the method 900 includes forming the upper DBM 106 over the chip assembly 104. In some implementations, the upper DBM 106 is formed separately and is attached with solder layer 116 to the chip assemblies 104 using a soldering reflow process, a

sintering process, or other appropriate process. In some implementations, attaching the upper DBM 106 to the chip assemblies 104 can be accomplished by mounting, or bonding, upper DBM 106 to the chip assemblies 104, e.g., using a bonding adhesive, e.g., a conductive bonding adhesive in place of the solder layer 116. The operation 910 can be omitted when single-sided cooling is used.

[0083] At 912, the method 900 includes forming wire bonds 404 to connect the substrate 102 to leads 304. A lower end of the wire bond 404 can be soldered to bond pads formed in the substrate 102, e.g., in the top outer metal layer 102a. An upper end of the wire bond 404 can be soldered to a selected one of leads 304, in accordance with a prescribed circuit design. Brackets 306 can be attached to the substrate 102 at structural connection points 800 at the same time as the wire bond 404 connections are made.

[0084] At 914, the method 900 includes encapsulating the high-power semiconductor device module 100 with the molding compound 112 using, for example, an injection molding process. The encapsulation introduces the molding compound 112 into remaining spaces between and around the chip assemblies 104 that are not occupied by electronic components, connections, or the protective dams 114. In some implementations, the upper and lower DBMs define the top and bottom surfaces of the package such that the molding compound 112 does not surround the upper and lower DBMs. External connections can then be made to the top outer metal layers 106a and 102a.

[0085] FIG. 10 shows computer simulation results 1000 of tensile stress reduction in the molding compound 112, according to some implementations of the present disclosure. The tensile stress reduction is observed when the protective dams 114 are applied to the high-power semiconductor device module 100.

[0086] Computer simulations were run on a model of the high-power semiconductor device module 100, to compare calculated stresses at different representative locations of the molding compound 112 for different implementations of the protective dam 114. The results are compared with a high-power semiconductor device module 100 implemented without a protective dam 114. A first data set 1002 is calculated as an overall representation of stress in the molding compound 112; a second data set 1004 is calculated at a representative location in the vicinity of the FRD diode chip assembly 104b; a third data set 1006 is calculated at a representative location near the edge of the spacer 110b of the FRD diode chip assembly 104b; and. The different implementations of the protective dam 114 that were simulated include a soft epoxy version of the flexible protective dam 114a, 114b an enclosed copper protective dam

114c, 114d, and a copper protective dam 114e formed by etching a recess in the top outer metal layer 102a.

[0087] Referring still to FIG. 10, the computer simulations of tensile stress within the molding compound 112, or “EMC tensile stress” show a performance improvement with use of the each of the simulated protective dams 114. The best overall protection, indicated by the first data set 1002, was shown to be associated with the flexible protective dams 114a/114b. In particular, EMC tensile stress can be reduced by about 33.5%, for flexible protective dams having the dimensions specified above, when the flexible protective dams 114a and 114b are made of a soft epoxy material. The computer simulations further indicate that EMC tensile stress can be reduced by about 22.4% using the enclosed copper protective dams 114c/114d regardless of whether the copper protective dam is soldered in place or formed by etching a wall in the copper top outer metal layer 102a. The computer simulations further indicate that EMC tensile stress can be reduced by about 4.2% using an integral protective dam 114e that is formed by etching a recess in the copper top outer metal layer 102a having a recess depth in a range of about 0.5 mm to about 1.0 mm. Results for the second data set 1004 are similar to those for the first data set 1002.

[0088] Referring to the third data set, 1006, near the FRD spacer edge, the best protection, as predicted by the models, can be achieved by using the copper dams 114c/114d, which shows about a 22.7% reduction in EMC stress, compared with about a 10.7% increase in stress with the flexible protective dams 114a/114b and about a 2.8% reduction in stress with the use of the recess-etched integral protective dam 114e. In these cases, the EMC stress does not exceed the strength of the EMC near the FRD spacer edge.

[0089] It will be understood that, in the foregoing description, when an element, such as a layer, a region, or a substrate, is referred to as being on, connected to, electrically connected to, coupled to, or electrically coupled to another element, it may be directly on, connected or coupled to the other element, or one or more intervening elements may be present. In contrast, when an element is referred to as being directly on, directly connected to or directly coupled to another element or layer, there are no intervening elements or layers present. Although the terms directly on, directly connected to, or directly coupled to may not be used throughout the detailed description, elements that are shown as being directly on, directly connected or directly coupled can be referred to as such. The claims of the application may be amended to recite exemplary relationships described in the specification or shown in the figures.

[0090] As used in this specification, a singular form may, unless definitely indicating a particular case in terms of the context, include a plural form. Spatially relative terms (e.g., over, above, upper, under, beneath, below, lower, top, bottom, and so forth) are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. In some implementations, the relative terms above and below can, respectively, include vertically above and vertically below. In some implementations, the term adjacent can include laterally adjacent to or horizontally adjacent to.

[0091] While certain features of the described implementations have been illustrated as described herein, many modifications, substitutions, changes and equivalents will now occur to those skilled in the art. For instance, features illustrated with respect to one implementation can, where appropriate, also be included in other implementations. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the scope of the implementations. It should be understood that they have been presented by way of example only, not limitation, and various changes in form and details may be made. Any portion of the apparatus and/or methods described herein may be combined in any combination, except mutually exclusive combinations. The implementations described herein can include various combinations and/or sub-combinations of the functions, components and/or features of the different implementations described.

WHAT IS CLAIMED IS:

1. An apparatus, comprising:
 - a substrate (102);
 - a chip assembly (104) coupled to the substrate (102), the chip assembly (104) including:
 - a semiconductor die (108),
 - a heat sink, and
 - a molding material (112) coupled to the heat sink; and
 - a protection dam (114) surrounding at least a portion of a perimeter of the chip assembly (104).
2. The apparatus of claim 1, wherein the protection dam (114) is configured to absorb mechanical stress from expansion of the heat sink.
3. The apparatus of claim 1, wherein the protection dam (114) includes a flexible material.
4. The apparatus of claim 3, wherein the protection dam includes a barrier configured to block a flow of solder.
5. The apparatus of claim 3, wherein the protection dam (114) forms a seal against the substrate (102).
6. The apparatus of claim 1, wherein the protection dam (114) includes copper.
7. The apparatus of claim 6, wherein the substrate (102) is a direct bonded metal (DBM) substrate, including a first metal layer (102a), a second metal layer (102c), and an insulating layer (102b) disposed between the first metal layer (102a) and the second metal layer (102c), the protection dam (114) being a recessed copper layer integrated in the first metal layer (102a).
8. The apparatus of claim 6, wherein the chip assembly (104) is a first chip assembly (104a), and further comprising a second chip assembly (104b) coupled to the substrate (102), wherein the protection dam (114) encompasses both chip assemblies (104a, 104b).

9. The apparatus of claim 1, wherein the chip assembly (104) is a first chip assembly (104a), the apparatus further comprising a second chip assembly (104b) coupled to the substrate (102), the second chip assembly (104b) being disposed outside the protection dam (114).
10. The apparatus of claim 1, wherein the semiconductor die (108) is coupled to the heat sink by a sintered layer of silver (Ag) (120).
11. The apparatus of claim 1, wherein the chip assembly (104) is a component of a high-power module (100) configured for use in an automotive system.
12. An apparatus, comprising:
a substrate (102);
a die assembly (104) coupled to the substrate (102), the die assembly (104) including copper components in contact with a polymer layer (112); and
a protection dam (114) disposed around the die assembly (104).
13. The apparatus of claim 12, wherein the protection dam (114) is attached to the substrate (102).
14. The apparatus of claim 12, wherein the protection dam (114) is integrated into the substrate (102).
15. The apparatus of claim 12, wherein the protection dam (114) includes a recessed area of the substrate (102).
16. The apparatus of claim 12, wherein the protection dam (114) includes an extension configured as a solder barrier (116).
17. A method, comprising:
forming a chip assembly (104) that includes a semiconductor die (108) and a copper spacer (110b);
forming a protective dam (114) around the chip assembly (104);
coupling a substrate (102) to a lead frame;
coupling the chip assembly (104) to the substrate (102);

forming a direct bond metal (DBM) layer above the chip assembly (104);
forming wire bonds (404) to leads (304) of the lead frame; and
filling remaining space around the chip assembly (104) with a molding compound (112).

18. The method of claim 17, wherein forming the protective dam (114) around the chip assembly (104) includes attaching the protective dam (114) to the substrate (102).

19. The method of claim 18, wherein the protective dam (114) is flexible and attaching the protective dam (114) to the substrate (102) includes applying pressure to the protective dam (114).

20. The method of claim 17, wherein attaching the protective dam (114) to the substrate (102) includes applying an adhesive.

21. The method of claim 17, wherein the protective dam (114) is metallic and attaching the protective dam (114) to the substrate (102) includes soldering.

22. The method of claim 21, wherein forming the protective dam (114) comprises forming a solder barrier (116) integral to the protective dam (114).

23. A method, comprising:

 fabricating a chip assembly (104) that includes a semiconductor die (108) and a copper spacer (110b);
 etching a recessed area in a surface metal layer of a substrate (102) to form a protective dam (114);
 coupling the chip assembly (104) to the substrate (102) inside the protective dam (114);
 forming a direct bond metal (DBM) layer (106a) above the chip assembly (104); and
 filling remaining space around the chip assembly (104) with a molding compound (112).

24. The method of claim 23, further comprising coupling additional chip assemblies (104) to the substrate (102), and wherein etching the recessed area forms a protective dam (114) around at least one of the additional chip assemblies (104).