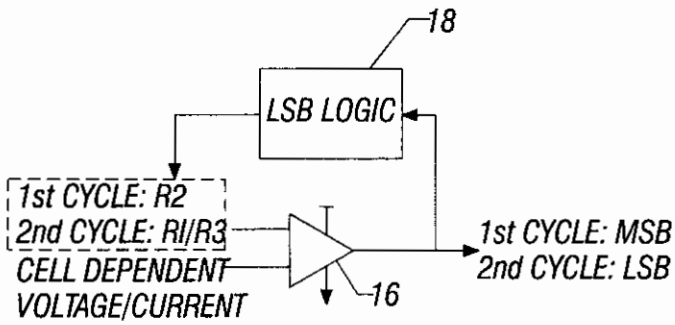
18
LSB LOGIC
1st CYCLE: R2
2nd CYCLE: RI/R3
CELL DEPENDENT
VOLTAGE/CURRENT
16
1st CYCLE: MSB
2nd CYCLE: LSB

FIG. 1

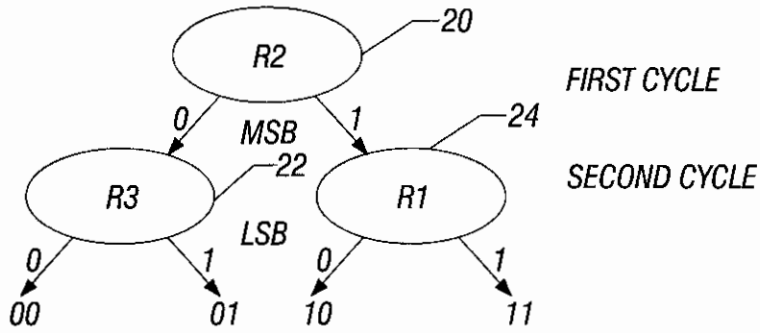
R2
20
FIRST CYCLE
0
MSB
1
24
R3
22
R1
SECOND CYCLE
LSB
0
1
0
1
00
01
10
11

FIG. 2

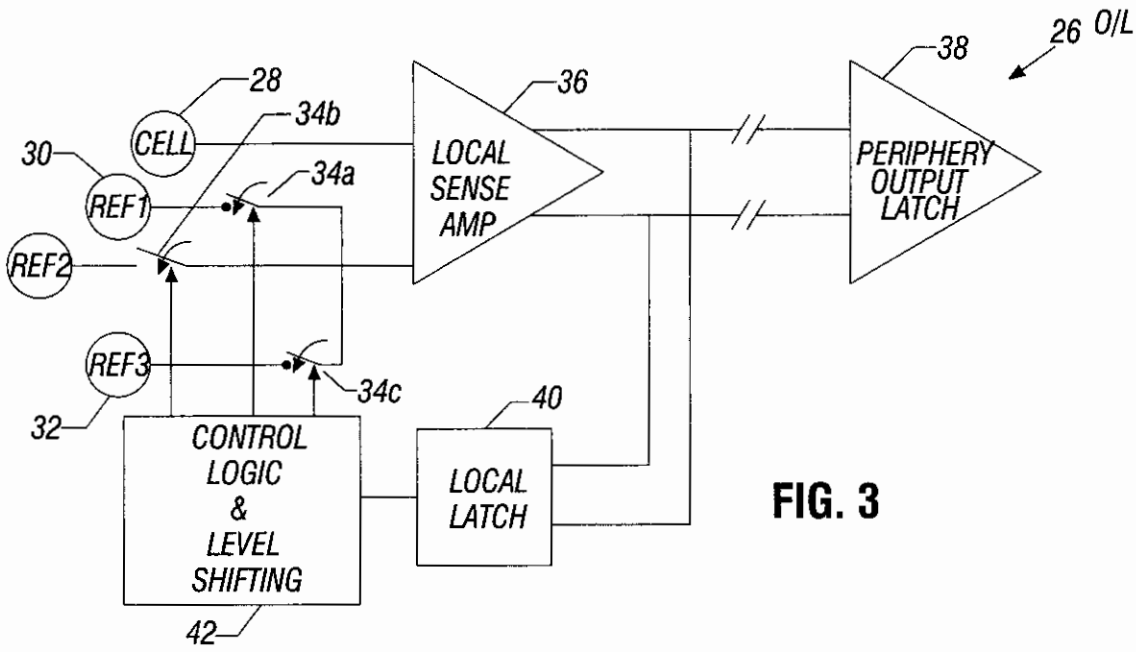
26 O/L
38
28
36
34b
CELL
30
LOCAL SENSE AMP
PERIPHERY OUTPUT LATCH
34a
REF1
REF2
REF3
34c
40
32
CONTROL LOGIC & LEVEL SHIFTING
LOCAL LATCH
42

FIG. 3

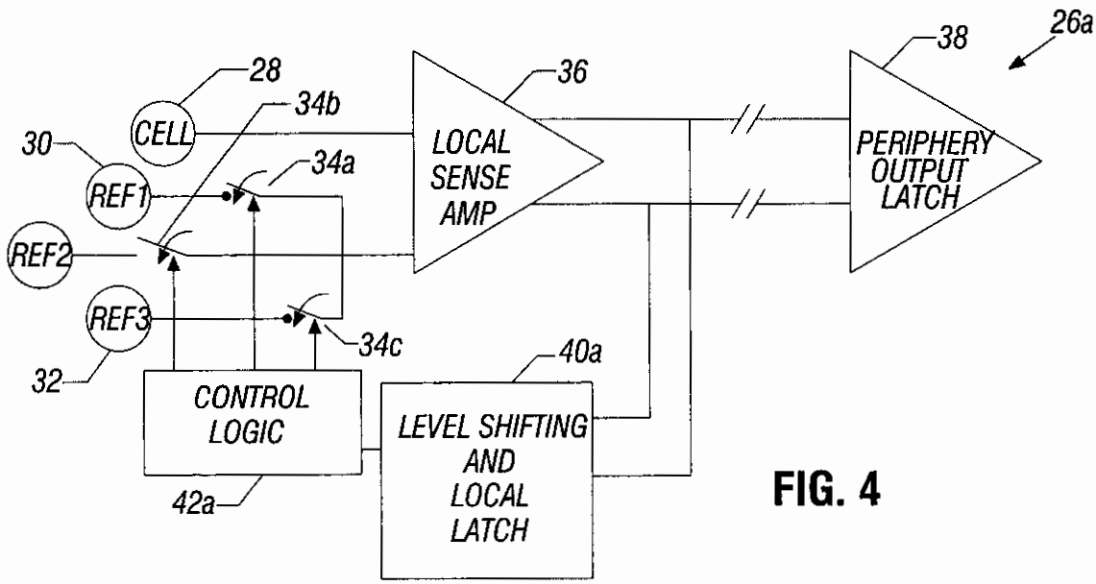
26a
38
28
36
34b
CELL
30
LOCAL SENSE AMP
PERIPHERY OUTPUT LATCH
34a
REF1
REF2
REF3
34c
40a
32
CONTROL LOGIC
LEVEL SHIFTING AND LOCAL LATCH
42a

FIG. 4

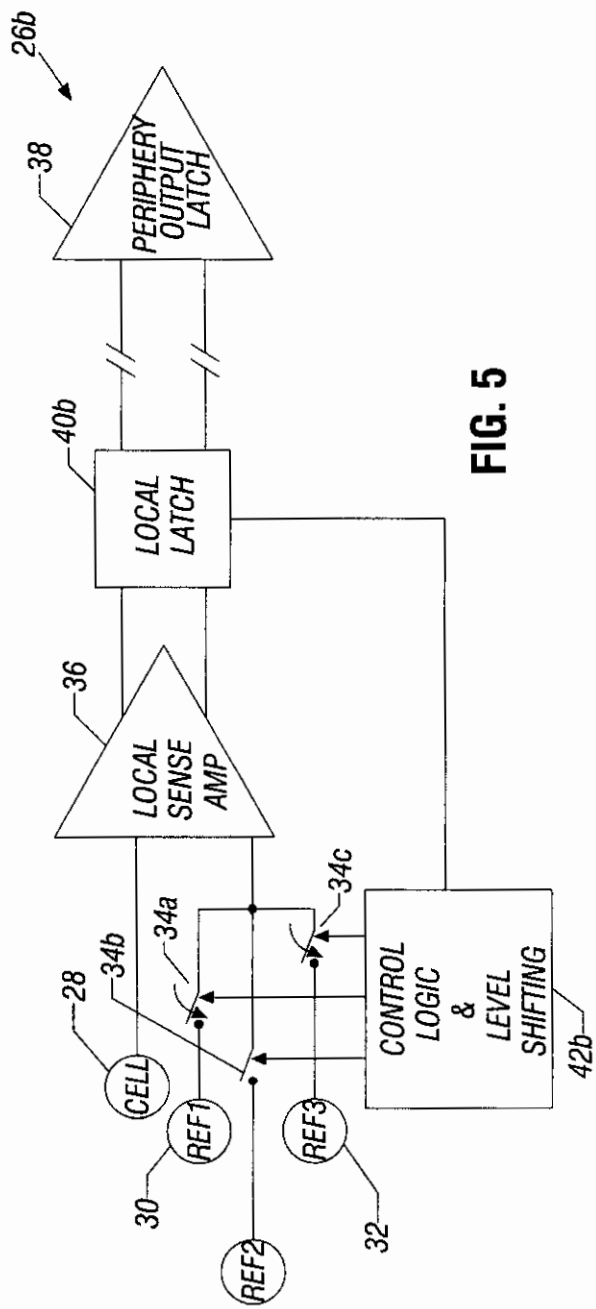
26b
38
PERIPHERY OUTPUT LATCH
40b
LOCAL LATCH
36
LOCAL SENSE AMP
34c
34a
34b
28
CELL
REF1
REF3
REF2
30
32
CONTROL LOGIC & LEVEL SHIFTING
42b

FIG. 5

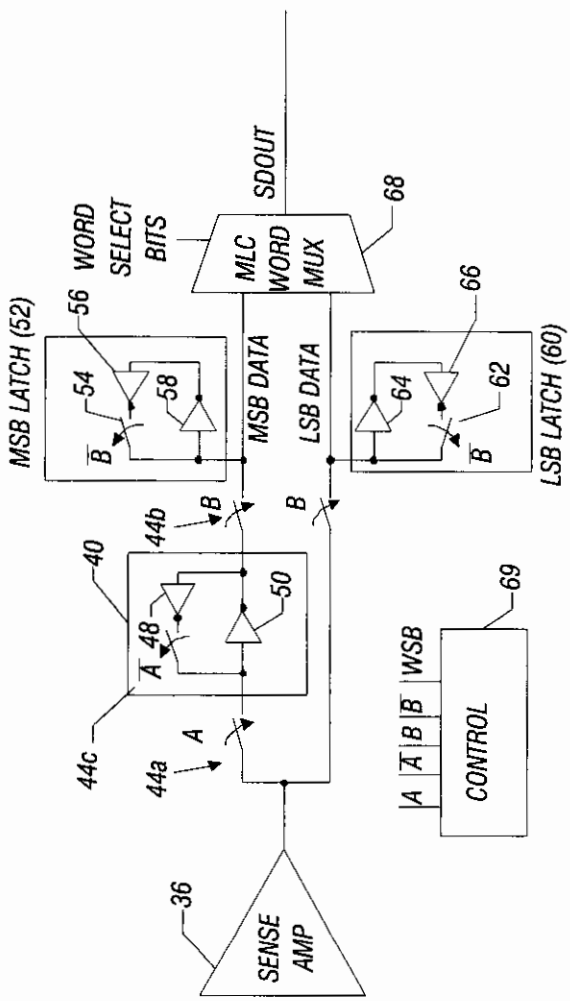
SDOUT
68
MLC WORD MUX
WORD SELECT BITS
MSB LATCH (52)
56
54
58
B
MSB DATA
LSB DATA
66
64
62
B
LSB LATCH (60)
B
B
44b
40
50
48
A
44c
A
44a
69
WSB
B
B
A
A
CONTROL
36
SENSE AMP

FIG. 6

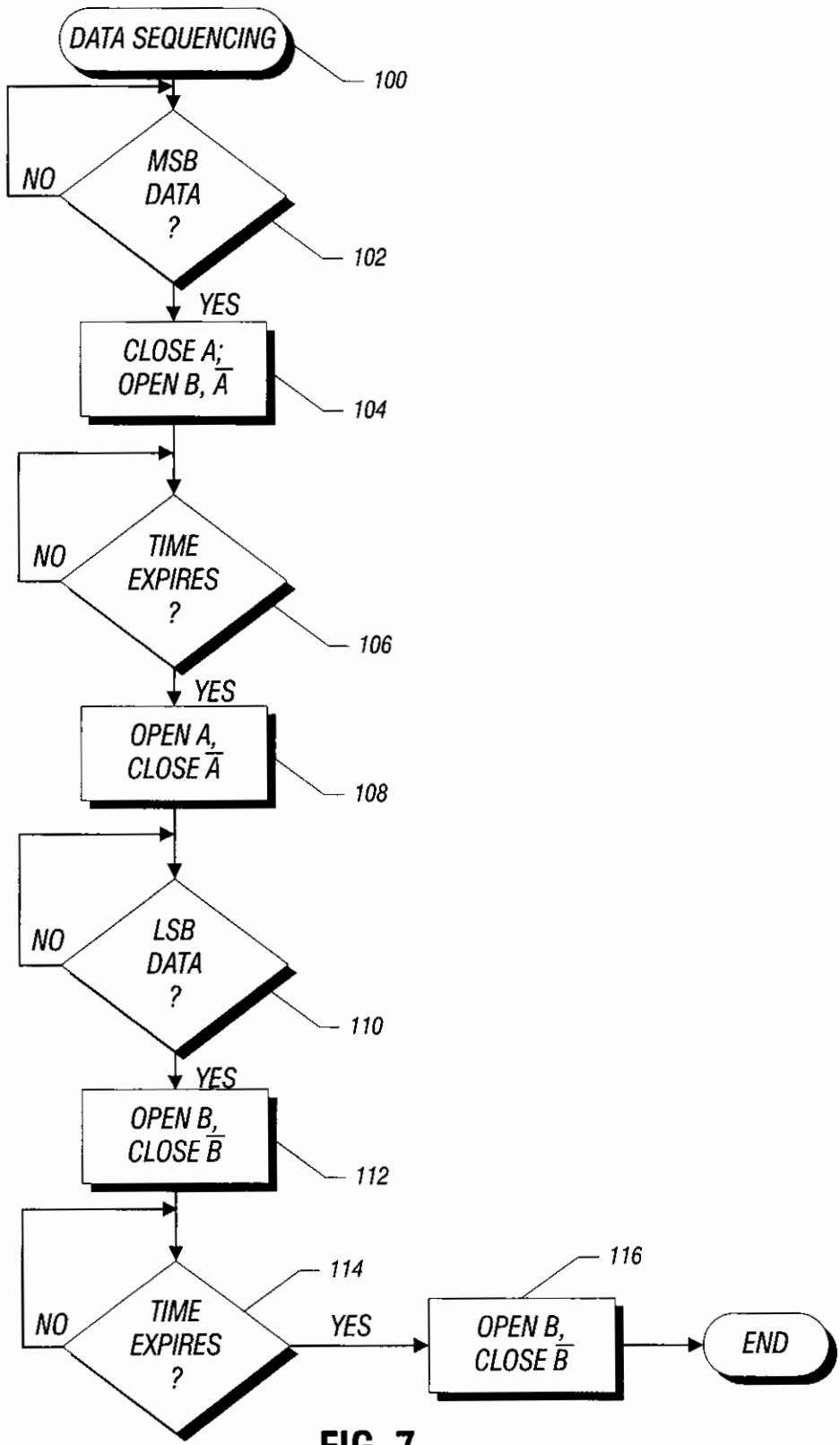
DATA SEQUENCING
100
MSB DATA ?
NO
102
YES
CLOSE A; OPEN B, $\overline{A}$
104
TIME EXPIRES ?
NO
106
YES
OPEN A, CLOSE $\overline{A}$
108
LSB DATA ?
NO
110
YES
OPEN B, CLOSE $\overline{B}$
112
TIME EXPIRES ?
NO
114
YES
OPEN B, CLOSE $\overline{B}$
116
END

FIG. 7

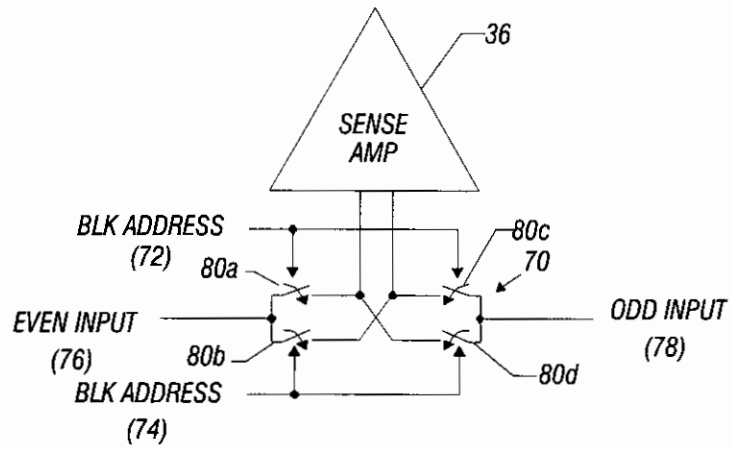
36
SENSE AMP
BLK ADDRESS (72)
80a
80c
70
EVEN INPUT (76)
80b
ODD INPUT (78)
80d
BLK ADDRESS (74)

FIG. 8

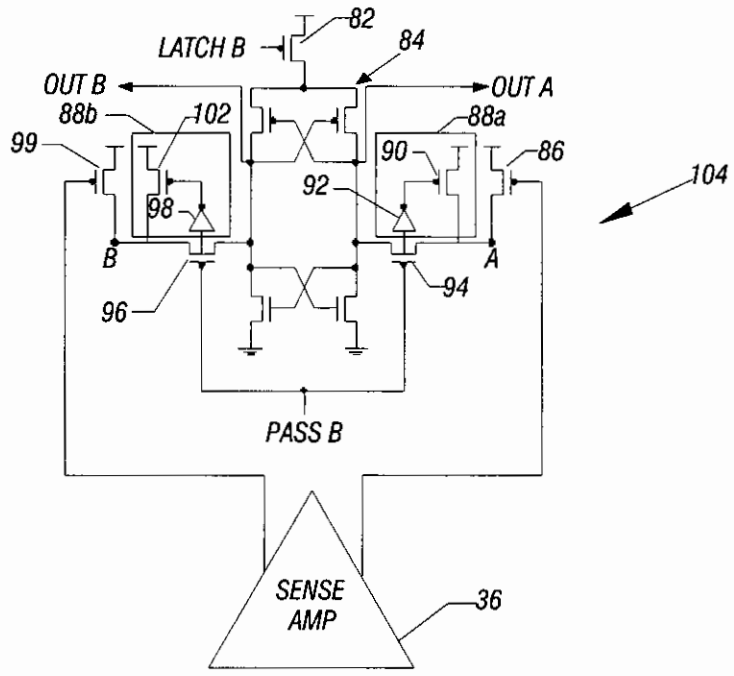
82
LATCH B
84
OUT B
OUT A
88b
102
88a
99
90
86
104
92
98
B
A
96
94
PASS B
SENSE AMP
36

FIG. 9