(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
12 May 2005 (12.05.2005)

PCT

(10) International Publication Number
WO 2005/043625 A3

(51) International Patent Classification[7]: H01L 27/146

(21) International Application Number:
PCT/US2004/034370

(22) International Filing Date: 19 October 2004 (19.10.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/689,948 22 October 2003 (22.10.2003) US

(71) Applicant *(for all designated States except US)*: **MICRON TECHNOLOGY, INC.** [US/US]; 8000 S. Federal Way, Boise, ID 83707-0006 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **RHODES, Howard, E.** [US/US]; 631 E. Ridgefield Drive, Boise, ID 83706 (US).

(74) Agent: **D'AMICO, Thomas, J.**; Dickstein Shapiro Morin & Oshinsky LLP, 2101 L Street NW, Washington, DC 20037-1526 (US).

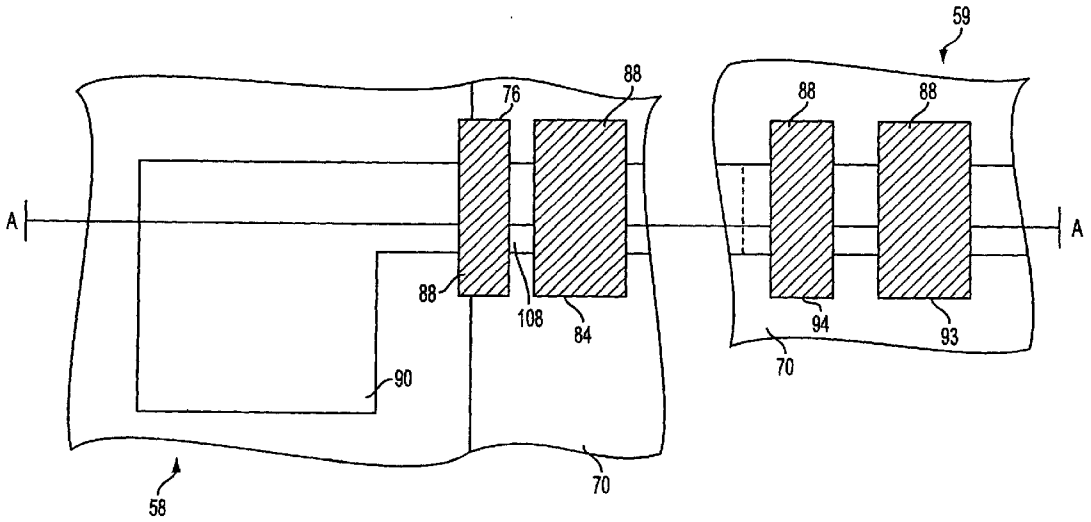
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) Title: DUAL CAPACITOR STRUCTURE FOR IMAGERS AND METHOD OF FORMATION



(57) Abstract: CMOS and CCD imaging devices comprising different in-pixel capacitors and peripheral capacitors and methods of formation are disclosed. The capacitors used in periphery circuits have different requirements from the capacitors used in the pixel itself. Dual stack capacitors comprising two dielectric layers may be provided to achieve low leakage and high capacitance. A single masking step may be provided such that one region has a dual dielectric capacitor and a second region has a single dielectric capacitor. A different dielectric may also be provided in one region compared to another region wherein the inter-electrode insulator comprises a single dielectric in both regions.

WO 2005/043625 A3

(88) Date of publication of the international search report:
1 September 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.