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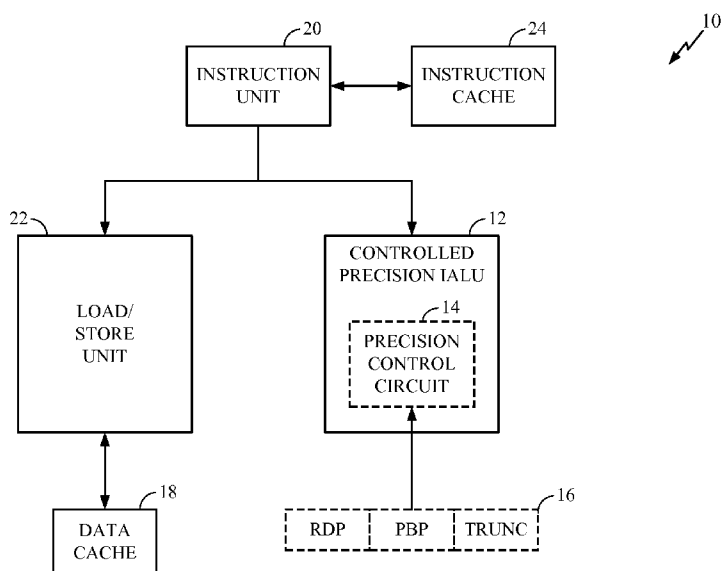
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(54) Title: CONTROLLED-PRECISION ITERATIVE ARITHMETIC LOGIC UNIT



(57) Abstract: A controlled-precision Iterative Arithmetic Logic Unit (IALU) included in a processor produces sub-precision results, i.e. results having a bit precision less than full precision. In one embodiment, the controlled-precision IALU comprises an arithmetic logic circuit and a precision control circuit. The arithmetic logic circuit is configured to iteratively process operands of a first bit precision to obtain a result. The precision control circuit is configured to end the iterative operand processing when the result achieves a programmed second bit precision less than the first bit precision. In one embodiment, the precision control circuit causes the arithmetic logic circuit to end the iterative operand processing in response to an indicator received by the control circuit. The controlled-precision IALU further comprises rounding logic configured to round the sub-precision result.



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