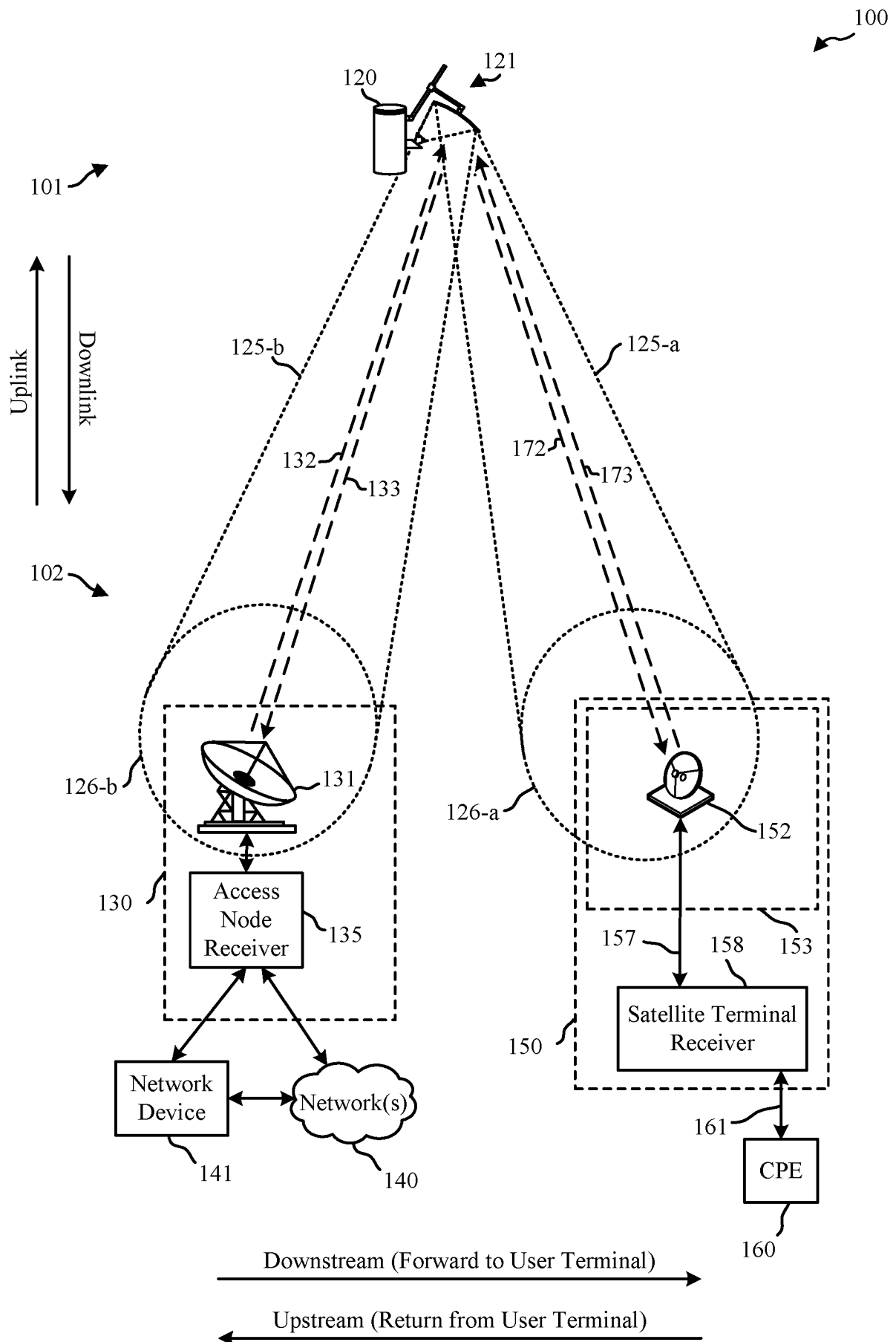




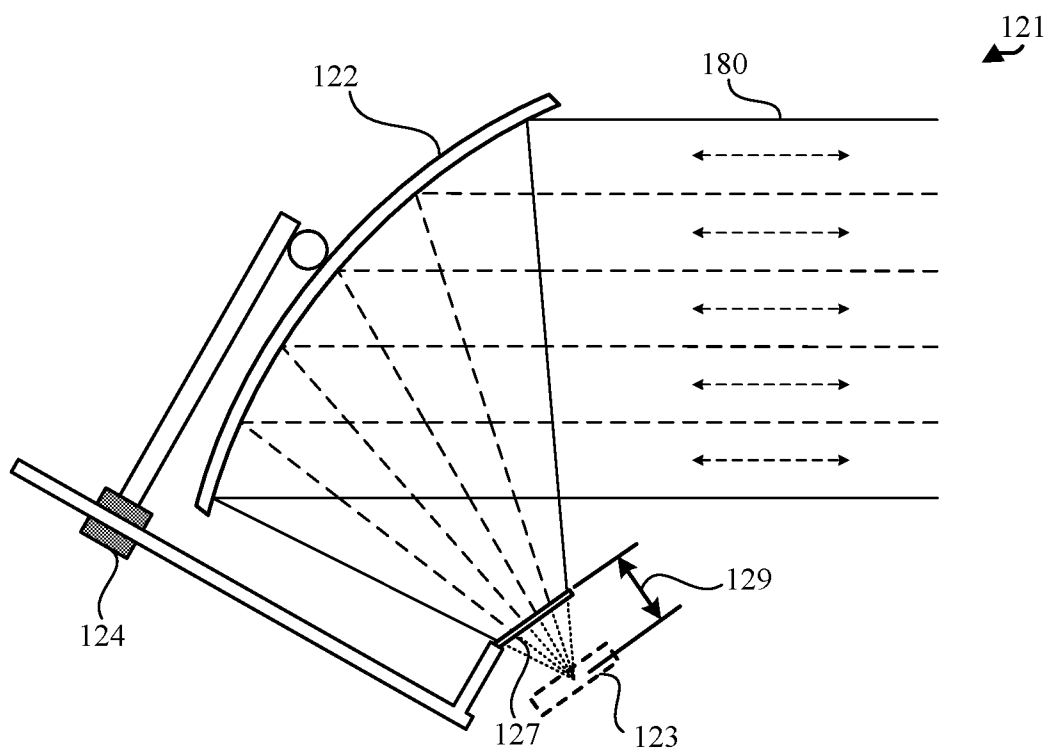


FIG. 1B

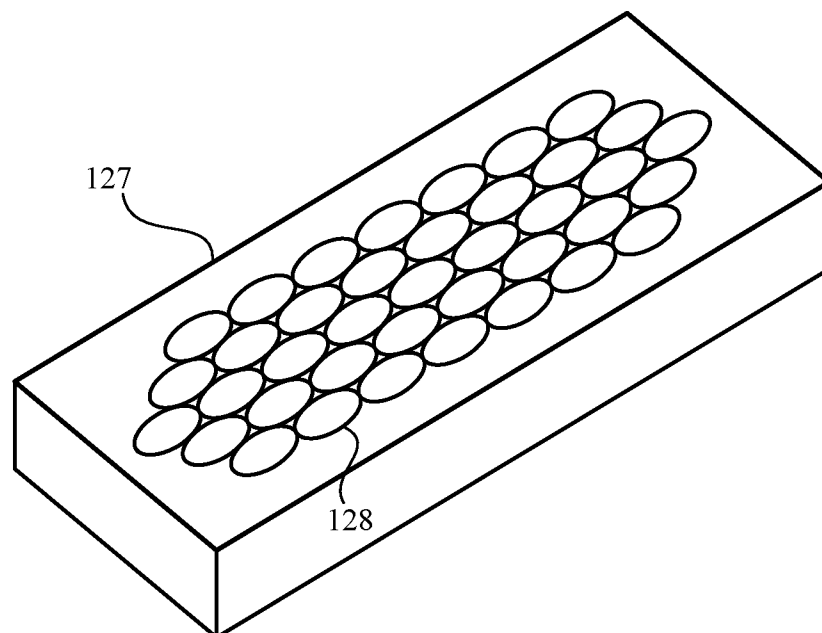


FIG. 1C

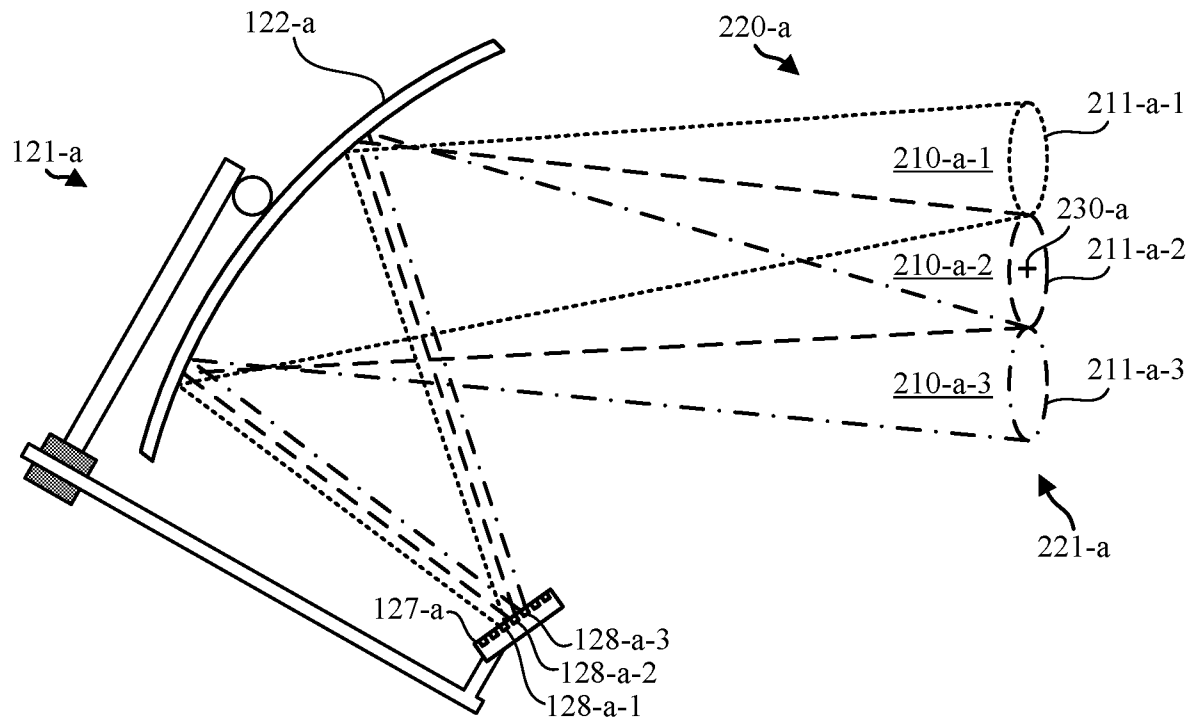


FIG. 2A

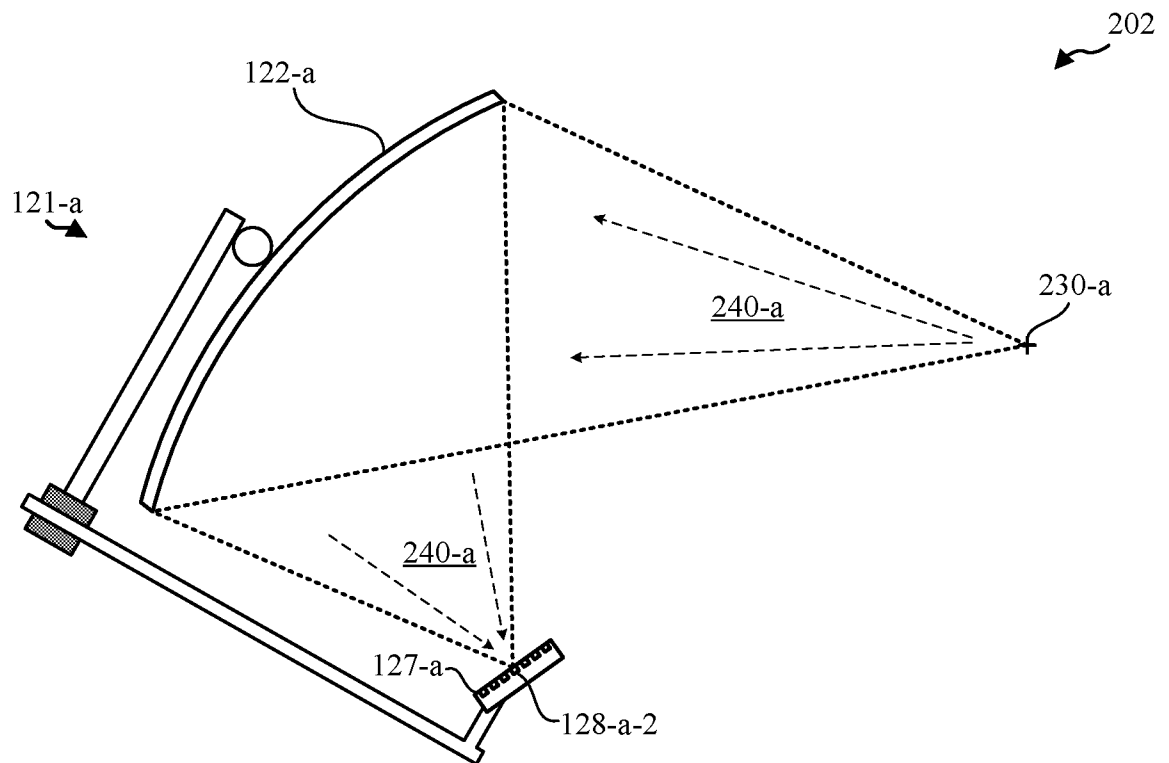


FIG. 2B

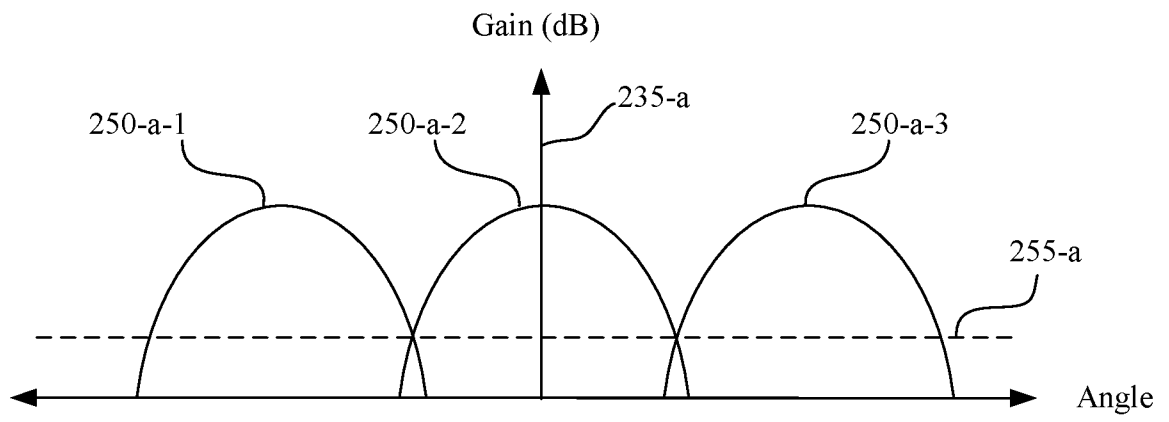
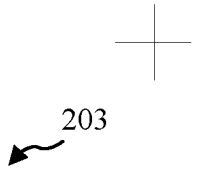


FIG. 2C

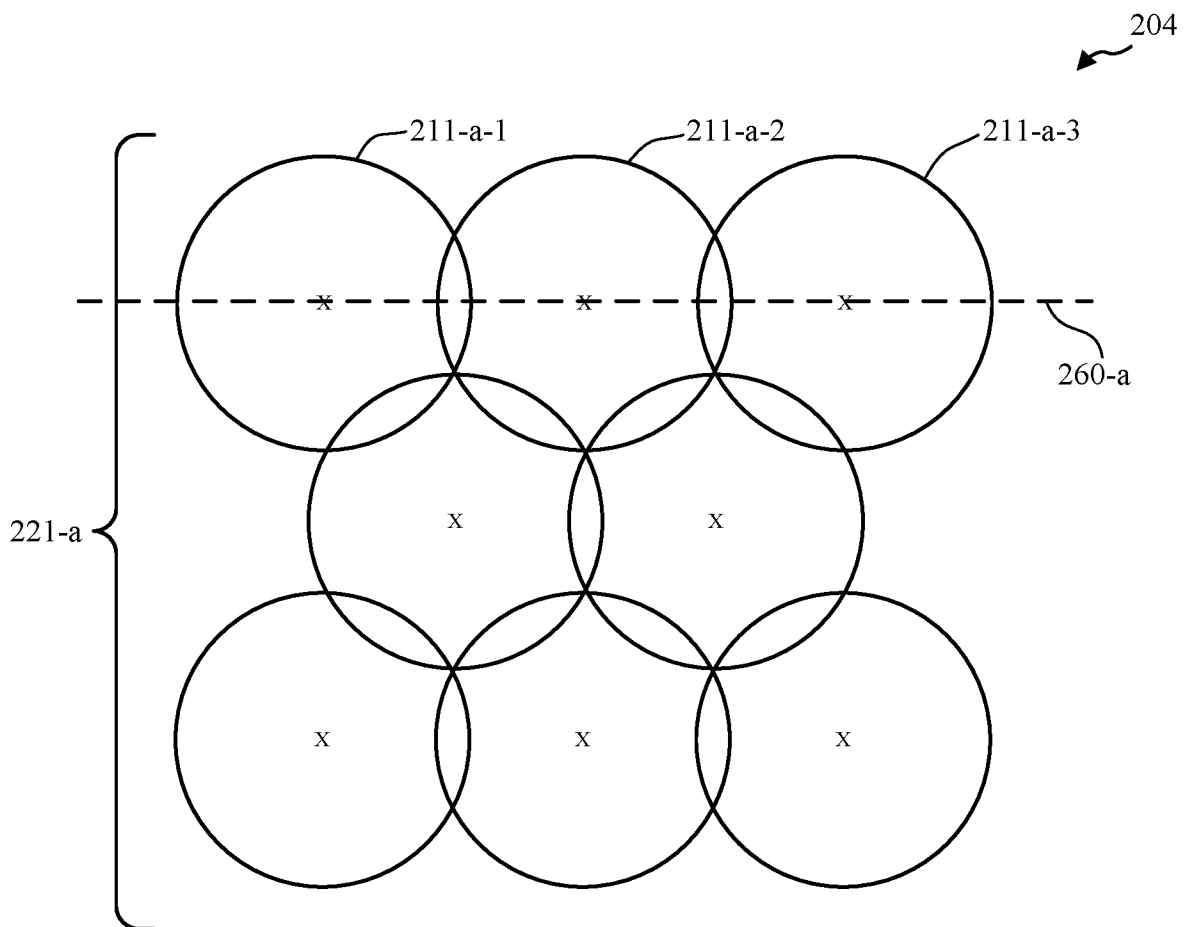


FIG. 2D



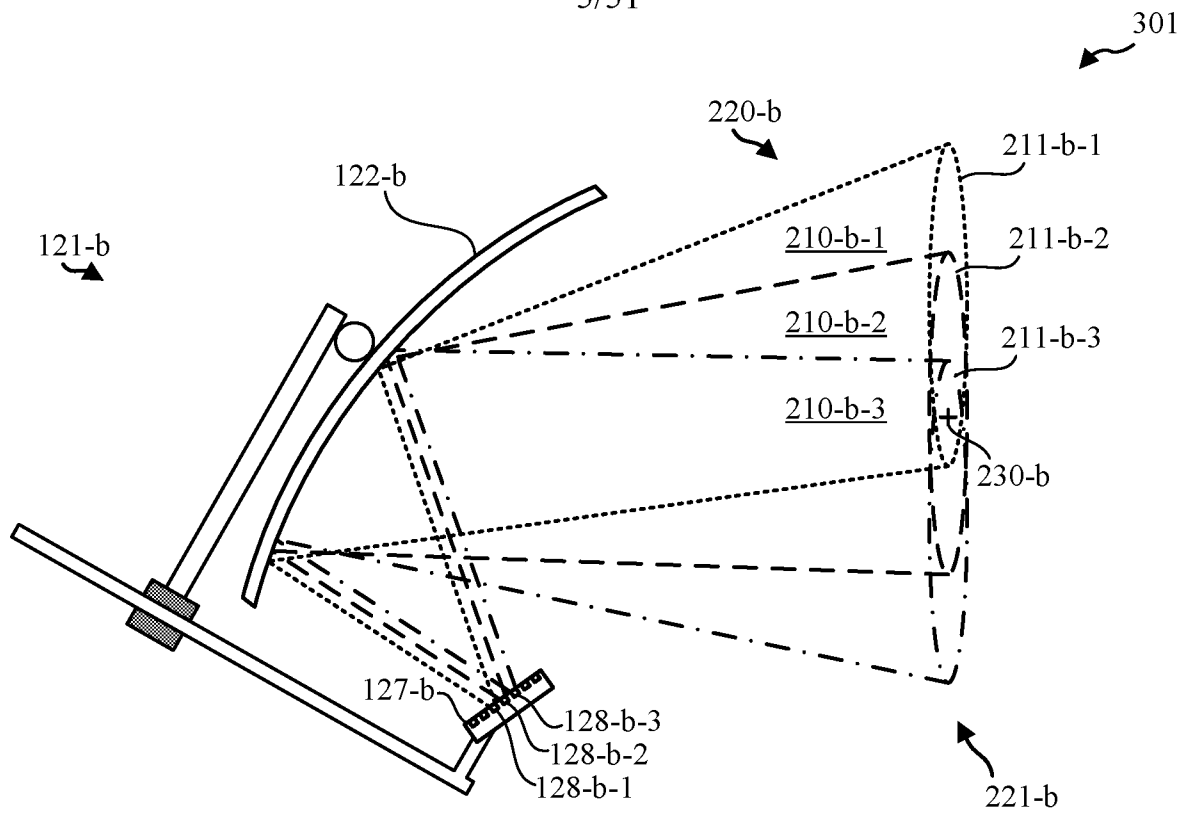


FIG. 3A

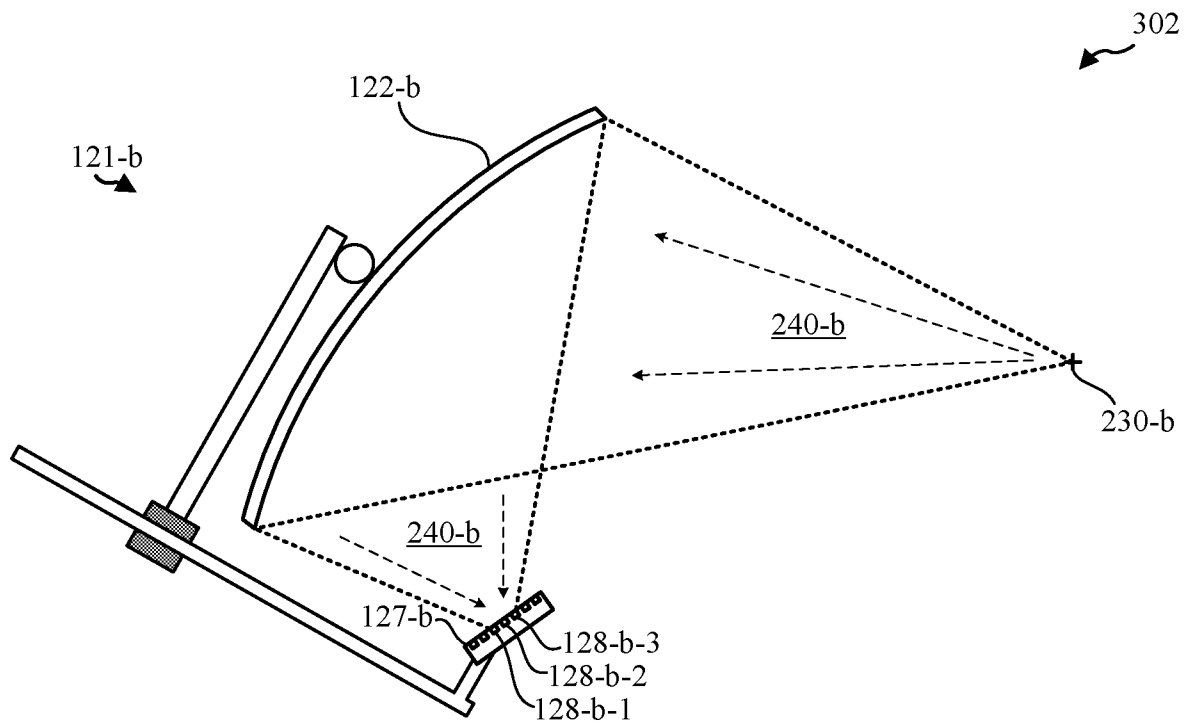


FIG. 3B

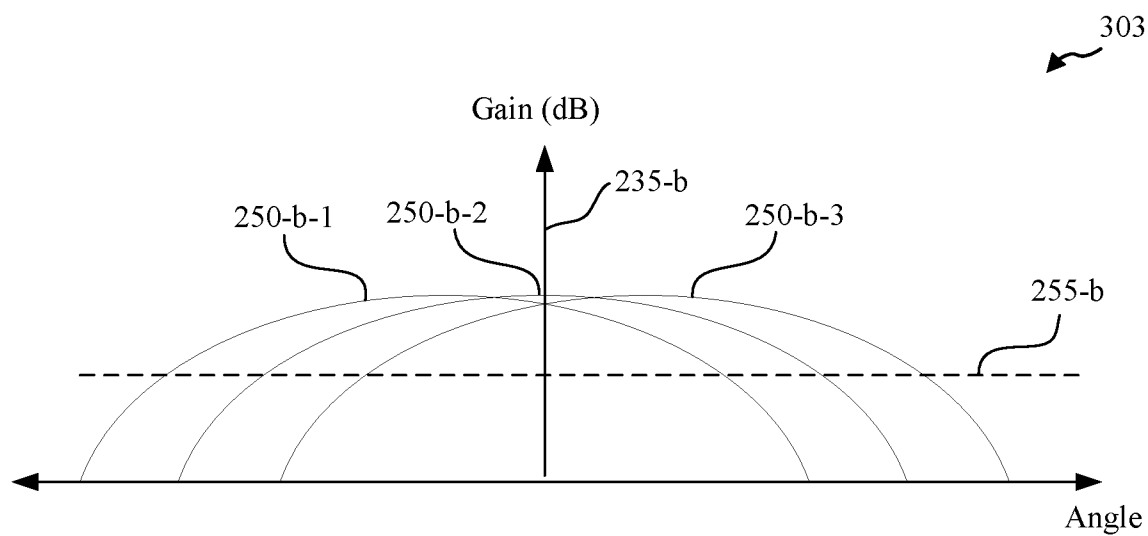


FIG. 3C

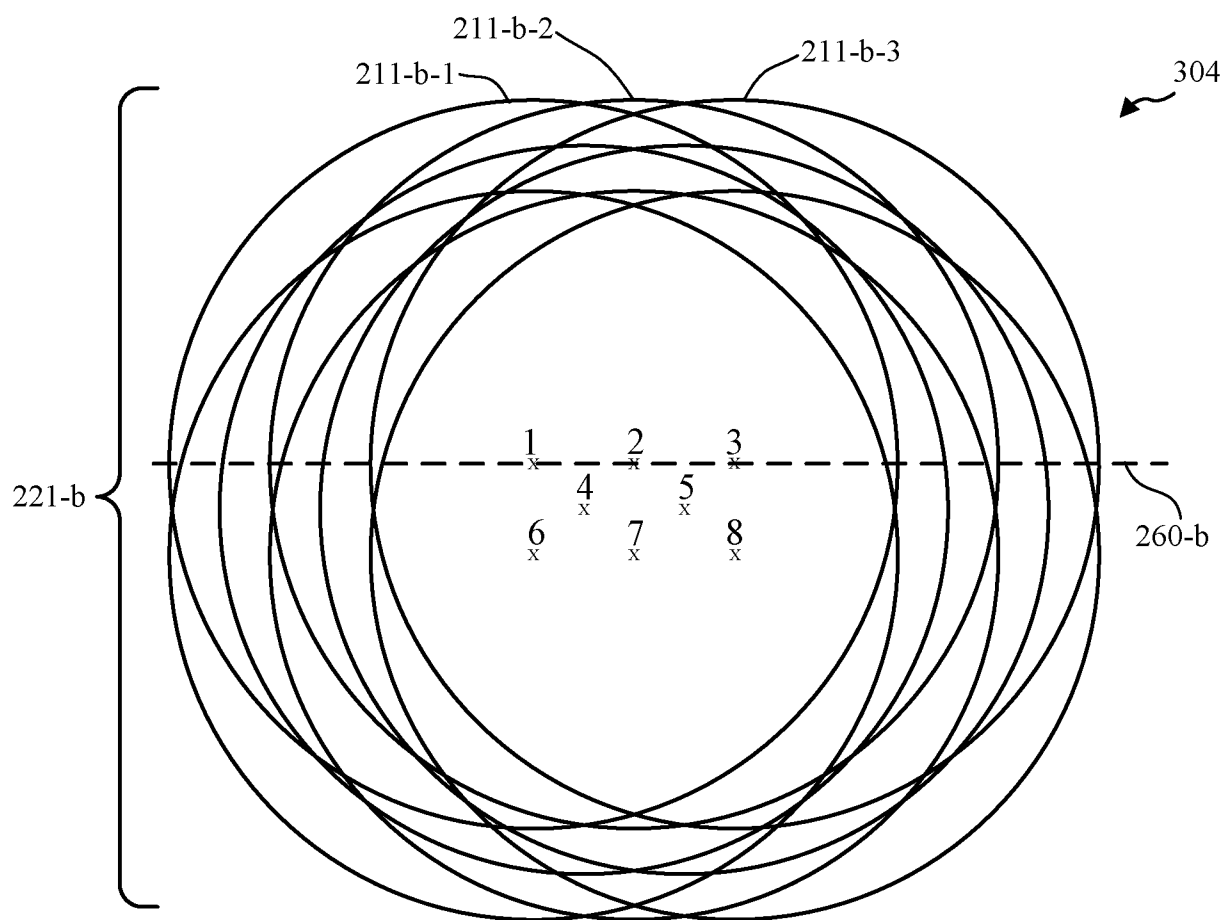


FIG. 3D

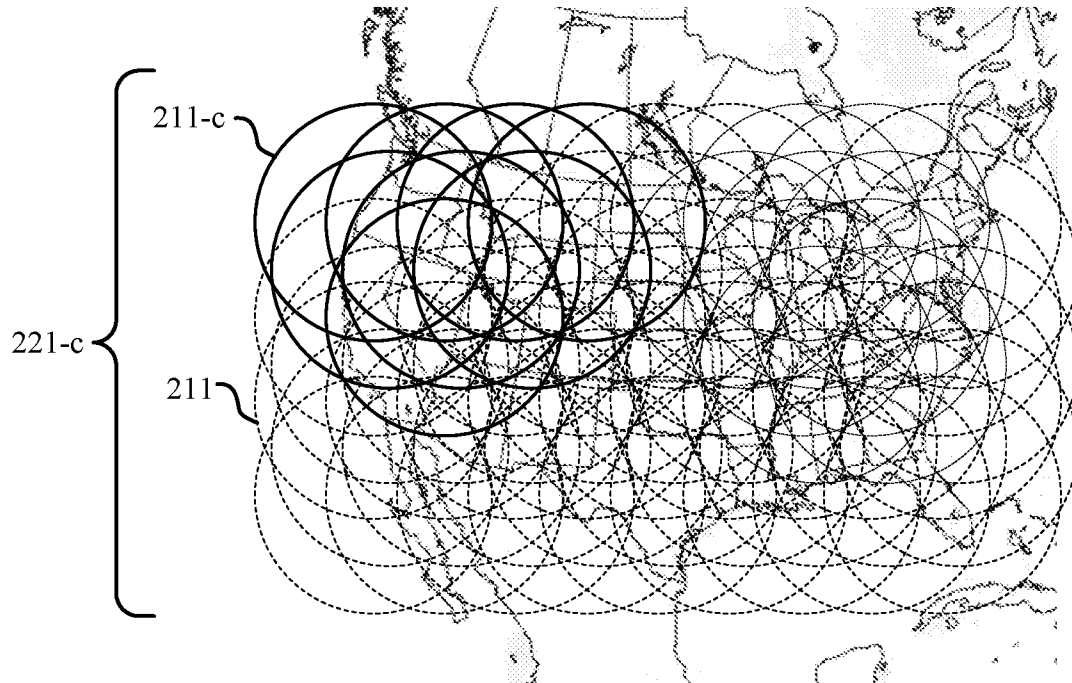
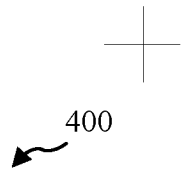


FIG. 4A

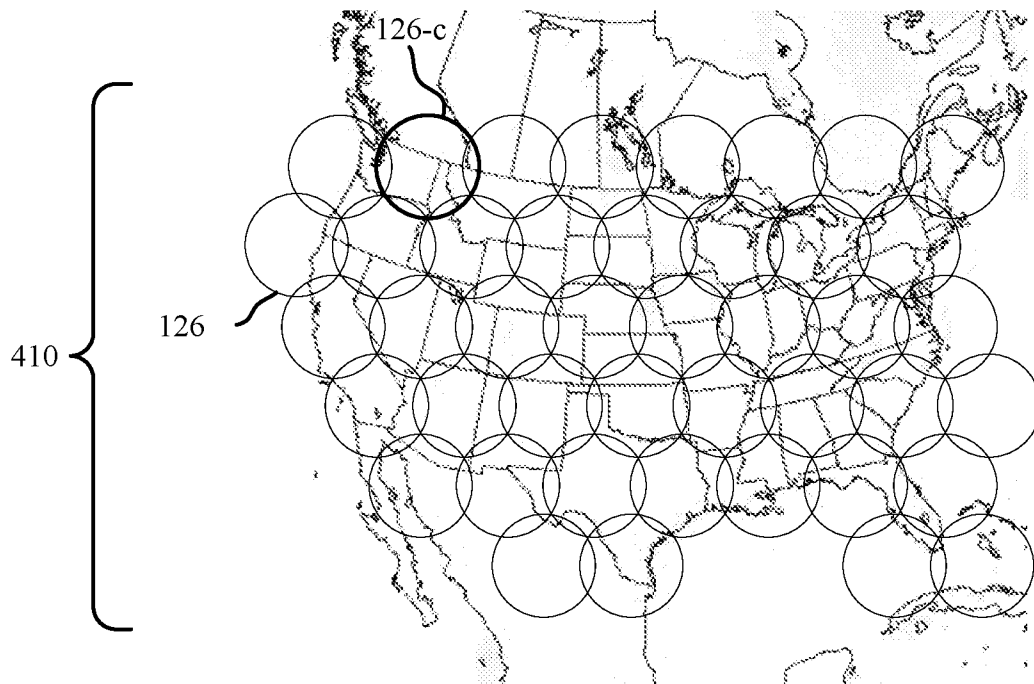
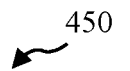


FIG. 4B



500

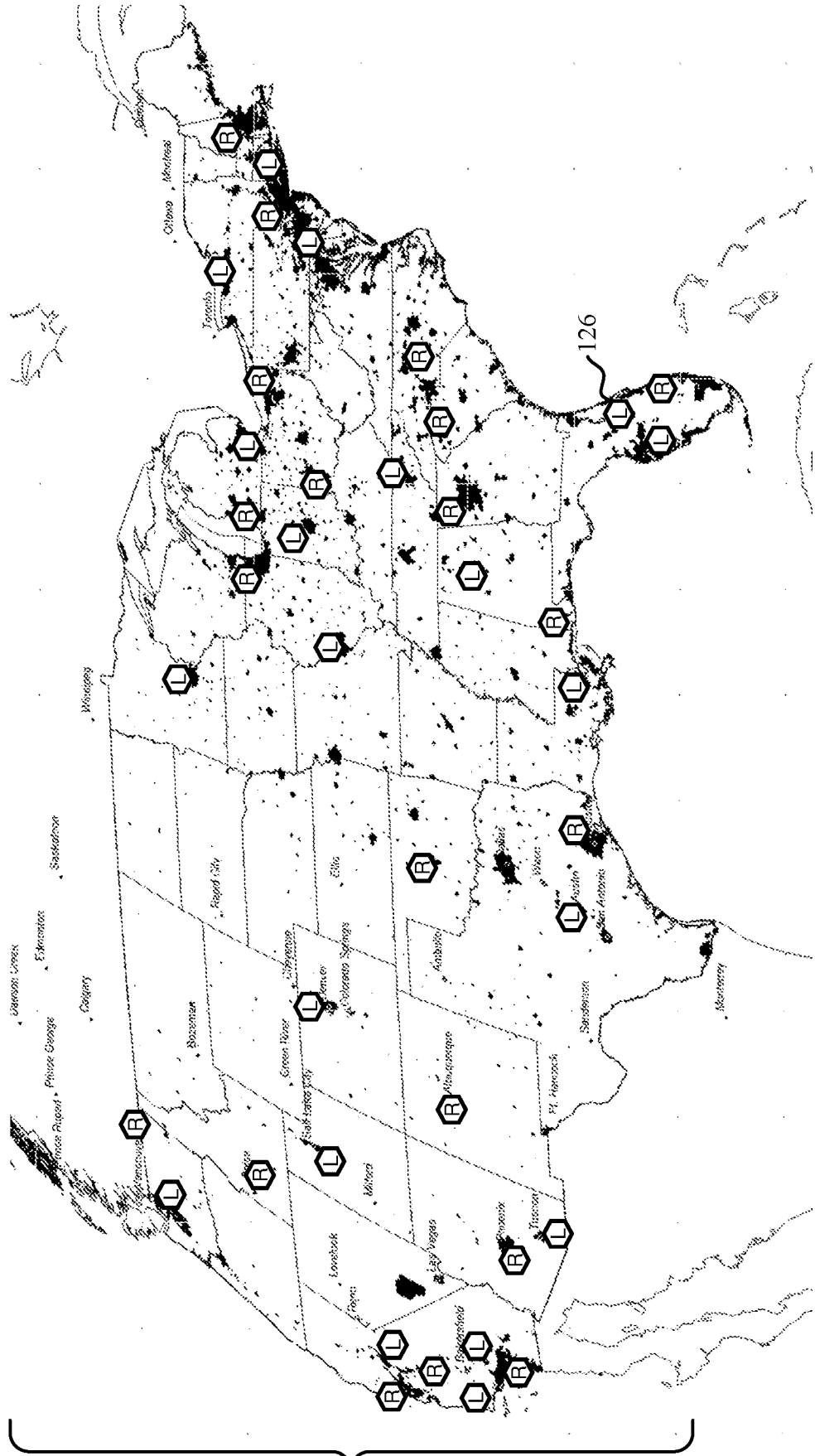


FIG. 5A

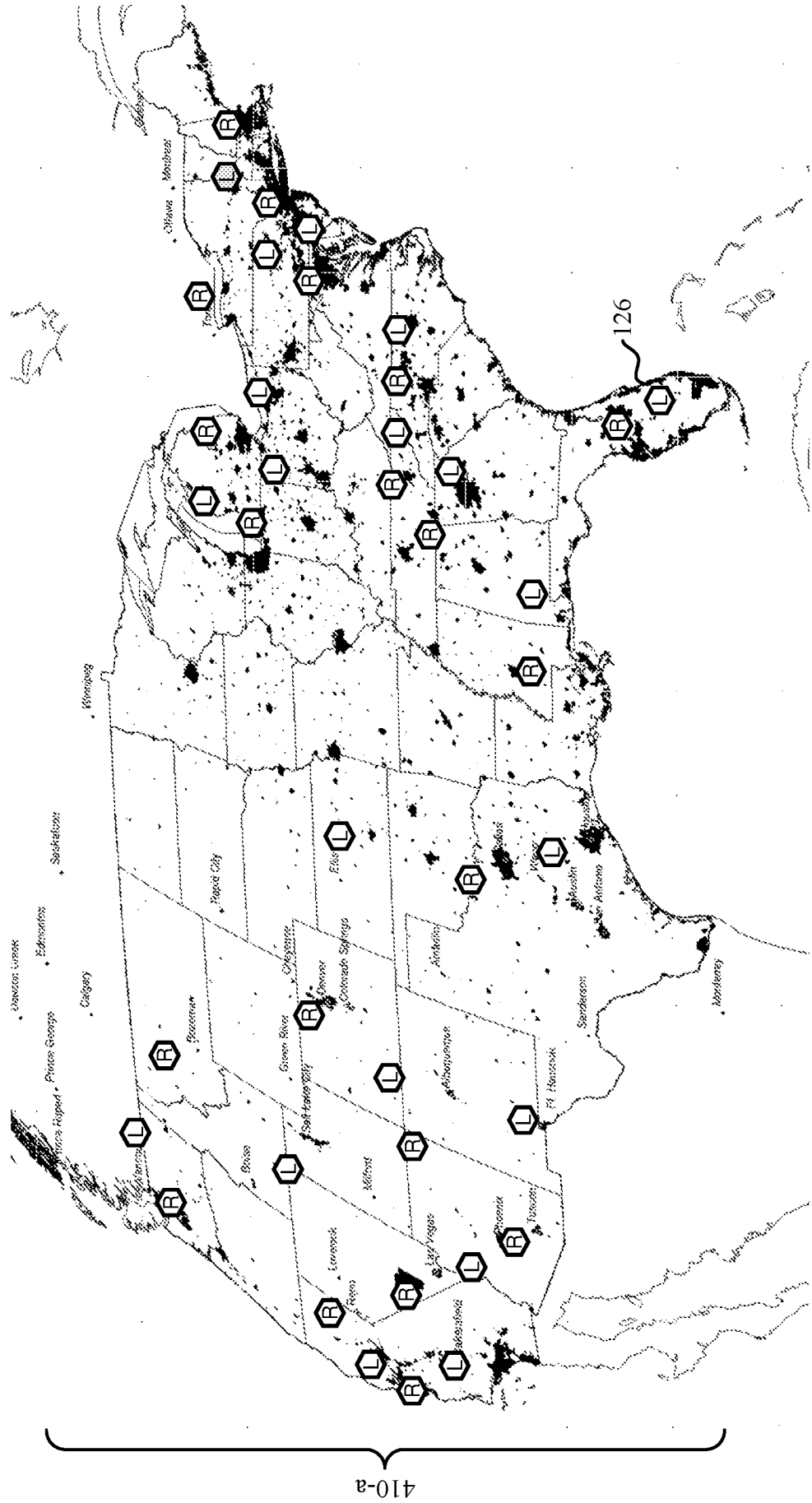


FIG. 5B

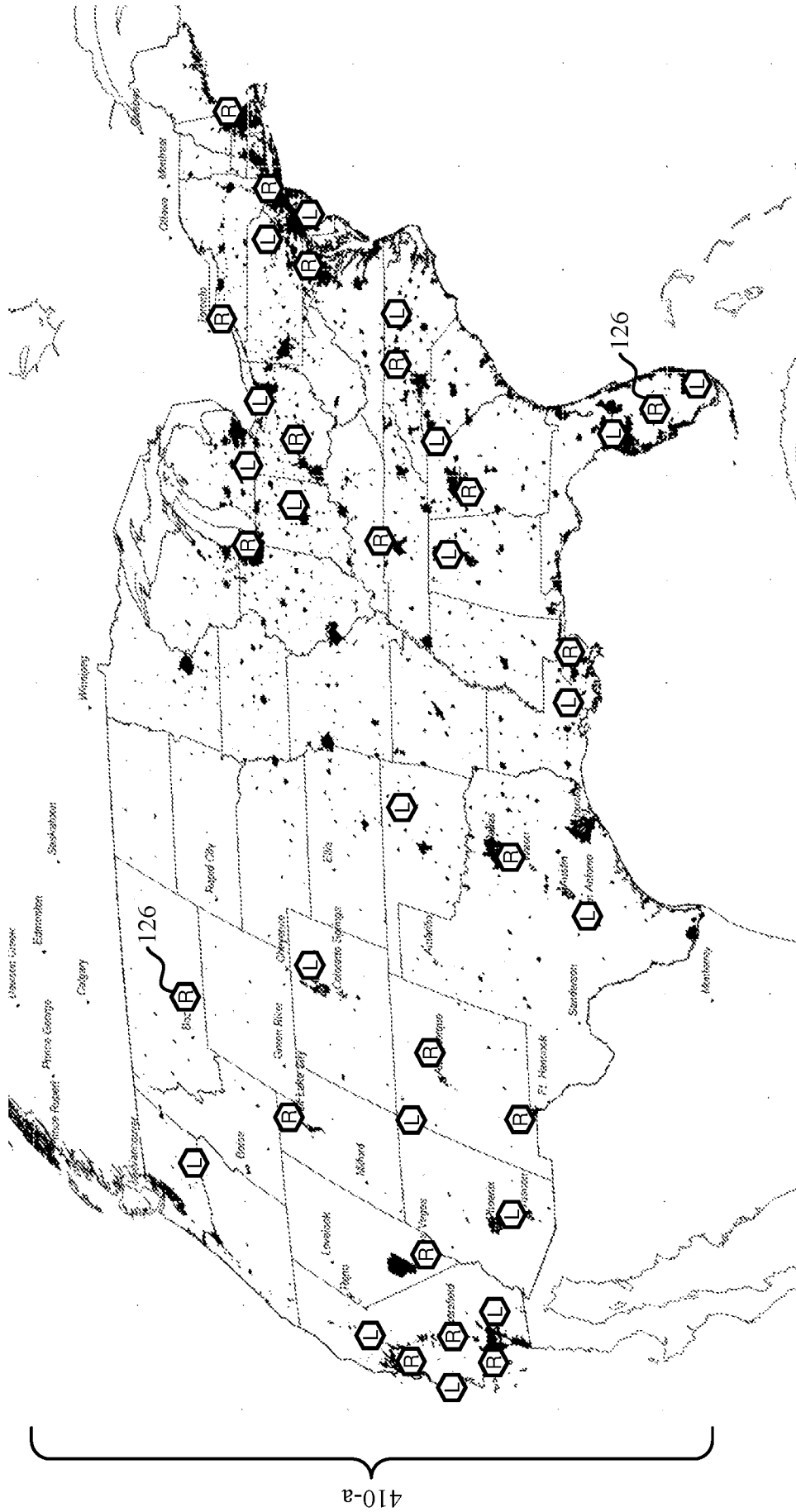


FIG. 5C

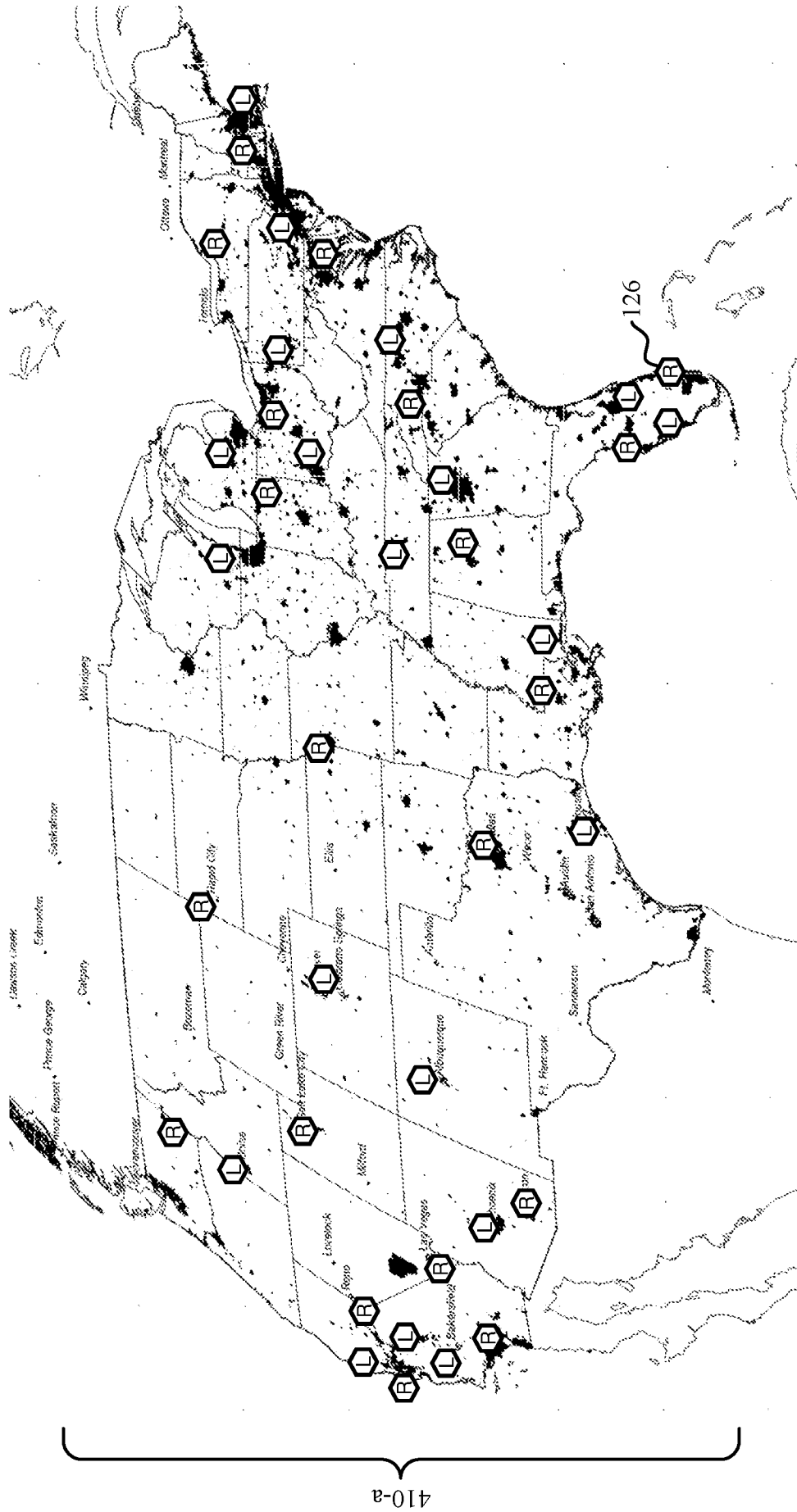


FIG. 5D

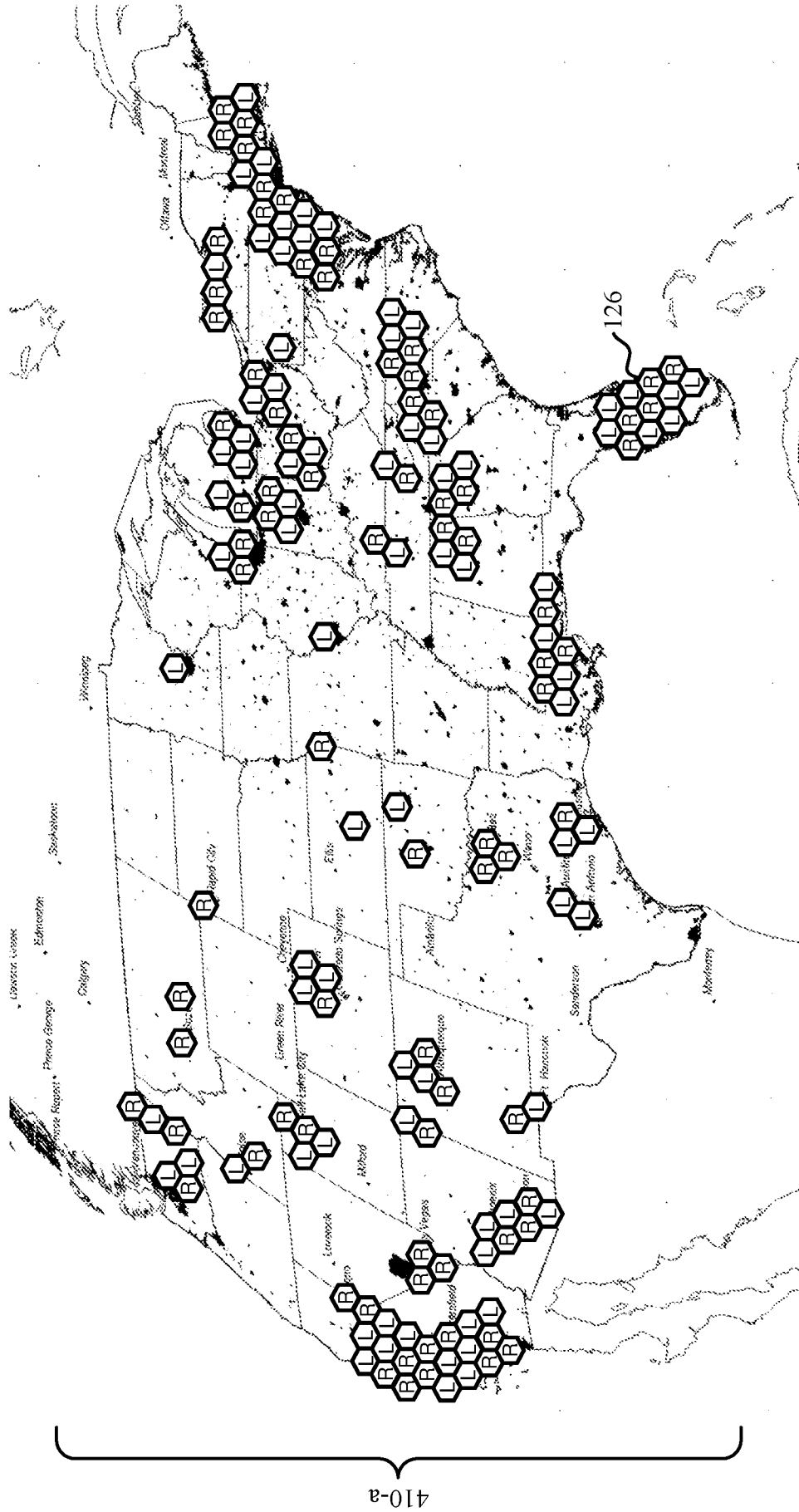


FIG. 5E

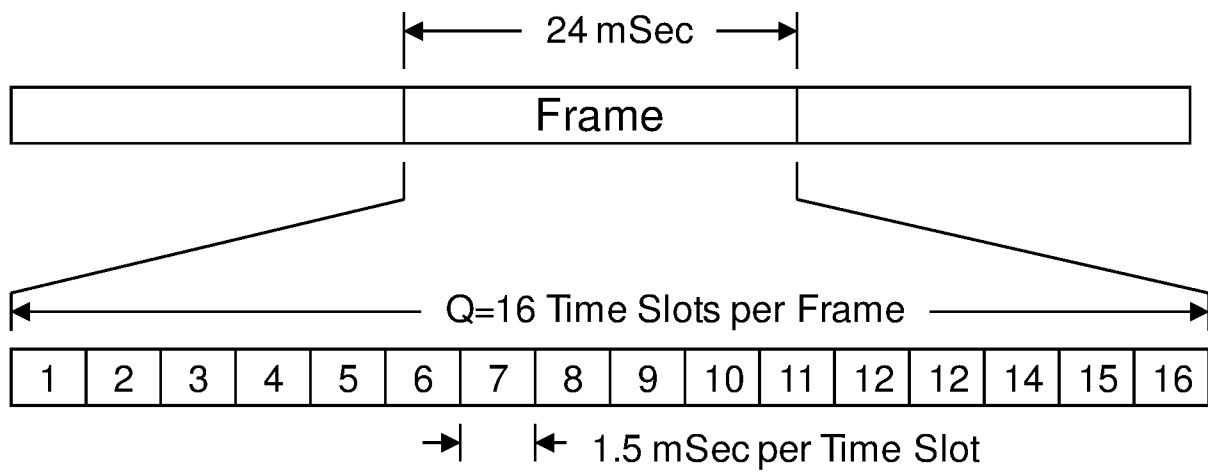
600


FIG. 6



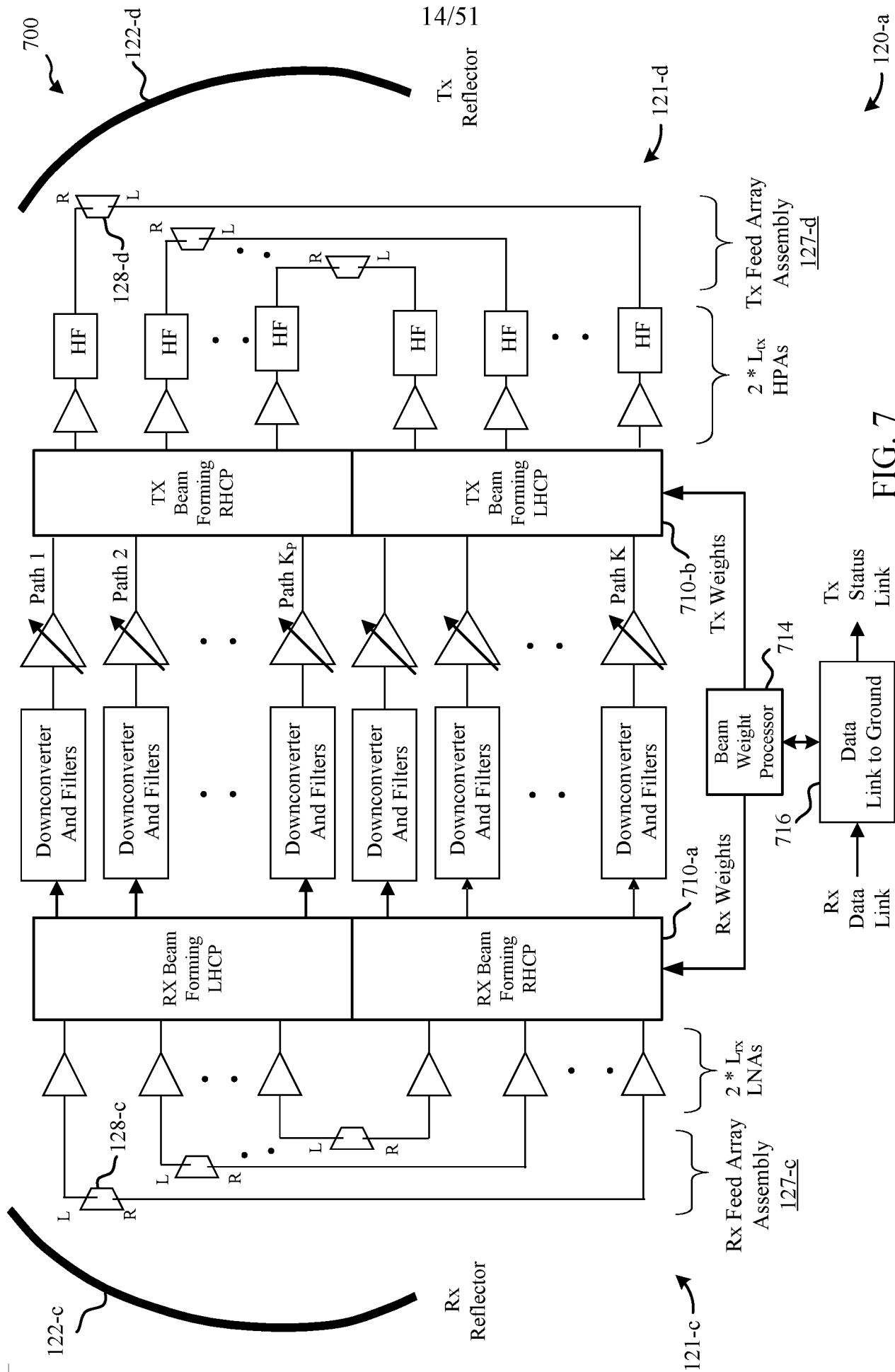


FIG. 7



800

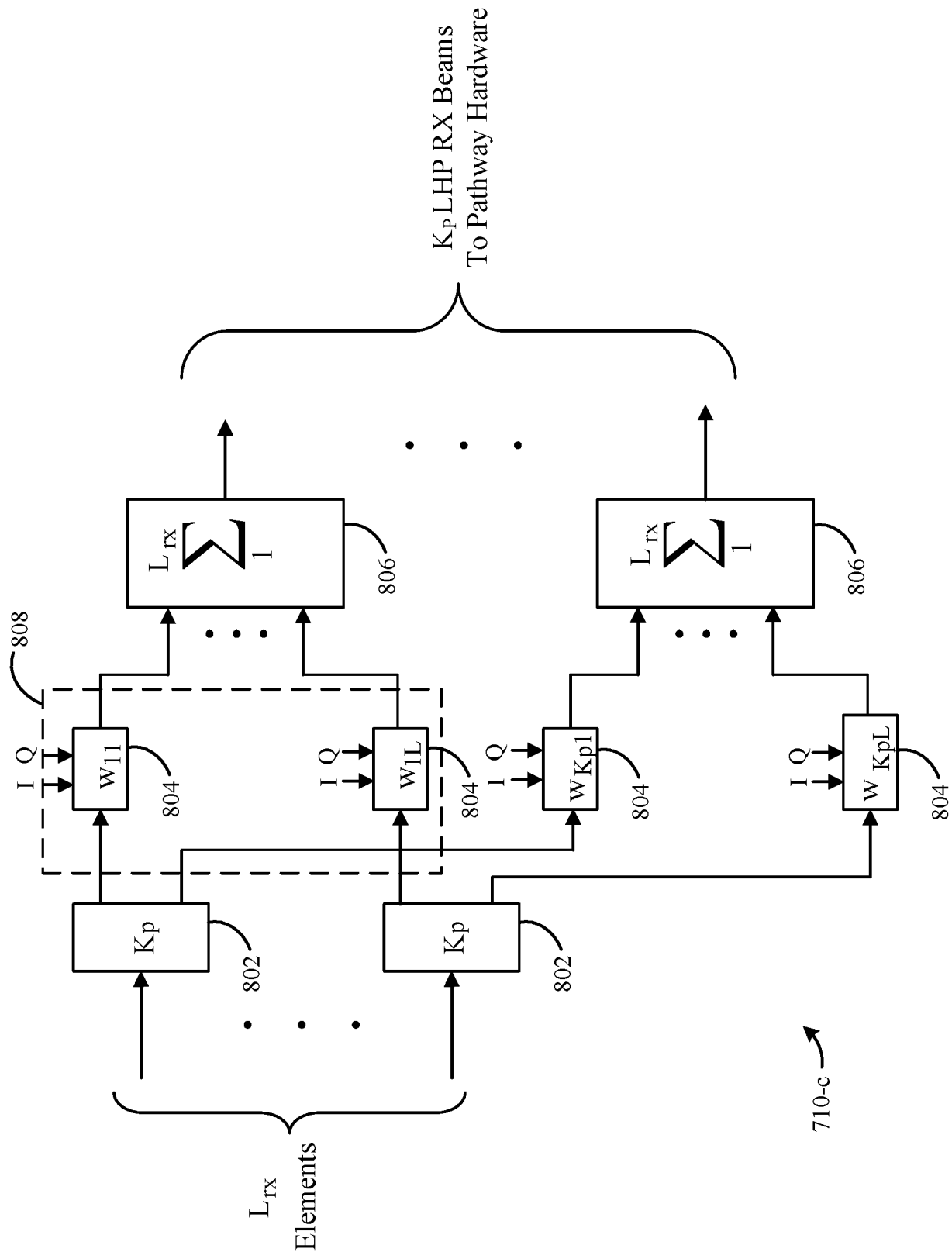


FIG. 8



900

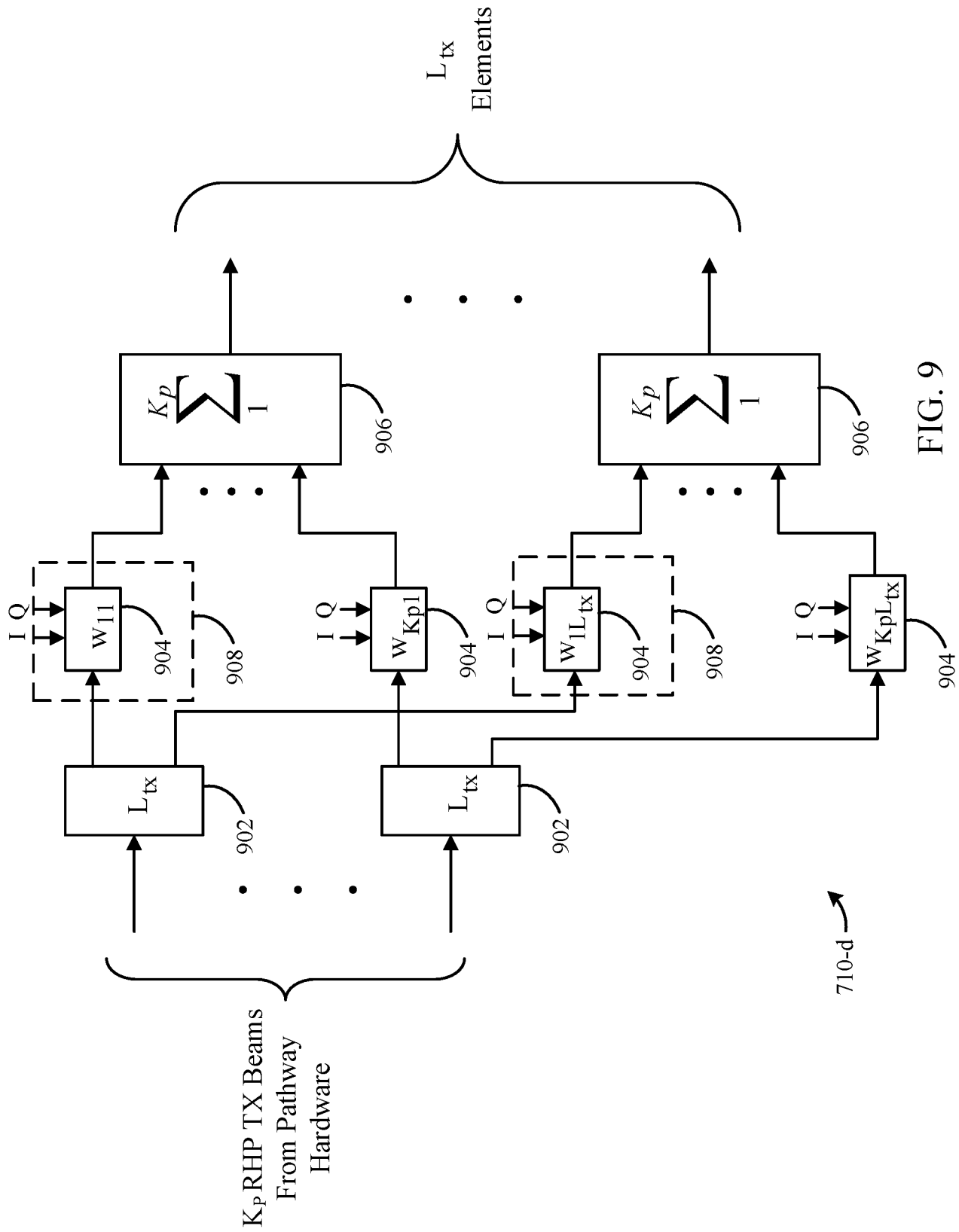


FIG. 9

710-d



1000

17/51

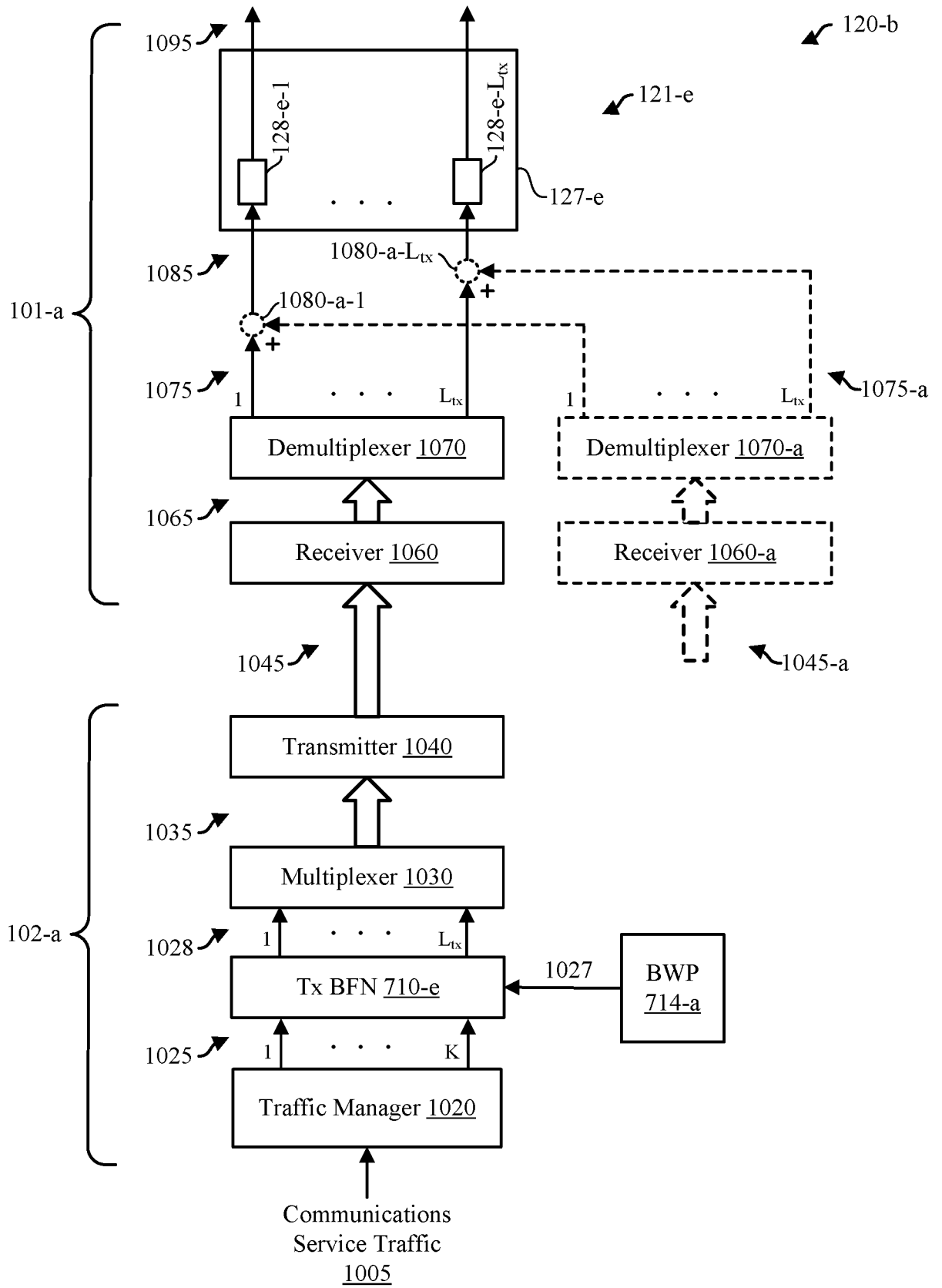


FIG. 10

1100

18/51

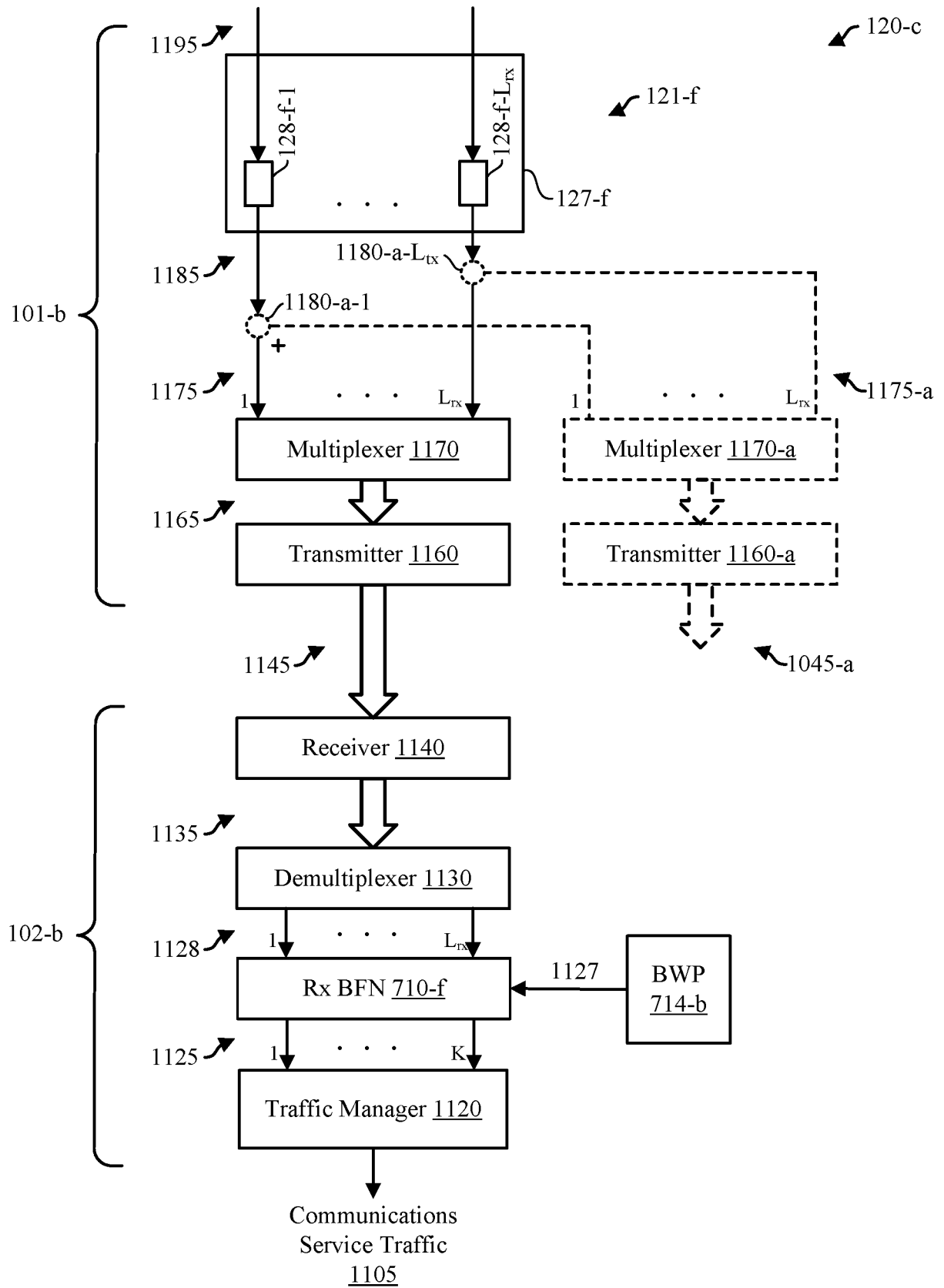


FIG. 11

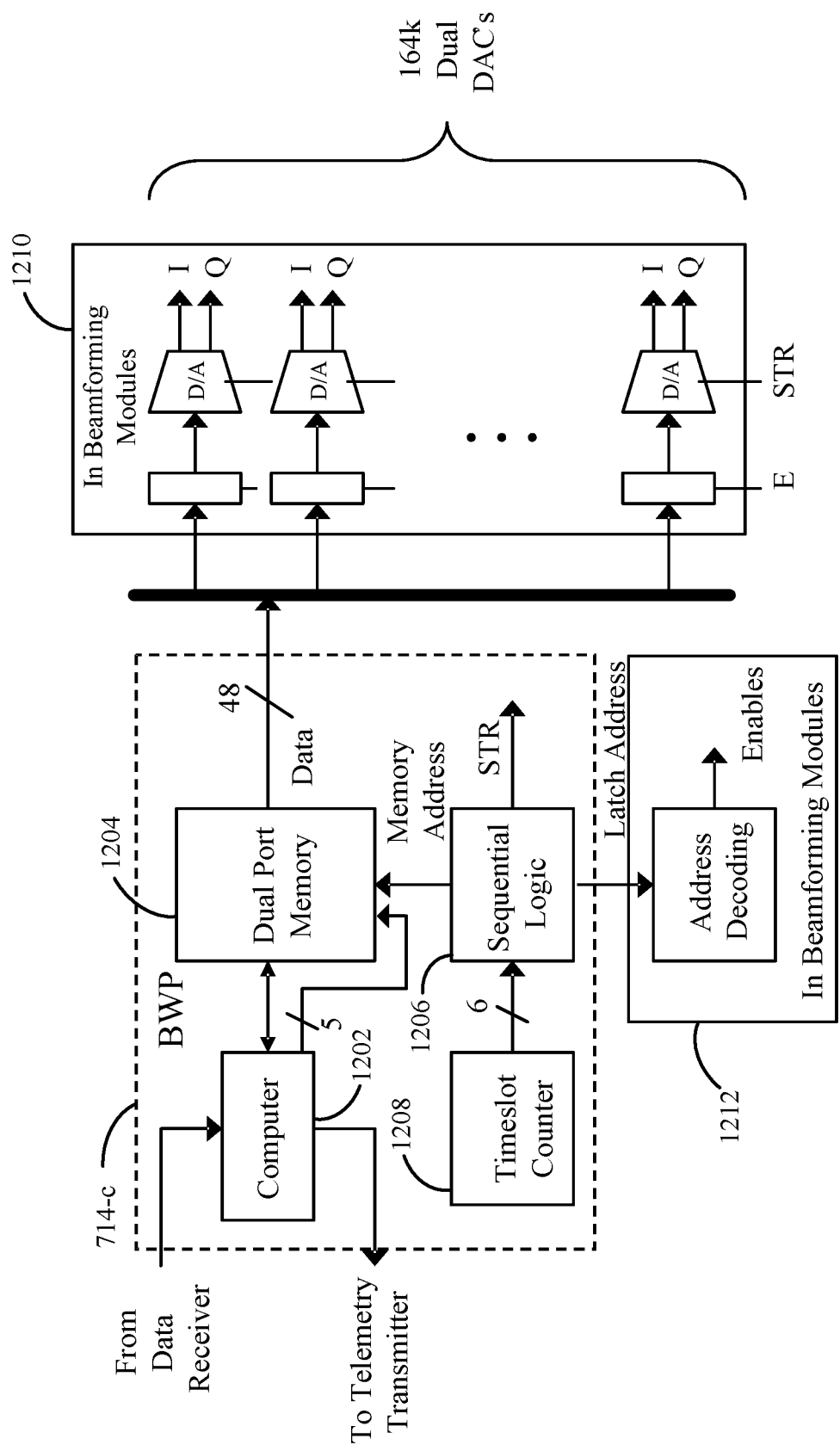


FIG. 12

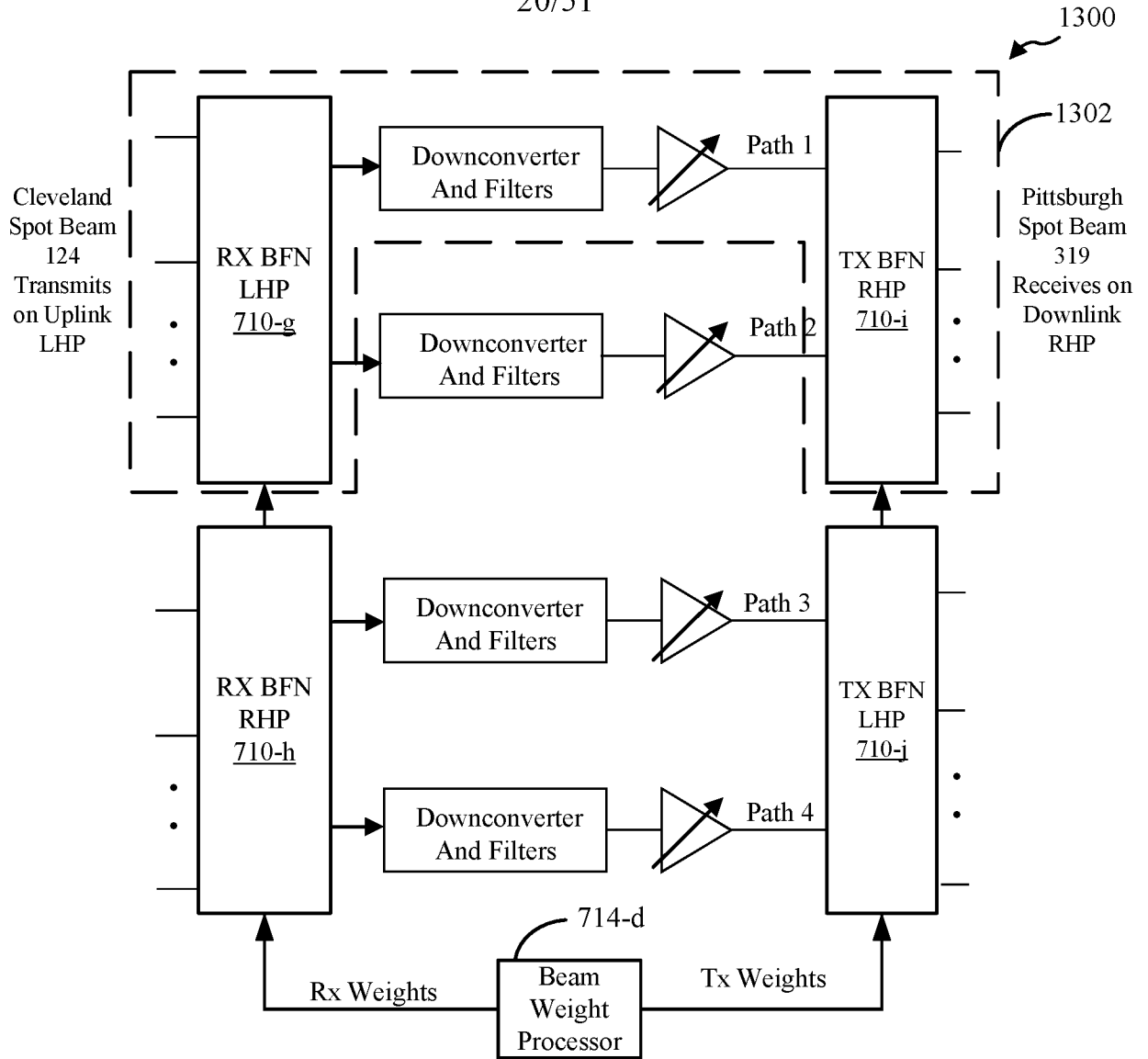


FIG. 13A

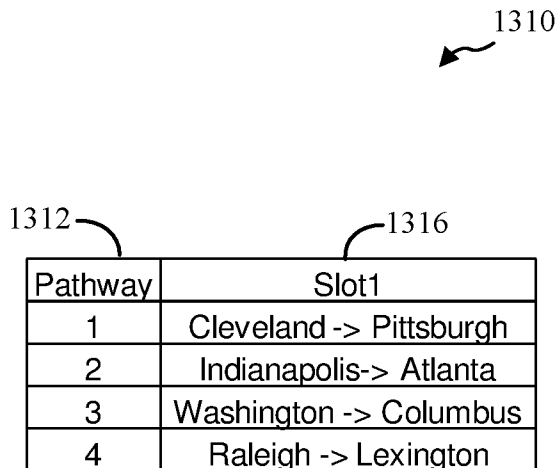


FIG. 13B

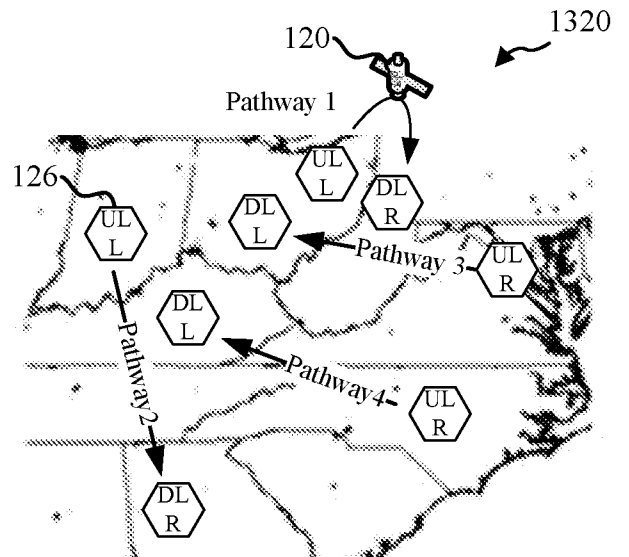
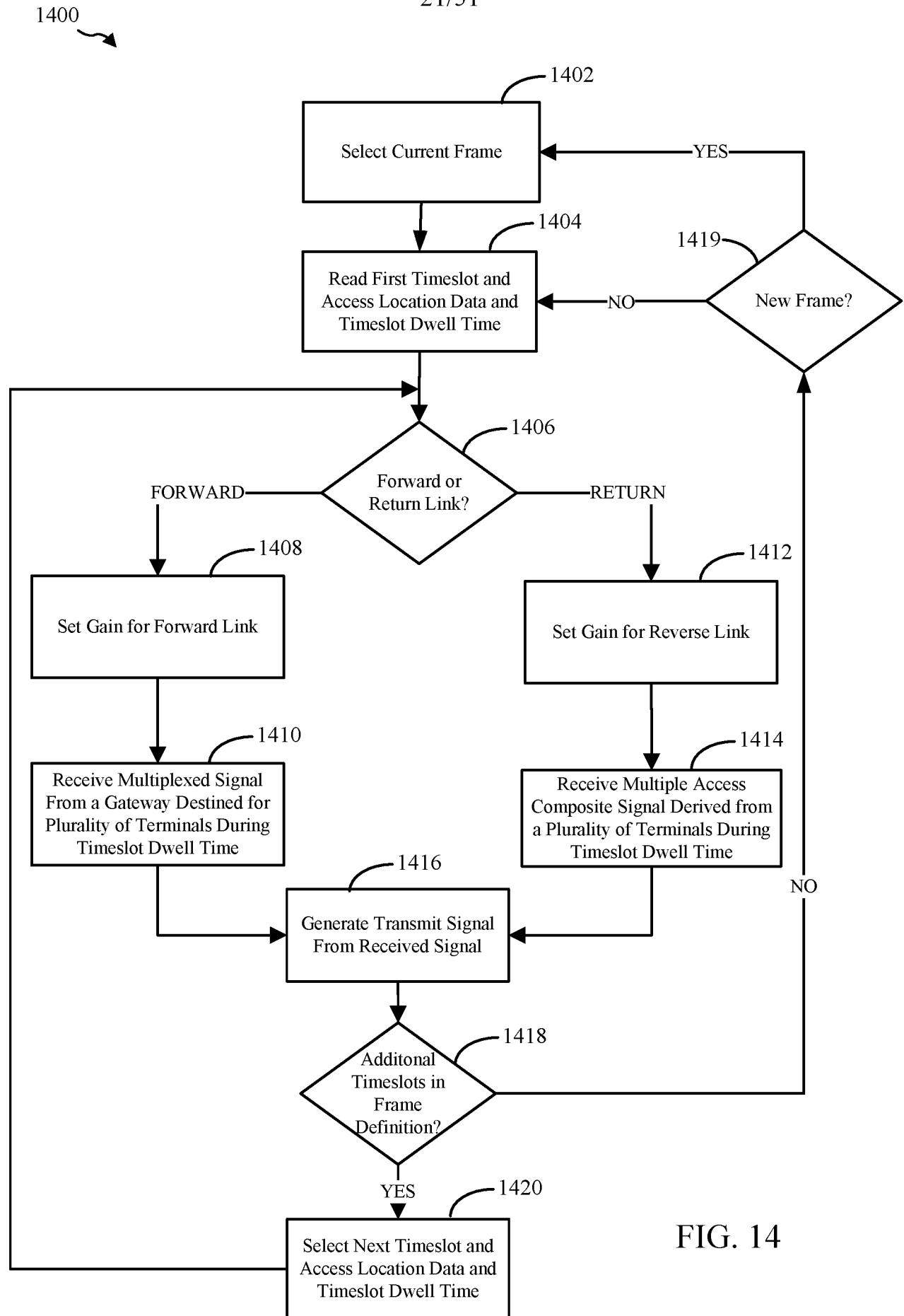


FIG. 13C





1500

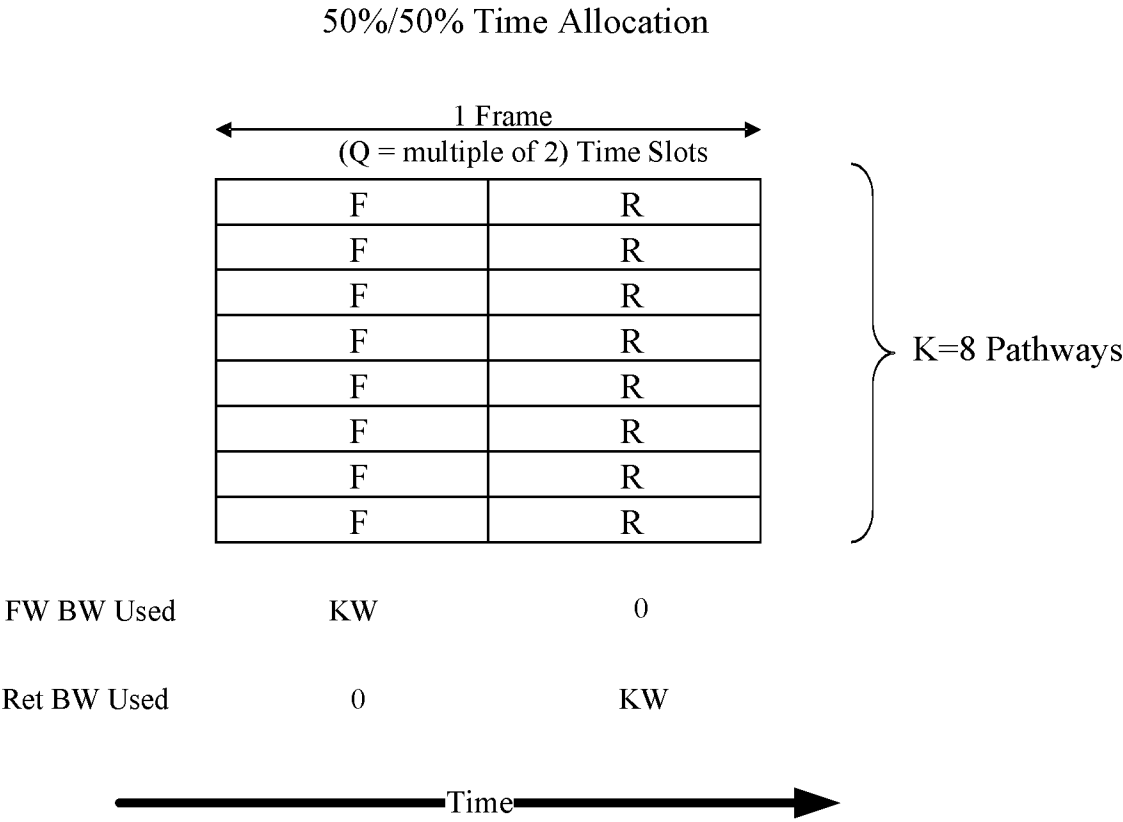


FIG. 15A



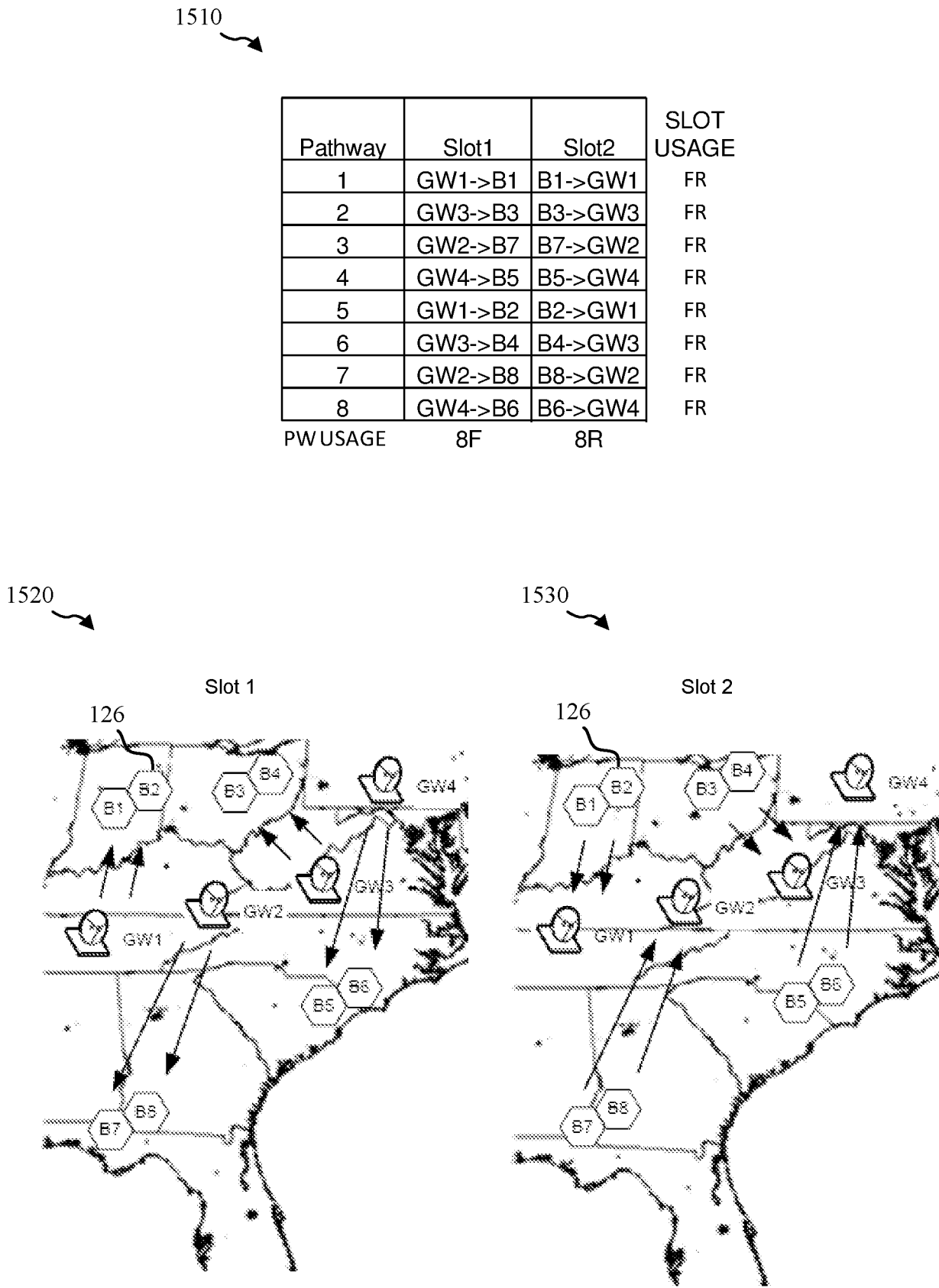


FIG. 15B



1600

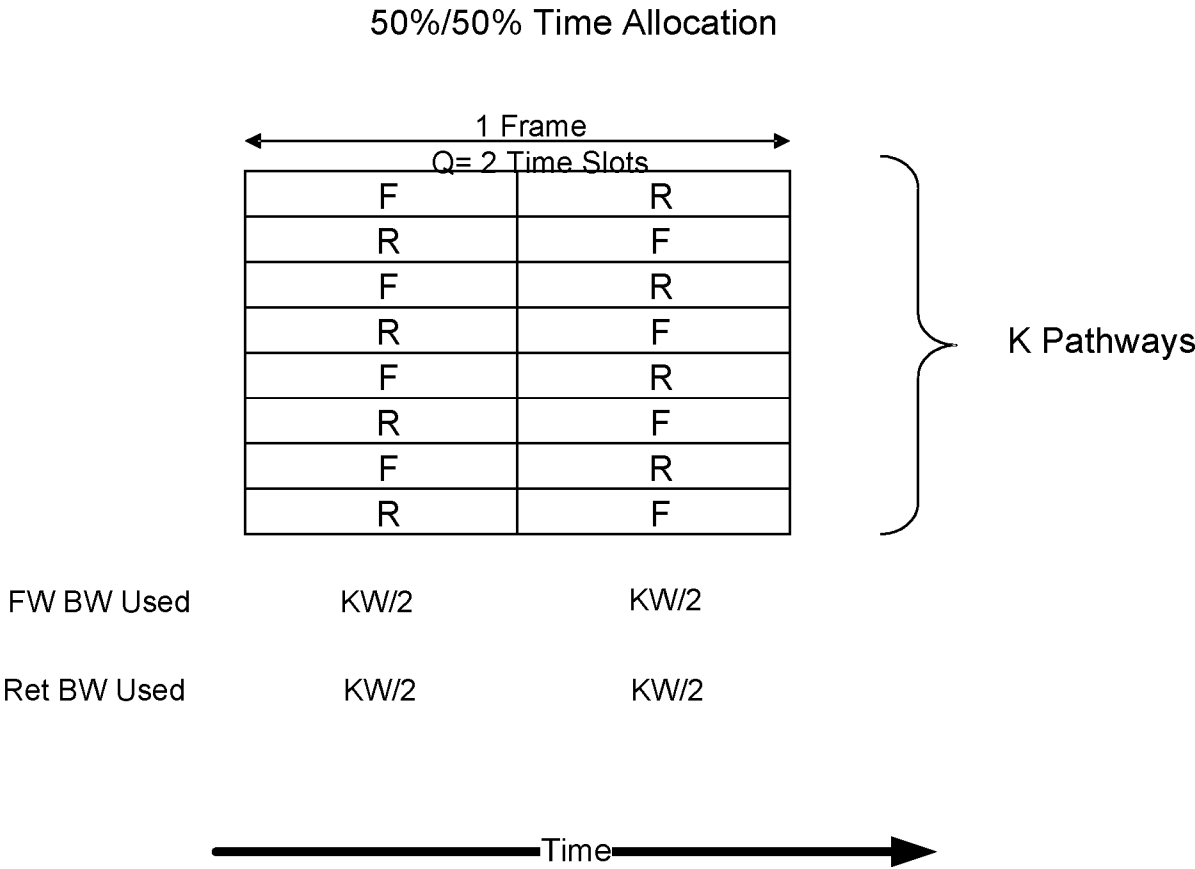


FIG. 16A





1610

Pathway	Slot1	Slot2	SLOT USAGE
1	GW1->B1	B1->GW1	FR
2	B7->GW1	GW1->B7	RF
3	GW2->B3	B3->GW2	FR
4	B5->GW2	GW2->B5	RF
5	GW1->B2	B2->GW1	FR
6	B8->GW1	GW1->B8	RF
7	GW2->B4	B4->GW2	FR
8	B6->GW2	GW2->B6	RF

PW USAGE 4F,4R 4F,4R

1620

1630

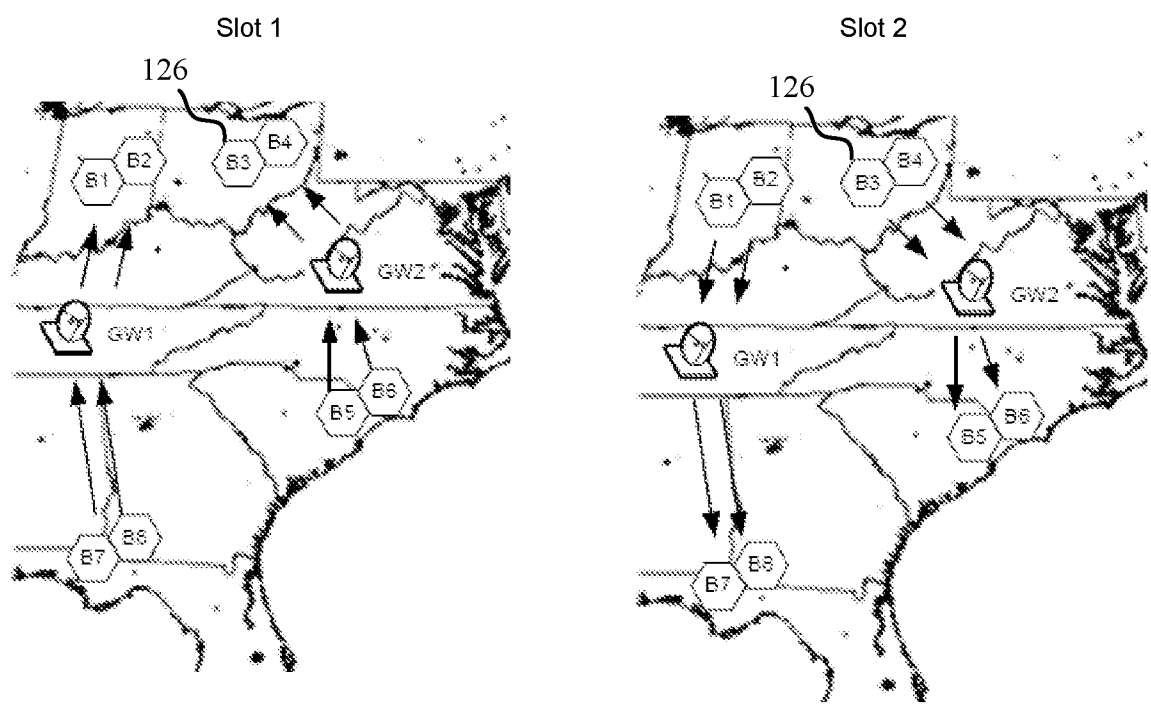


FIG. 16B





1700

75%/25% Time Allocation

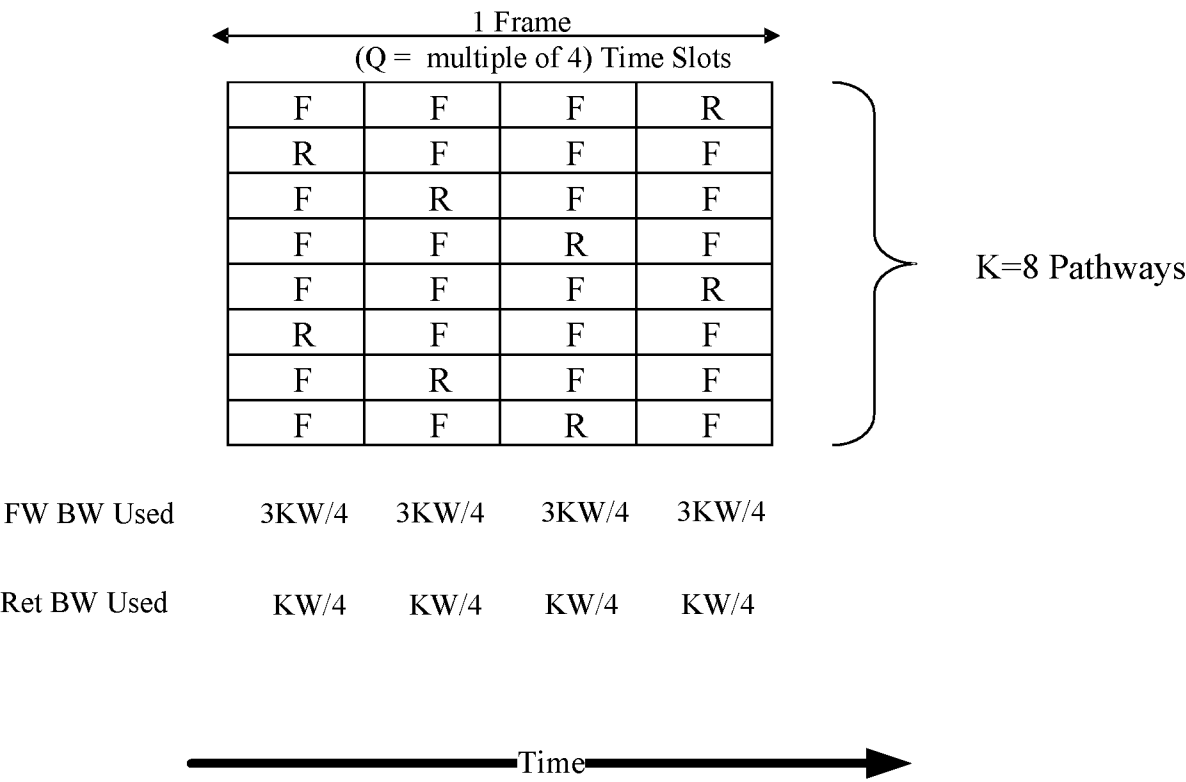


FIG. 17A



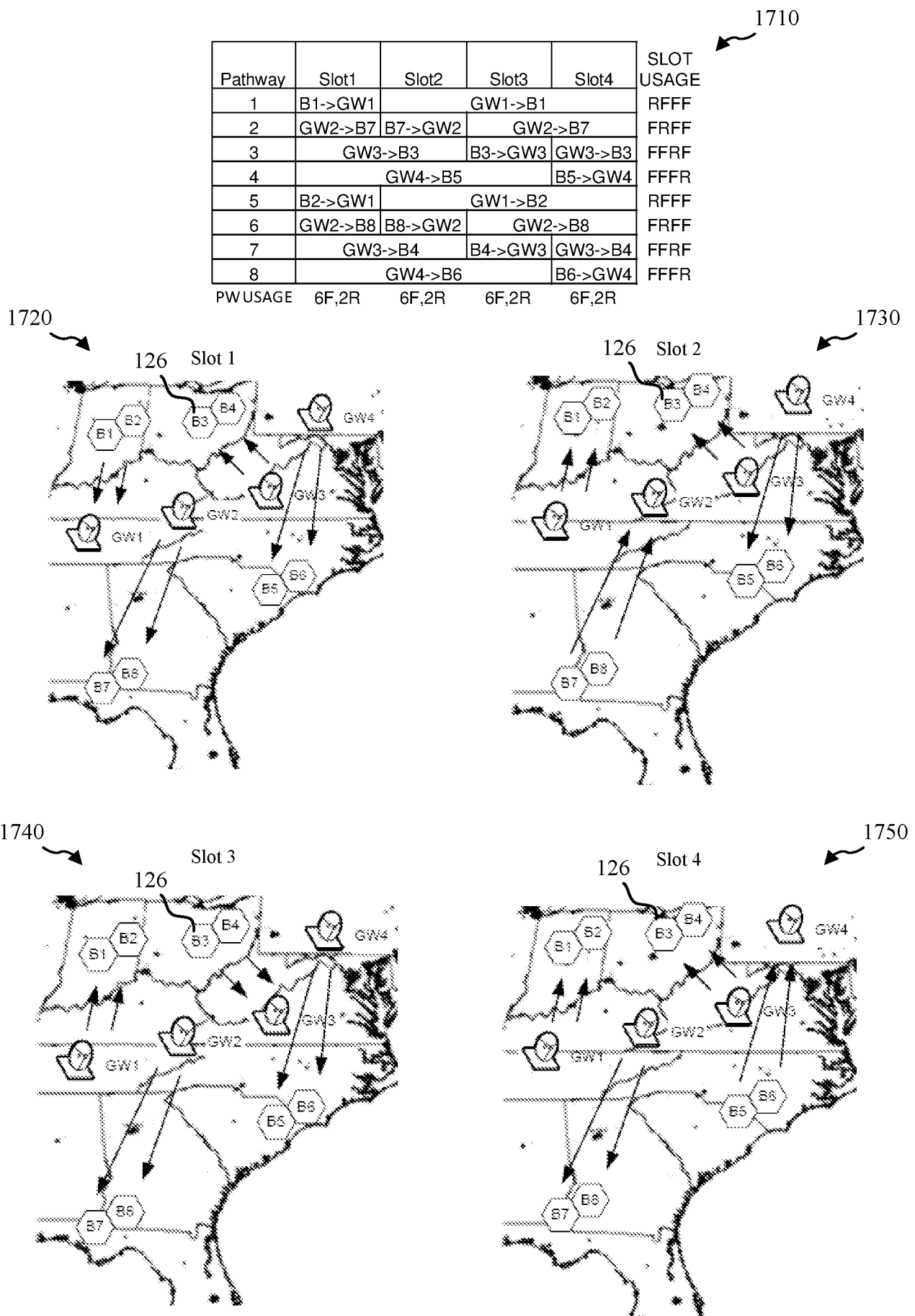


FIG. 17B

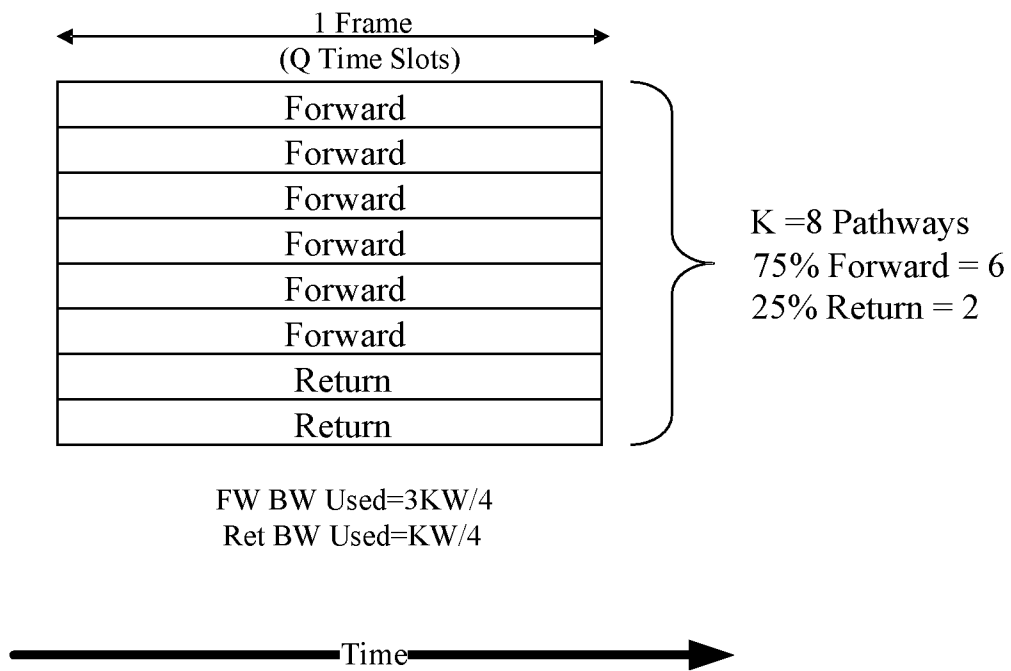
1800


FIG. 18A



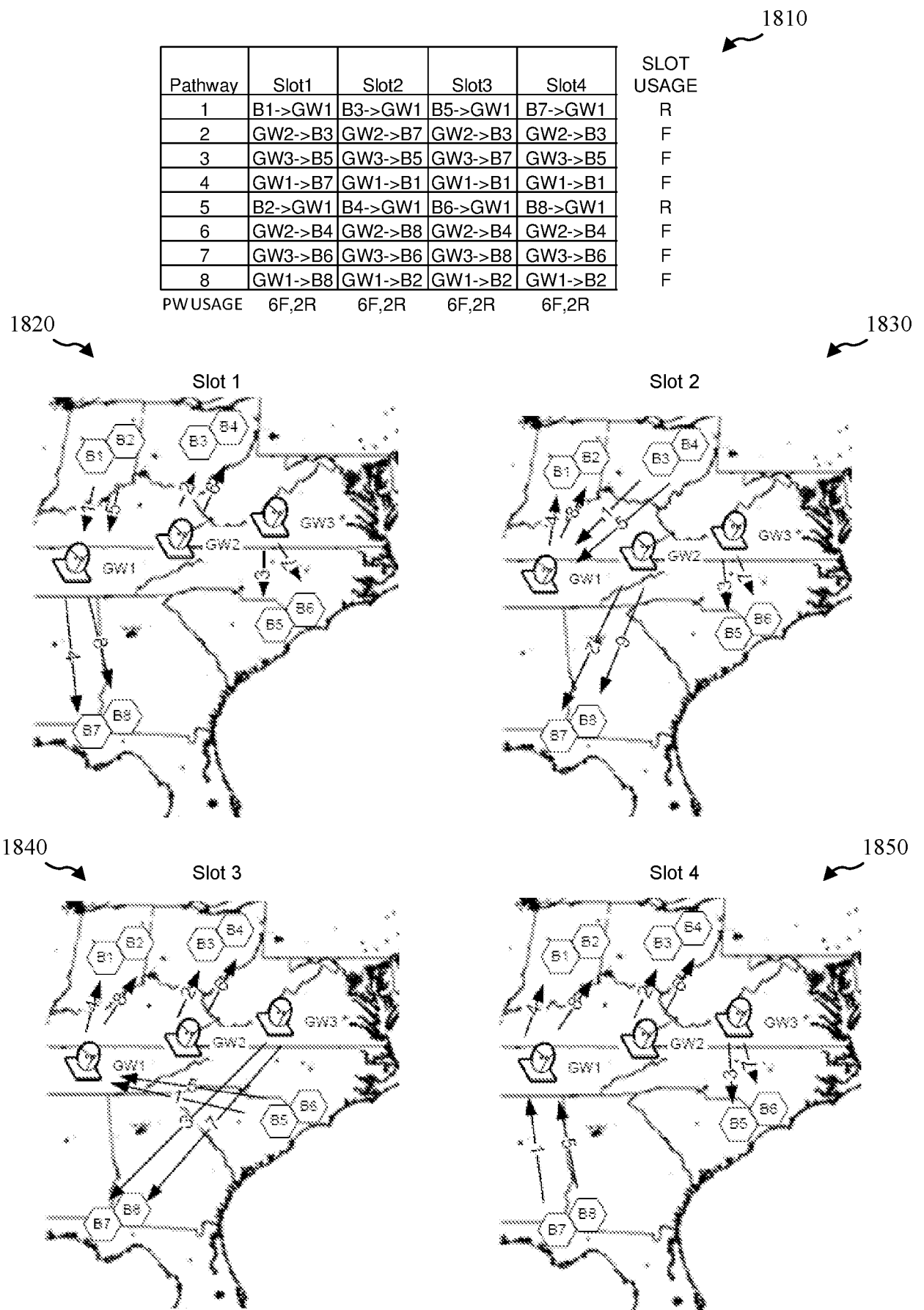


FIG. 18B

1860

1870

GW USAGE	Pathway	Slot1	Slot2	Slot3
SHARED	1	B1->GW1	B3->GW2	B5->GW3
GW2	2		GW2->B3	
GW3	3		GW3->B5	
GW1	4		GW1->B1	
SHARED	5	B2->GW1	B4->GW2	B6->GW3
GW2	6		GW2->B4	
GW3	7		GW3->B6	
GW1	8		GW1->B2	
PW USAGE	6F,2R	6F,2R	6F,2R	

FIG. 18C

GW USAGE	Pathway	Slot1	Slot2	Slot3	SLOT USAGE
R	1	B1->GW1	B3->GW1	B5->GW1	R
F	2		GW2->B3		F
F	3		GW3->B5		F
F	4		GW1->B1		F
R	5	B2->GW1	B4->GW1	B6->GW1	R
F	6		GW2->B4		F
F	7		GW3->B6		F
F	8		GW1->B2		F
PW USAGE	6F,2R	6F,2R	6F,2R		

FIG. 18D

1880

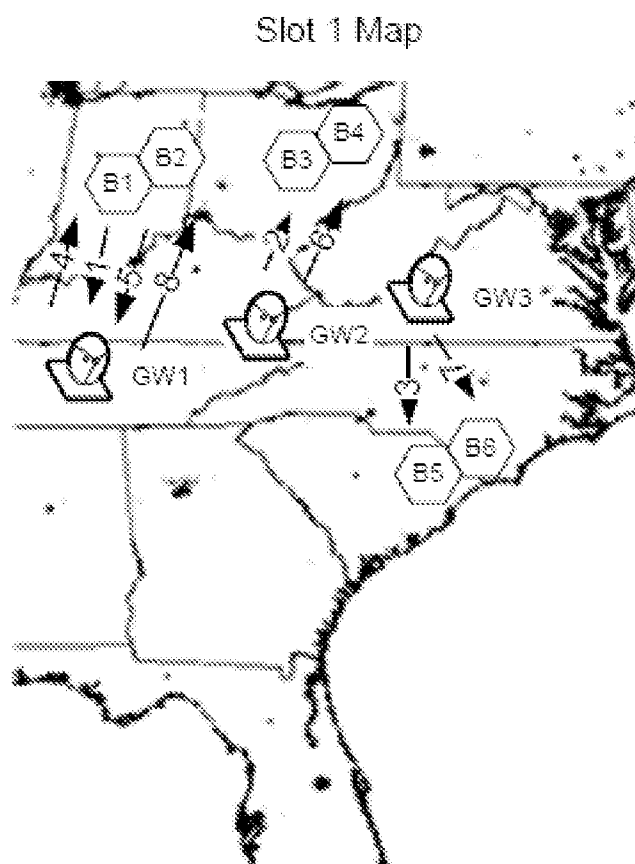


FIG. 18E

1900

100 total pathways

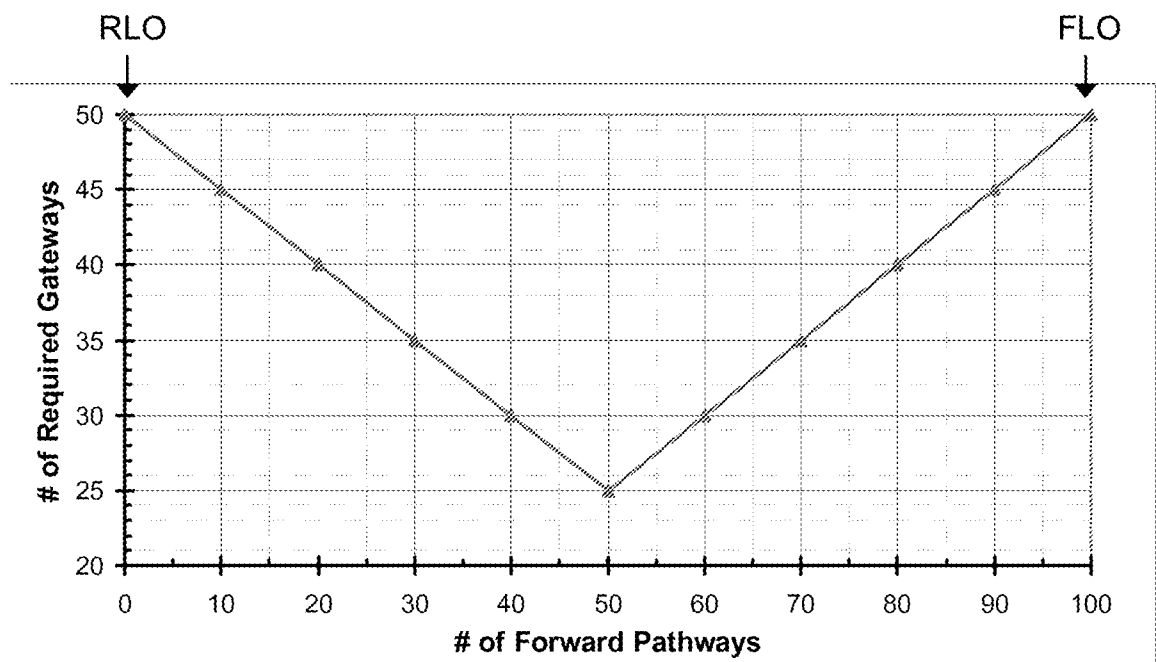


FIG. 19

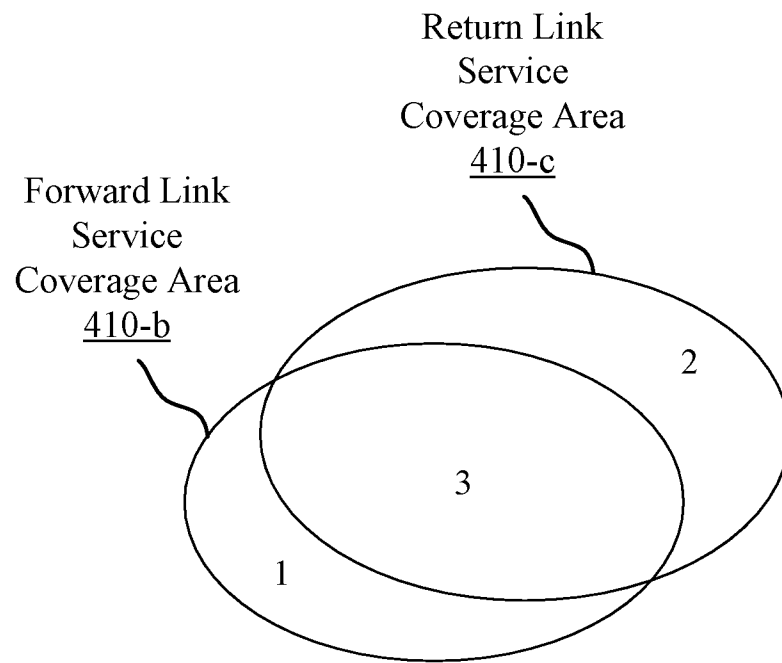
2000
↘

FIG. 20A

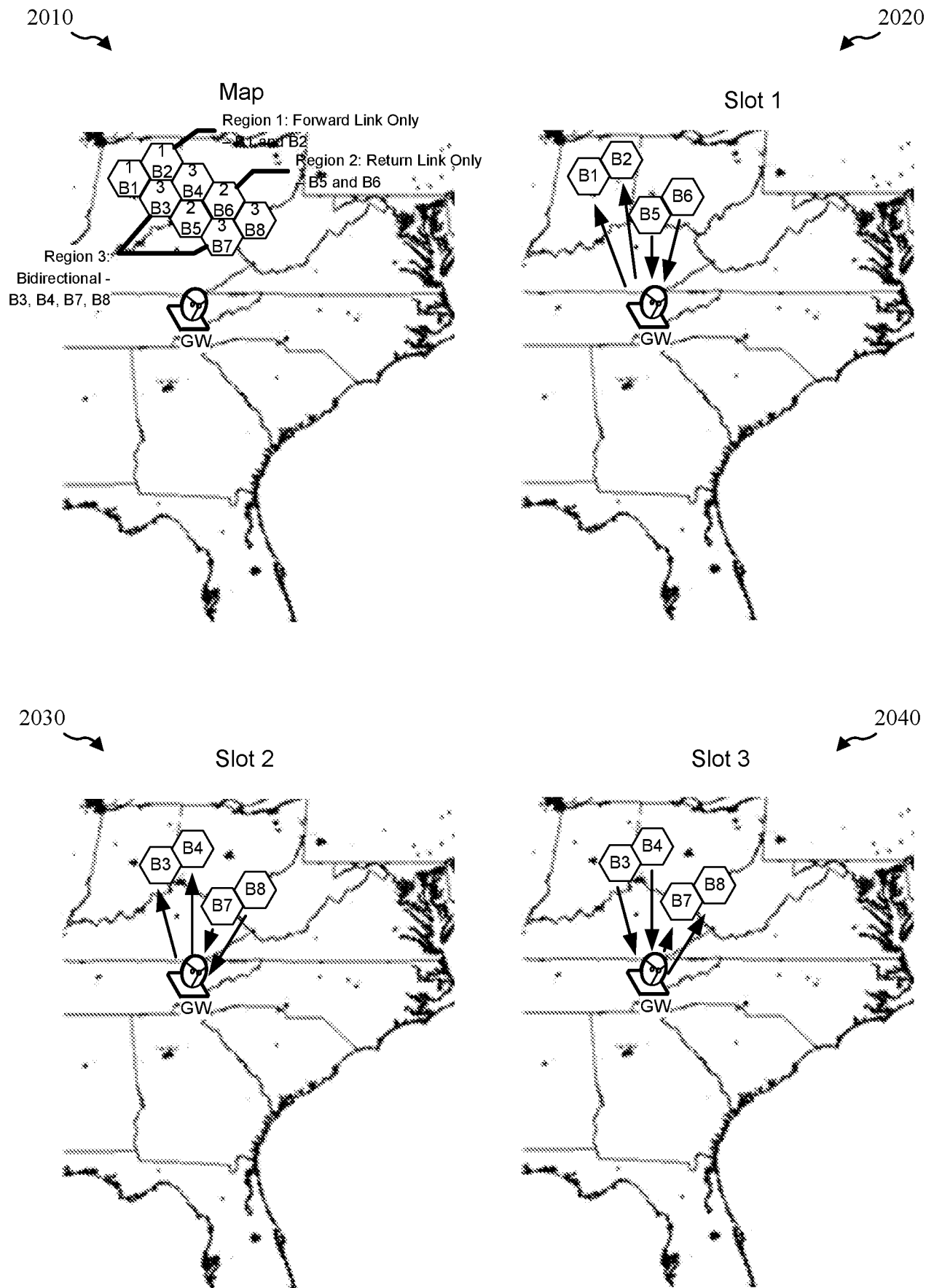


FIG. 20B

***Example with 8 dwell times,
Q=32 and $C_b=4.5$ Gbps***

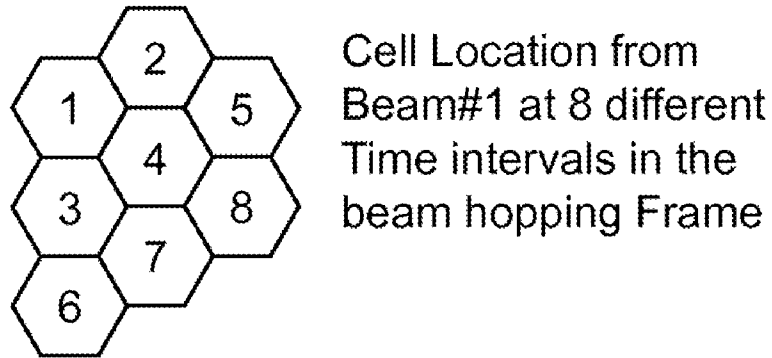


FIG. 21A

Dwell Time #	qj, # slots Assigned	Area Capacity, Mbps
1	16	2250
2	1	141
3	2	281
4	3	422
5	2	281
6	5	703
7	1	141
8	2	281
Total	32	4500

FIG. 21B

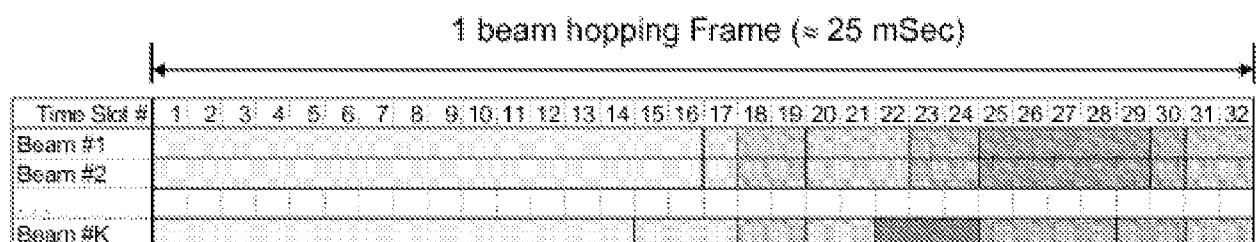
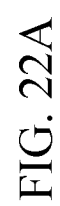


FIG. 21C



GW#	Location	# Beam Issues	Ci
1	Sanderson, TX	0	8
2	Ft. Hancock, TX	2	6
3	Amarillo, TX	0	8
4	Milford, UT	0	8
5	Ellis, KN	0	8
6	Lovelock, NV	1	7
7	Green River, WY	0	8
8	Boise, ID	2	6
9	Rapid City, SD	1	7
10	Bozeman, MT	2	6
11	Winnipeg, Canada	0	8
12	Duluth, MI	0	8
13	Syracuse, NY	2	6
14	Little Rock, AK	0	8
15	St. Louis, MO	1	7
16	Louisville, KY	1	7
17	Kansas City, MO	1	7
18	Las Vegas, NV	3	5
19	Montreal	0	8
20	Eugene, OR	0	8
21	Jacksonville, FL	0	8
22	Savannah, GE	0	8
23	Des Moines, IO	0	8
	Total		168

FIG. 22B

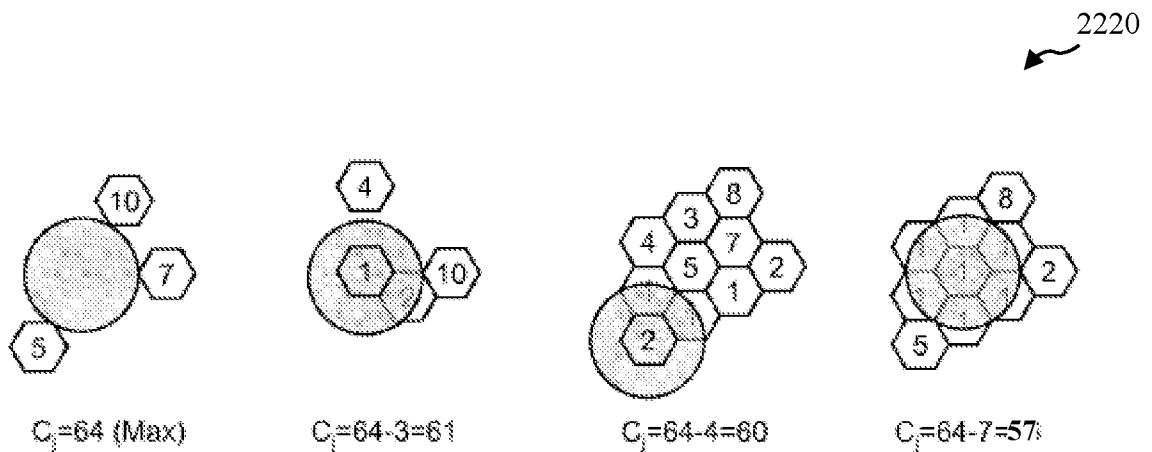


FIG. 22C

2300

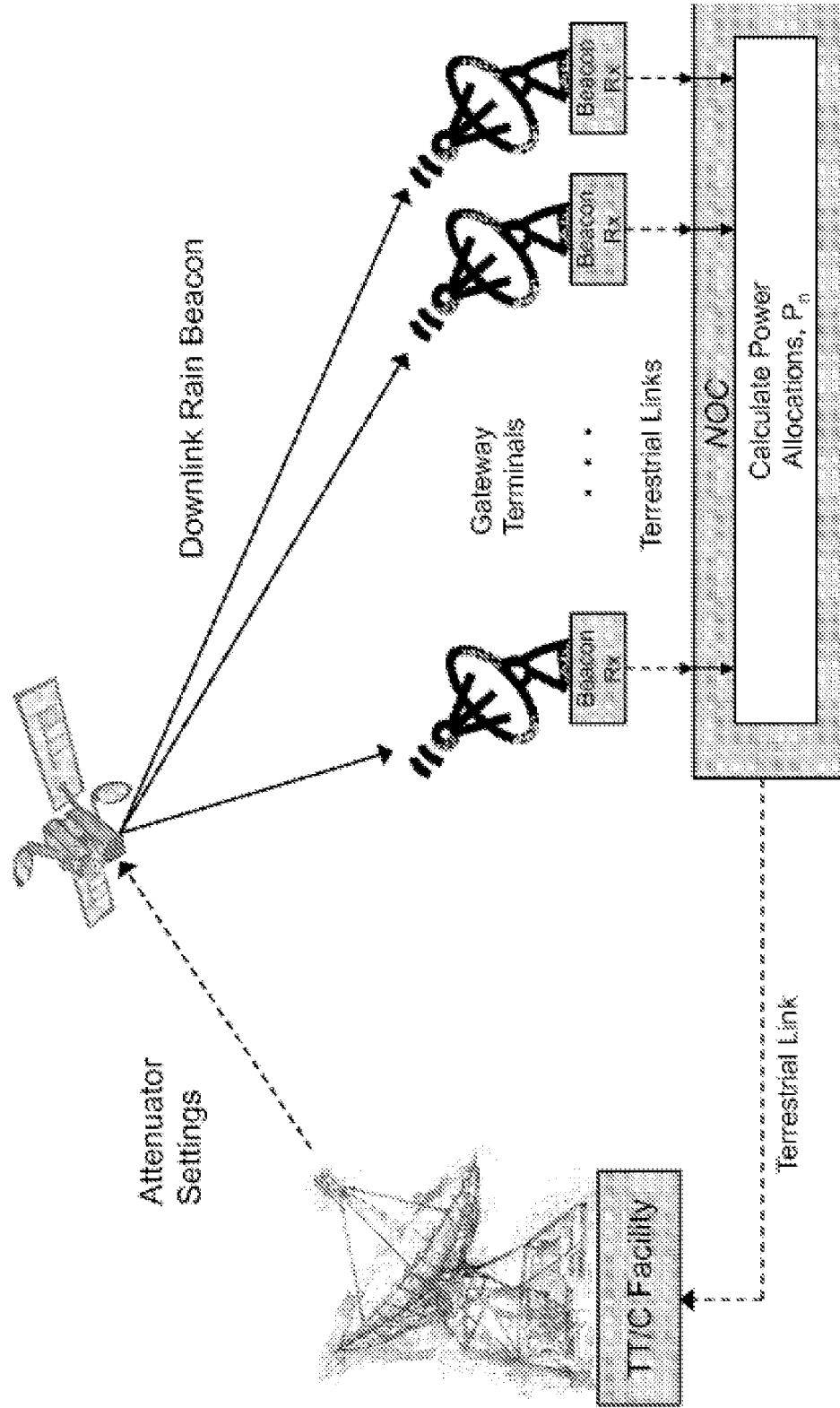


FIG. 23

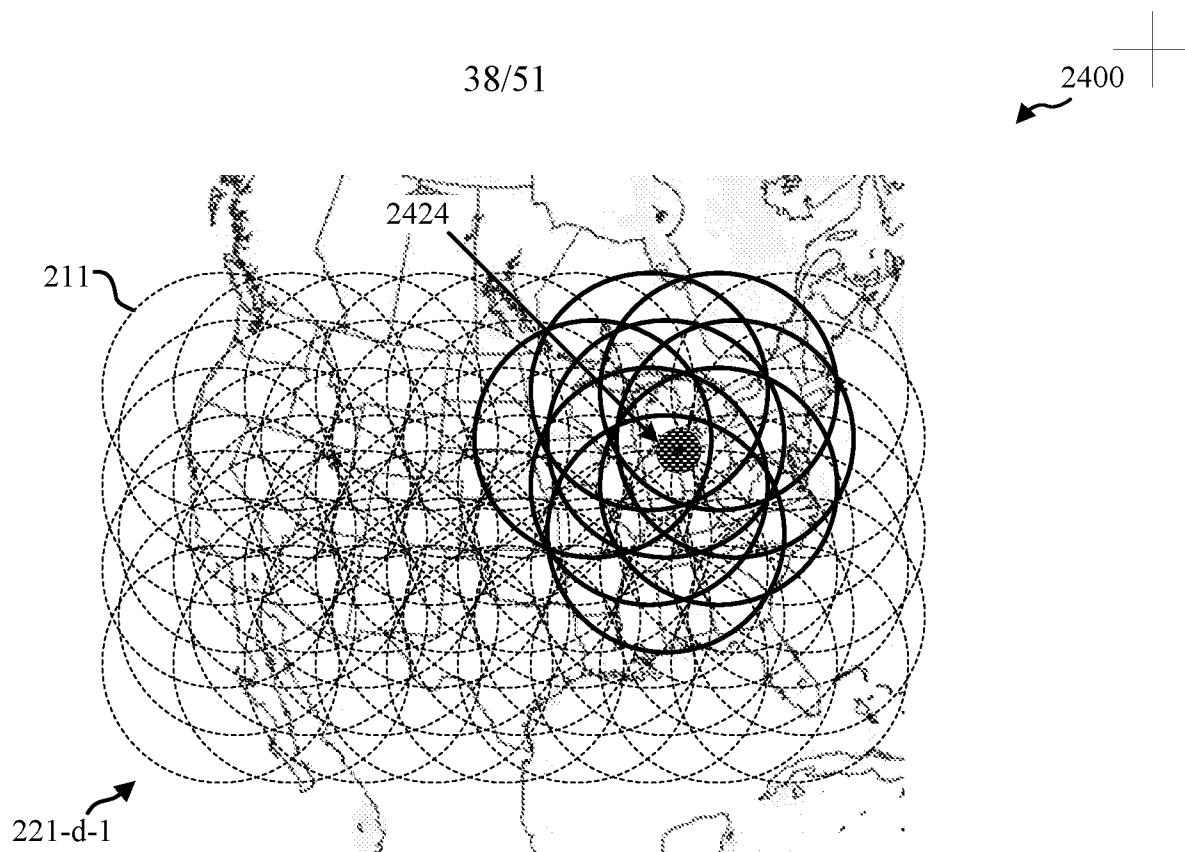


FIG. 24A

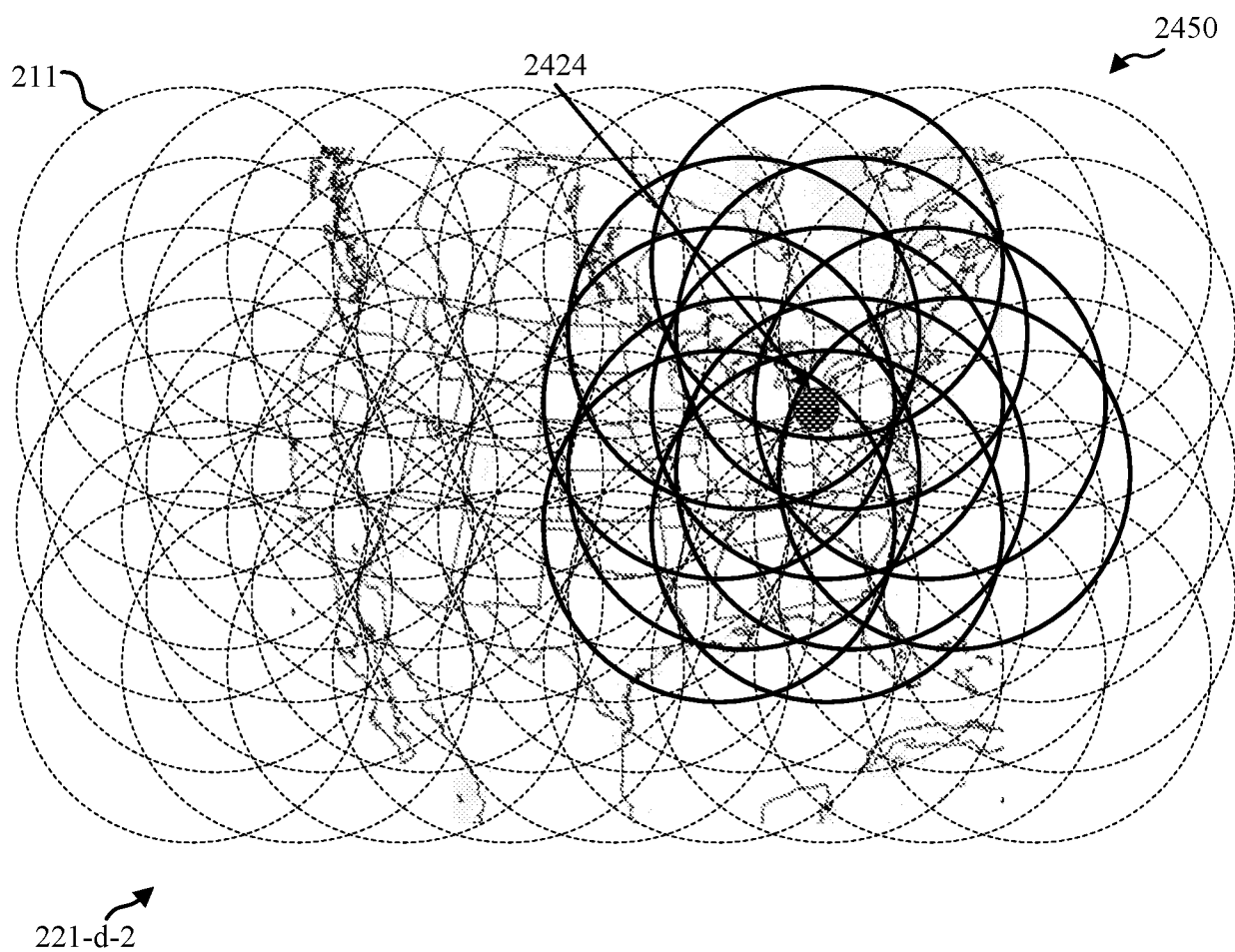


FIG. 24B

121-j

2470

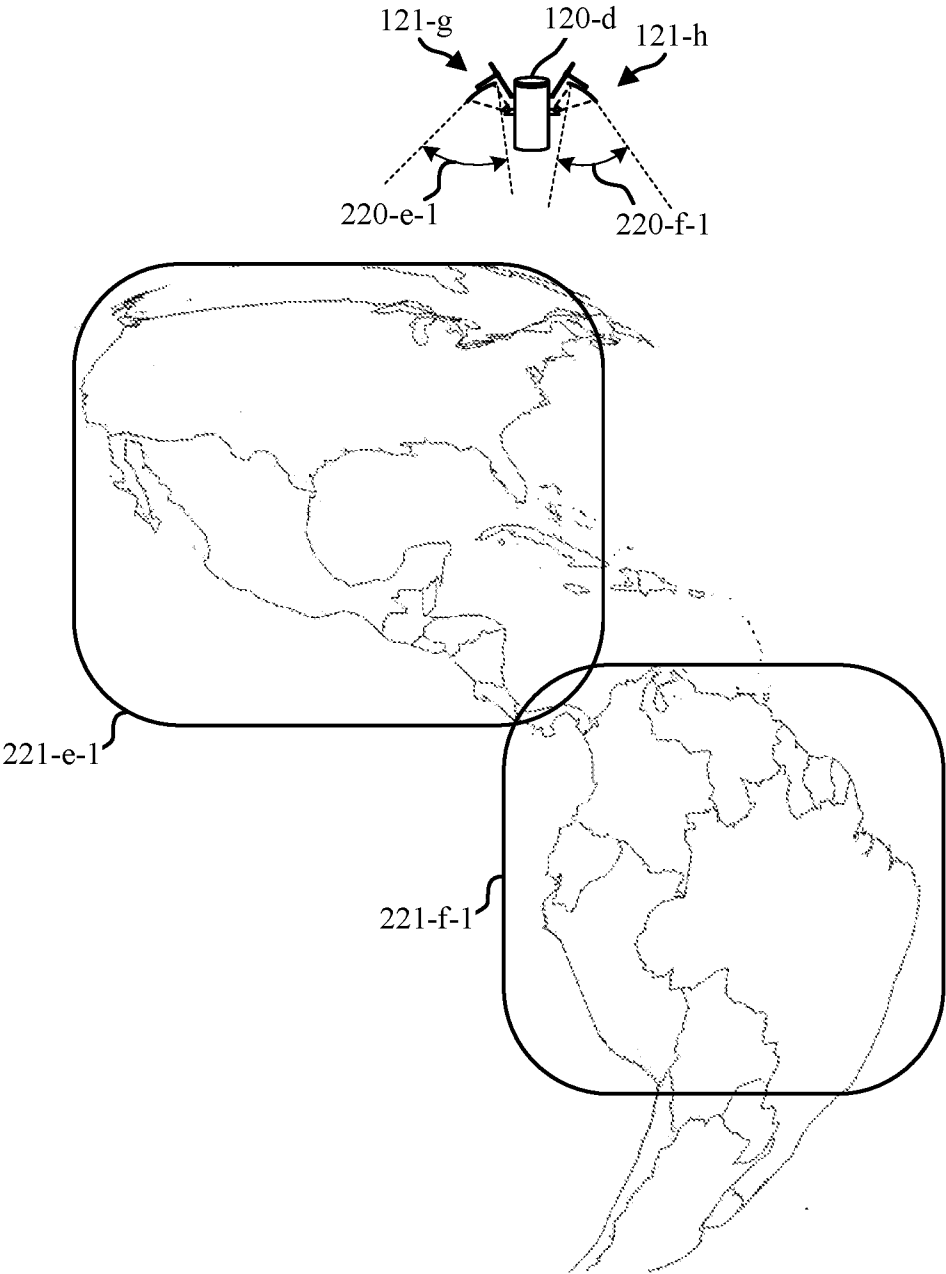


FIG. 24C

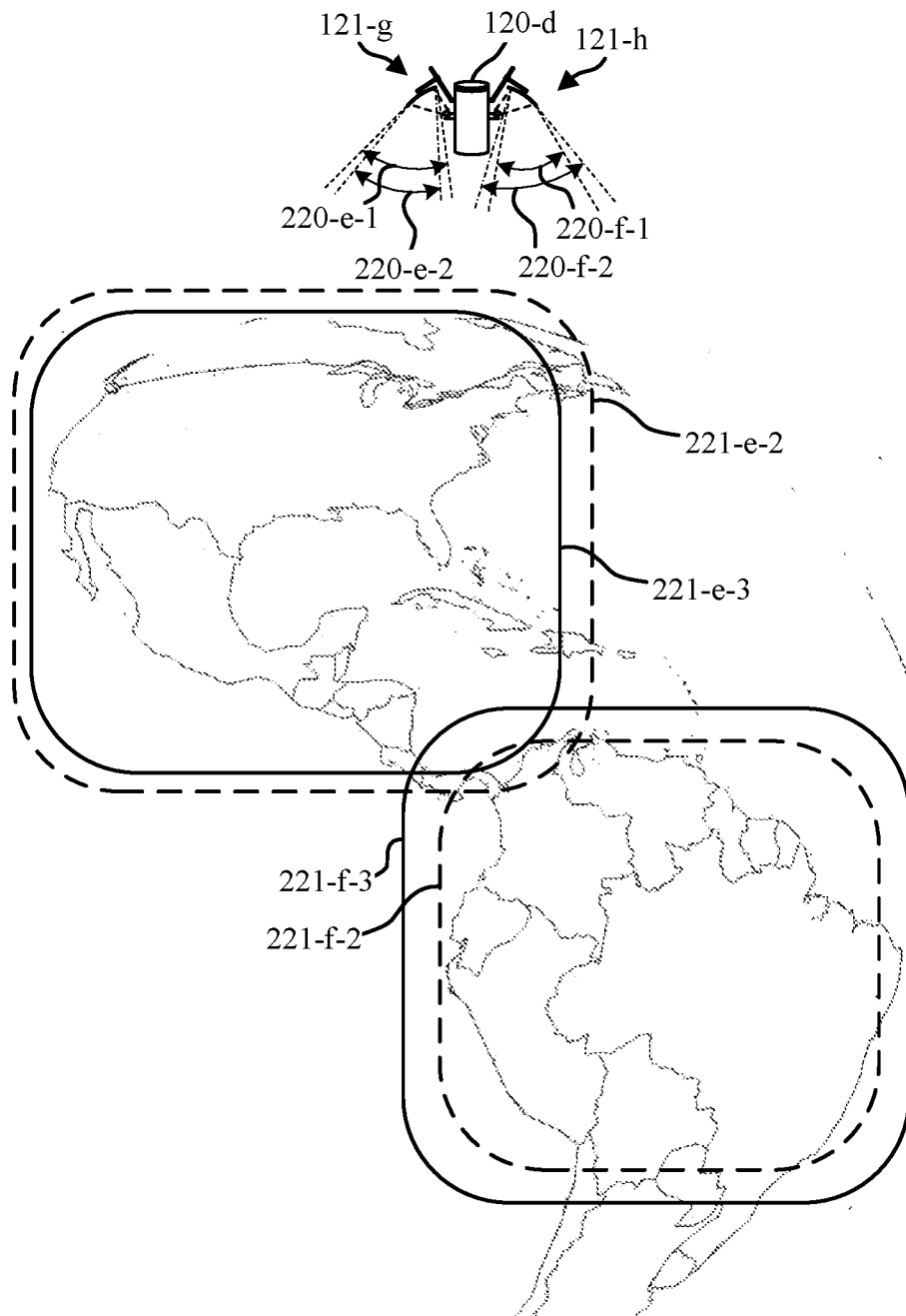


FIG. 24D

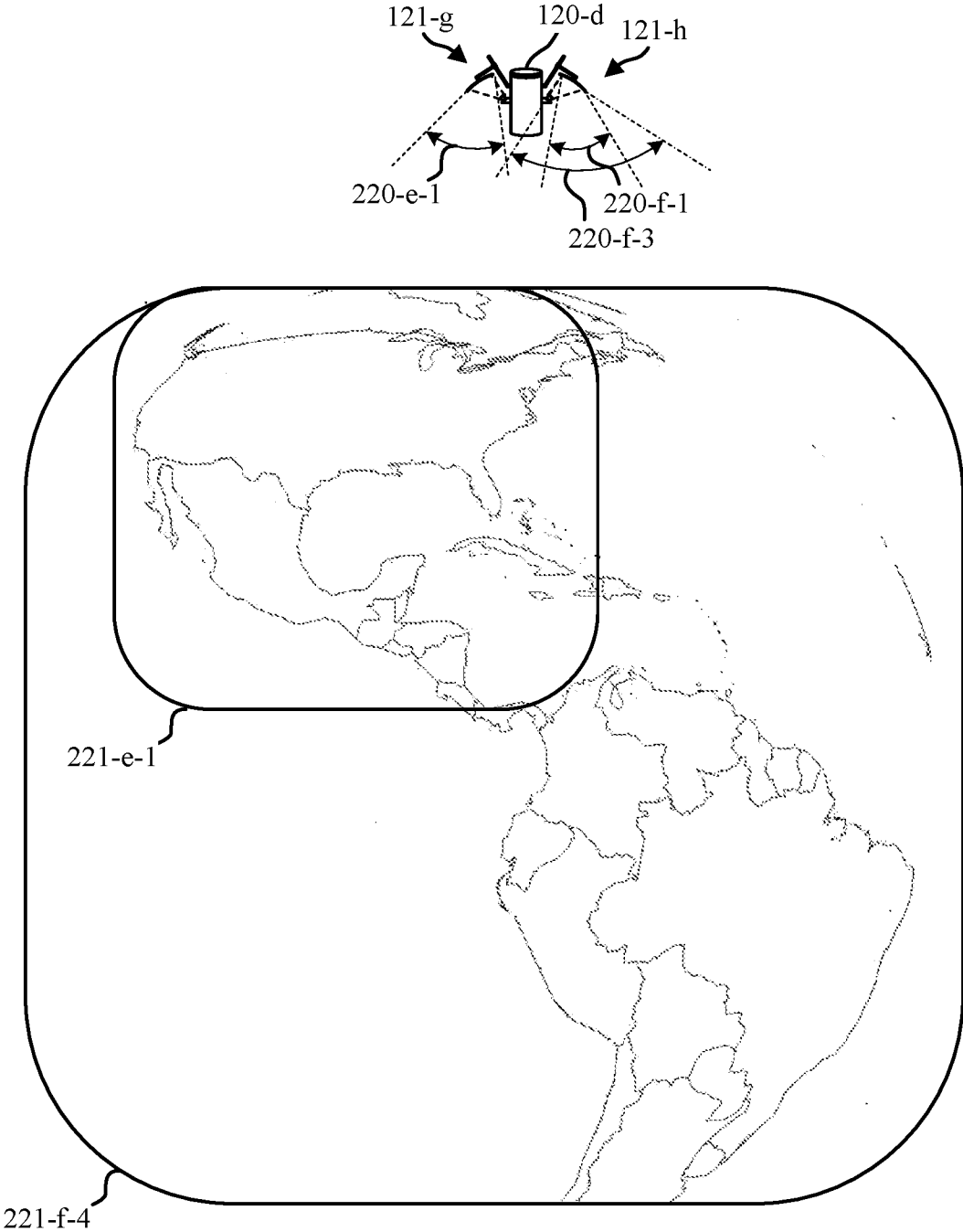
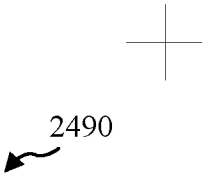


FIG. 24E

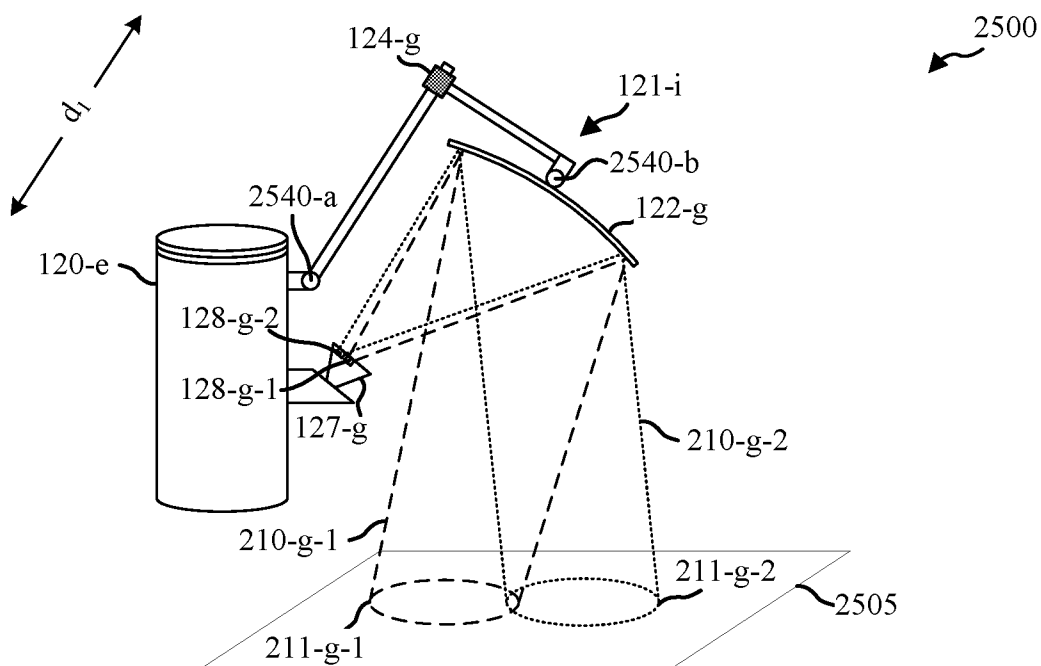


FIG. 25A

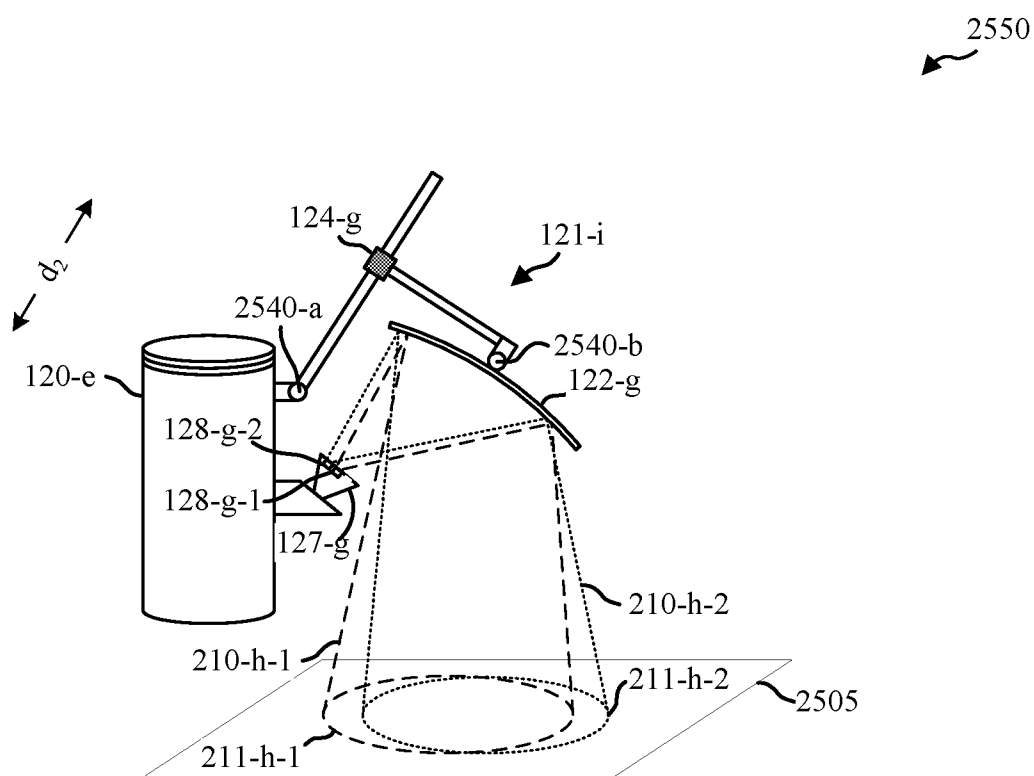


FIG. 25B

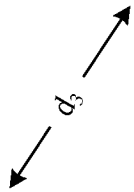
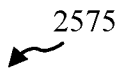


FIG. 25C



A blank coordinate plane with a horizontal x-axis and a vertical y-axis intersecting at the origin. The axes are represented by thin black lines.

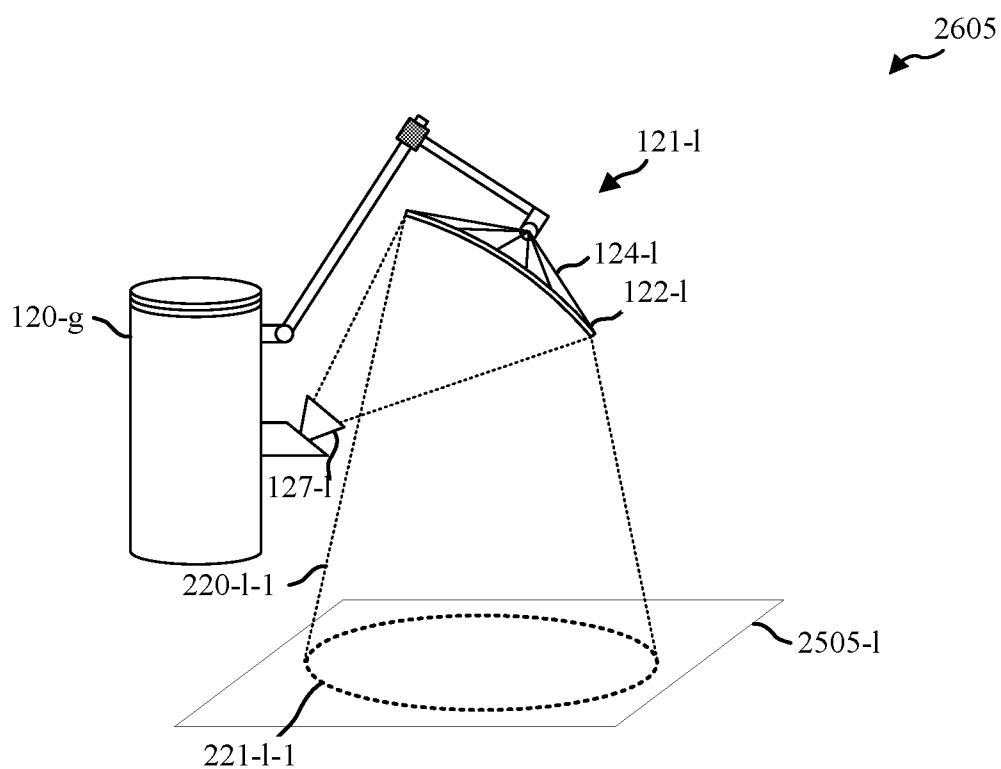


FIG. 26A

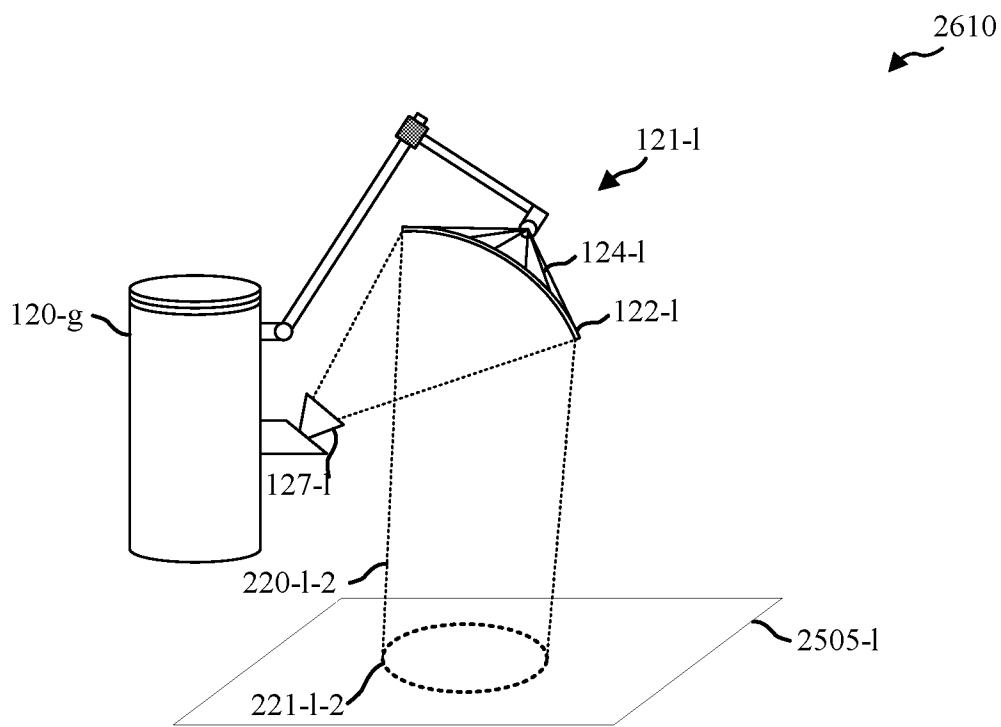


FIG. 26B

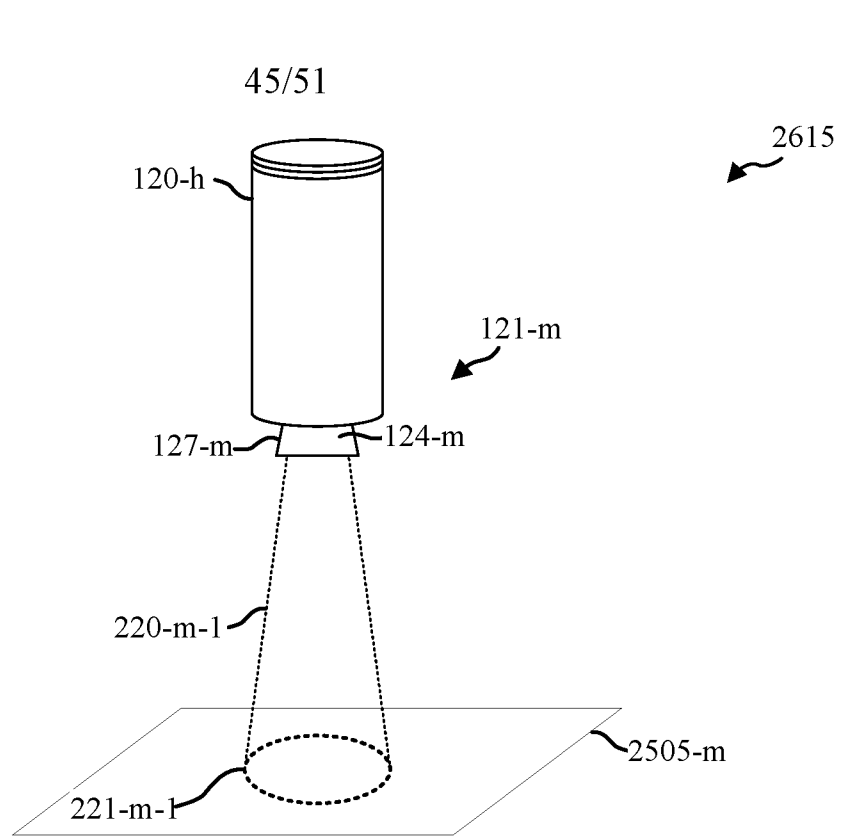


FIG. 26C

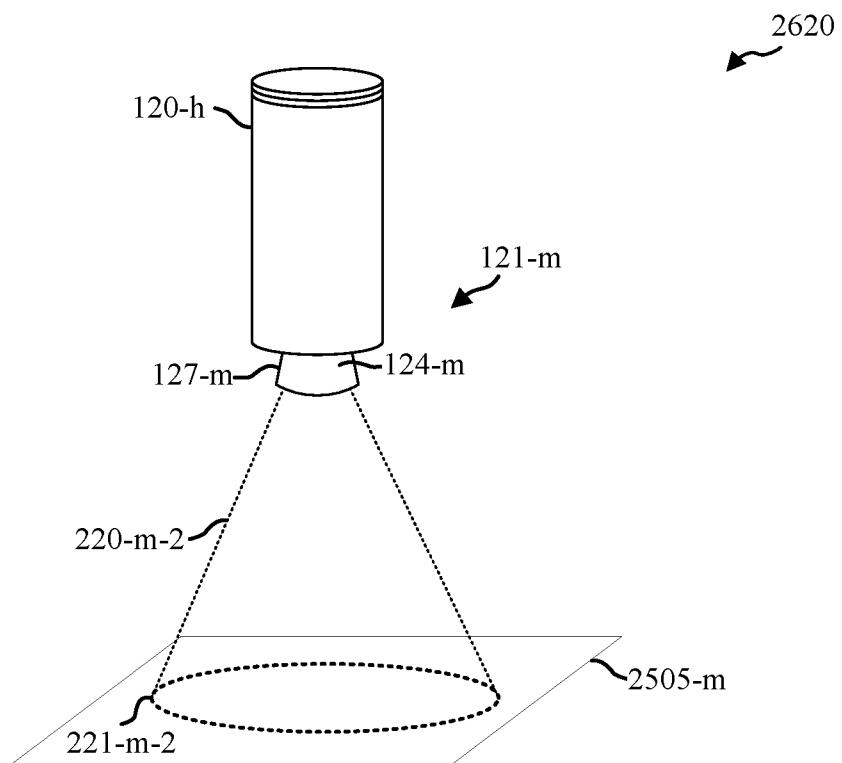


FIG. 26D

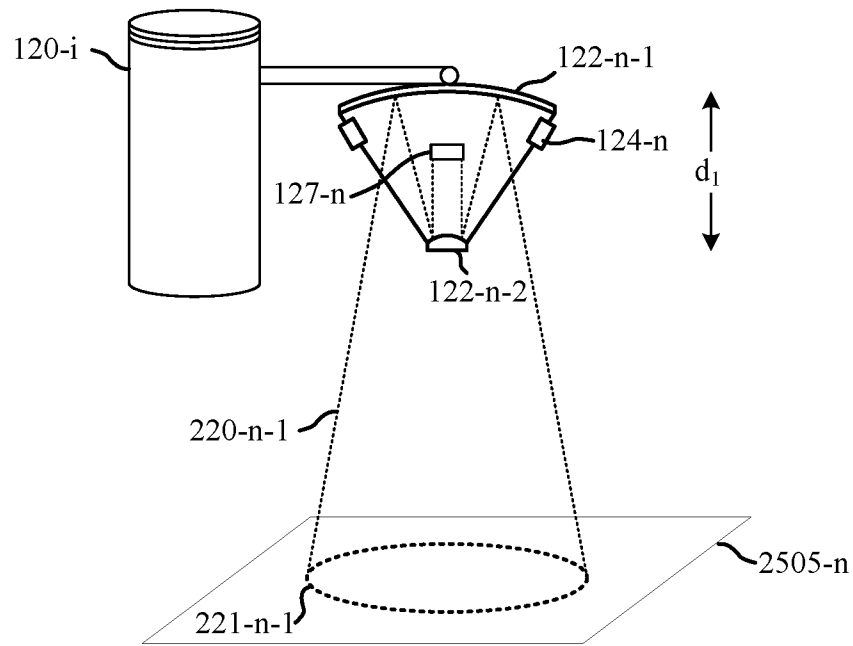
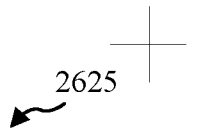


FIG. 26E

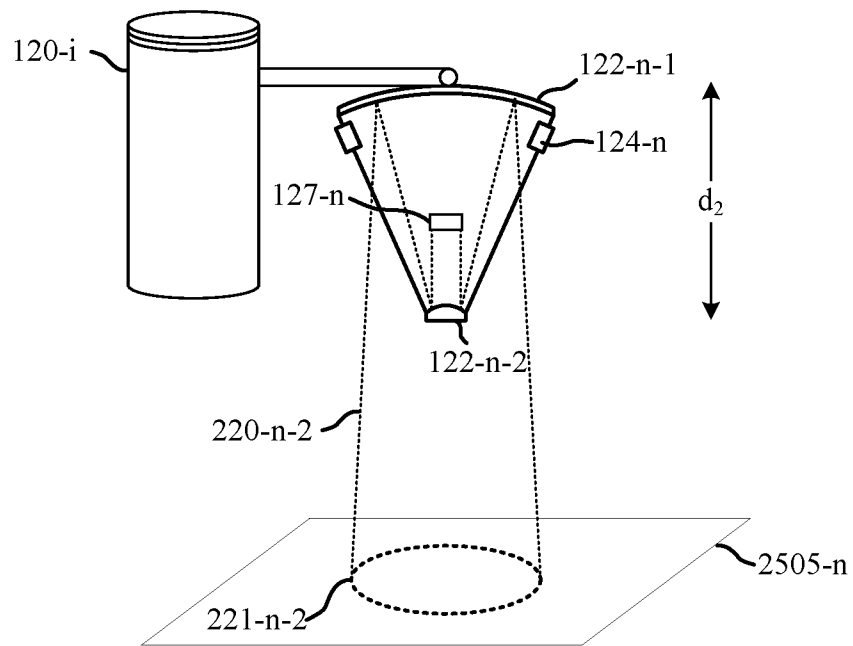
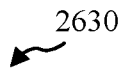


FIG. 26F



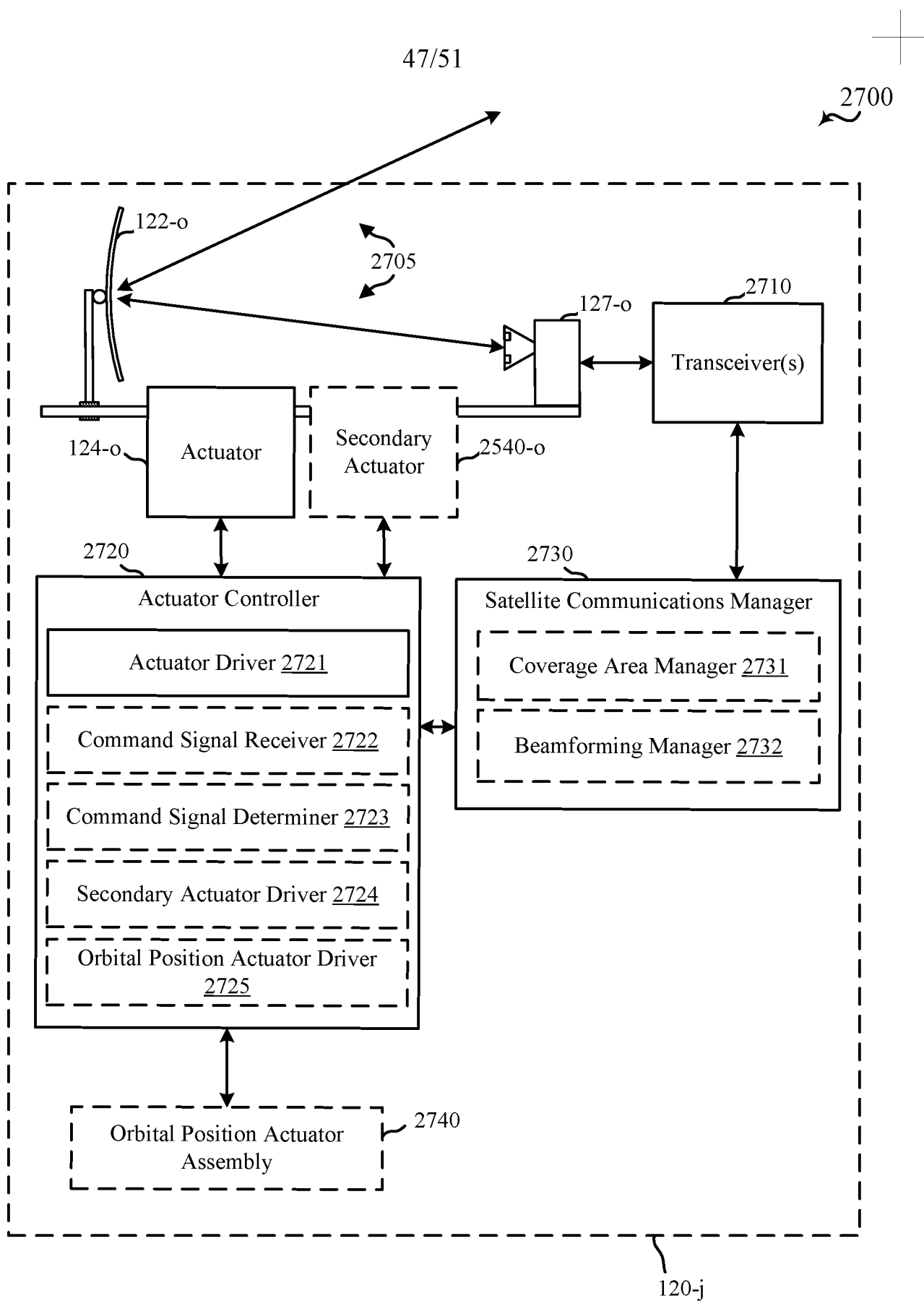


FIG. 27

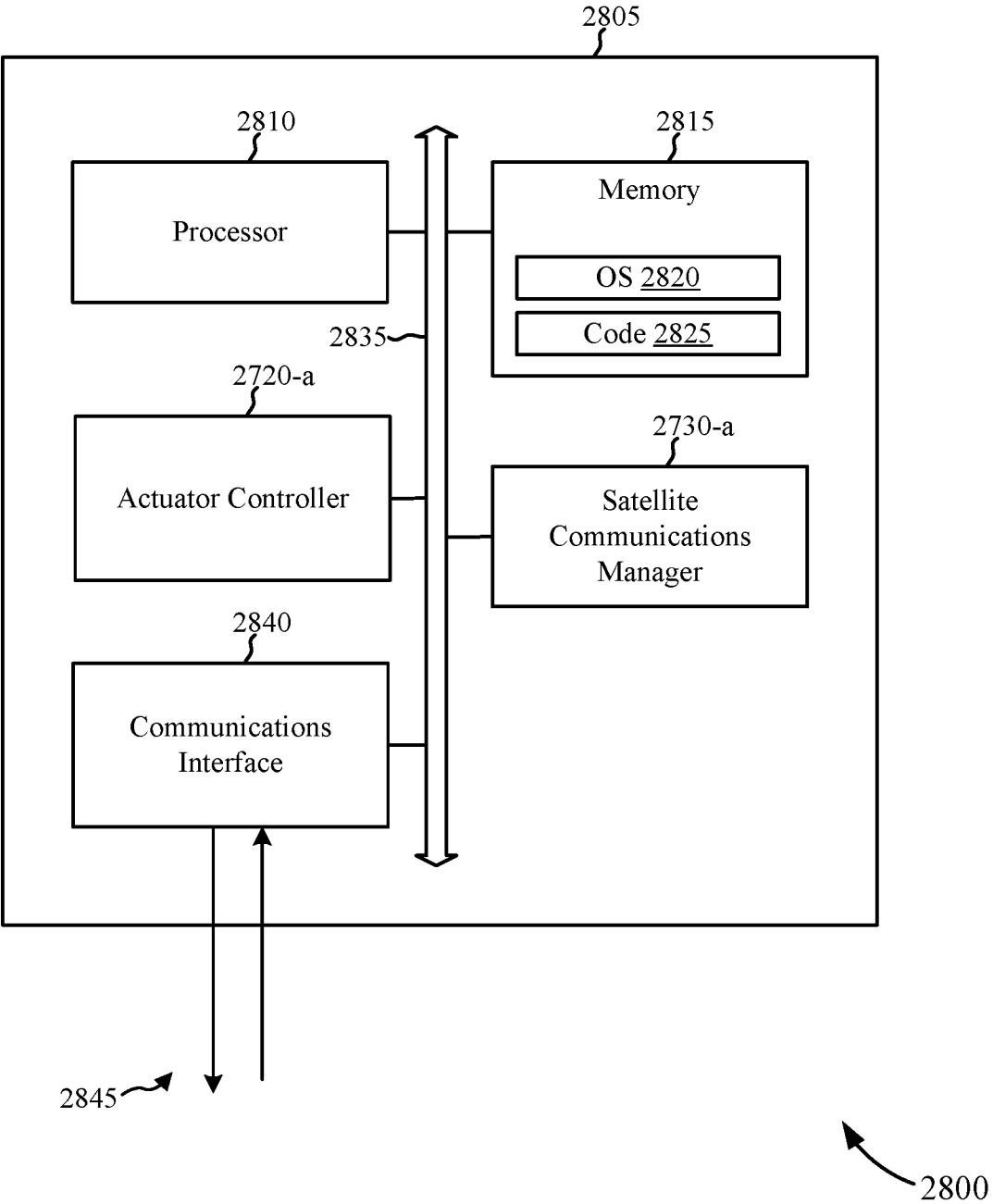


FIG. 28

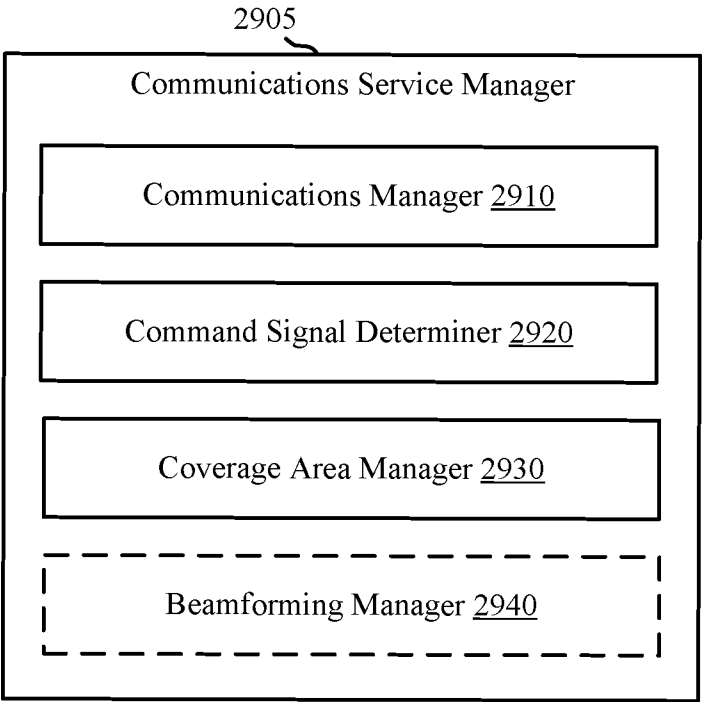


FIG. 29

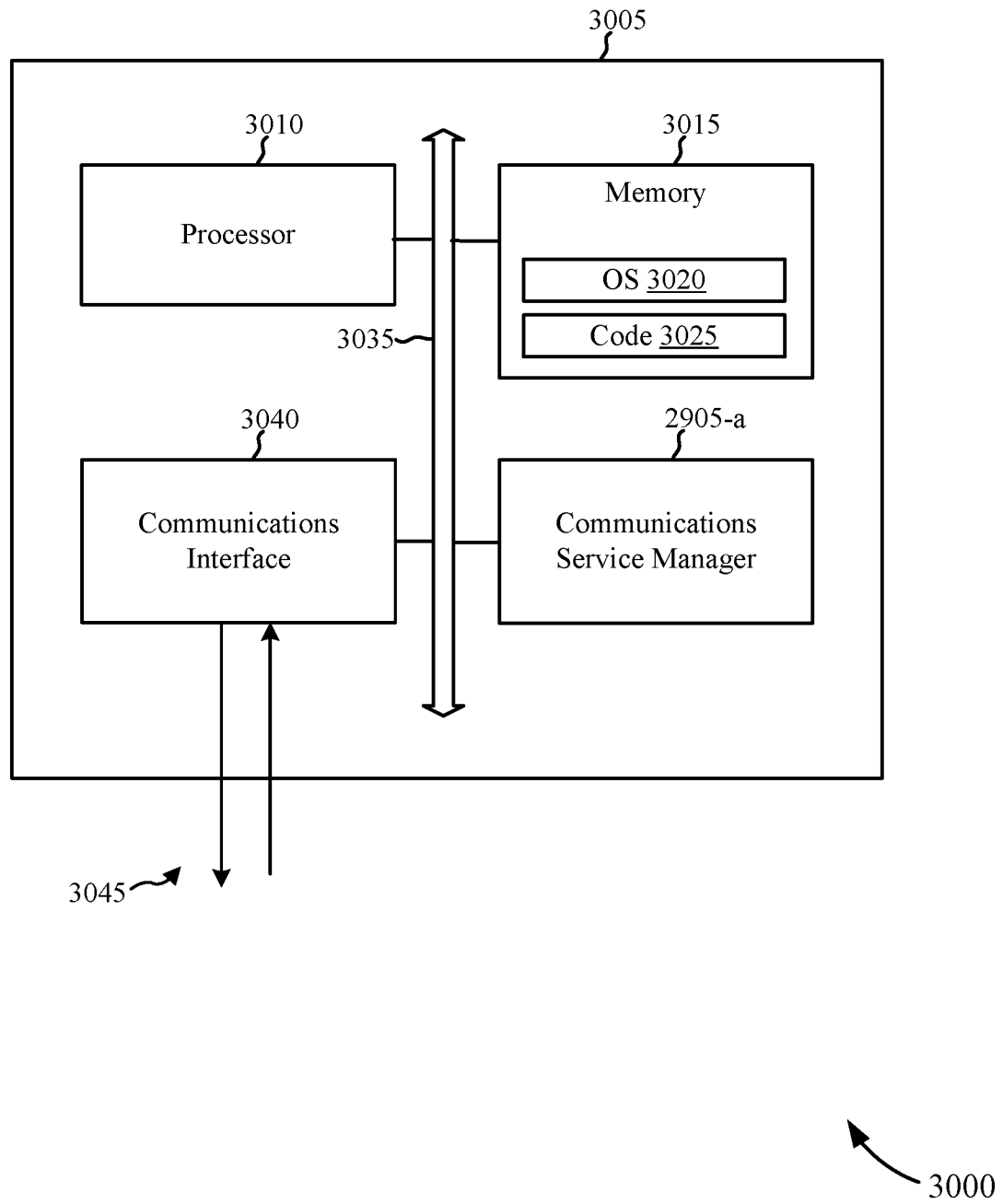


FIG. 30

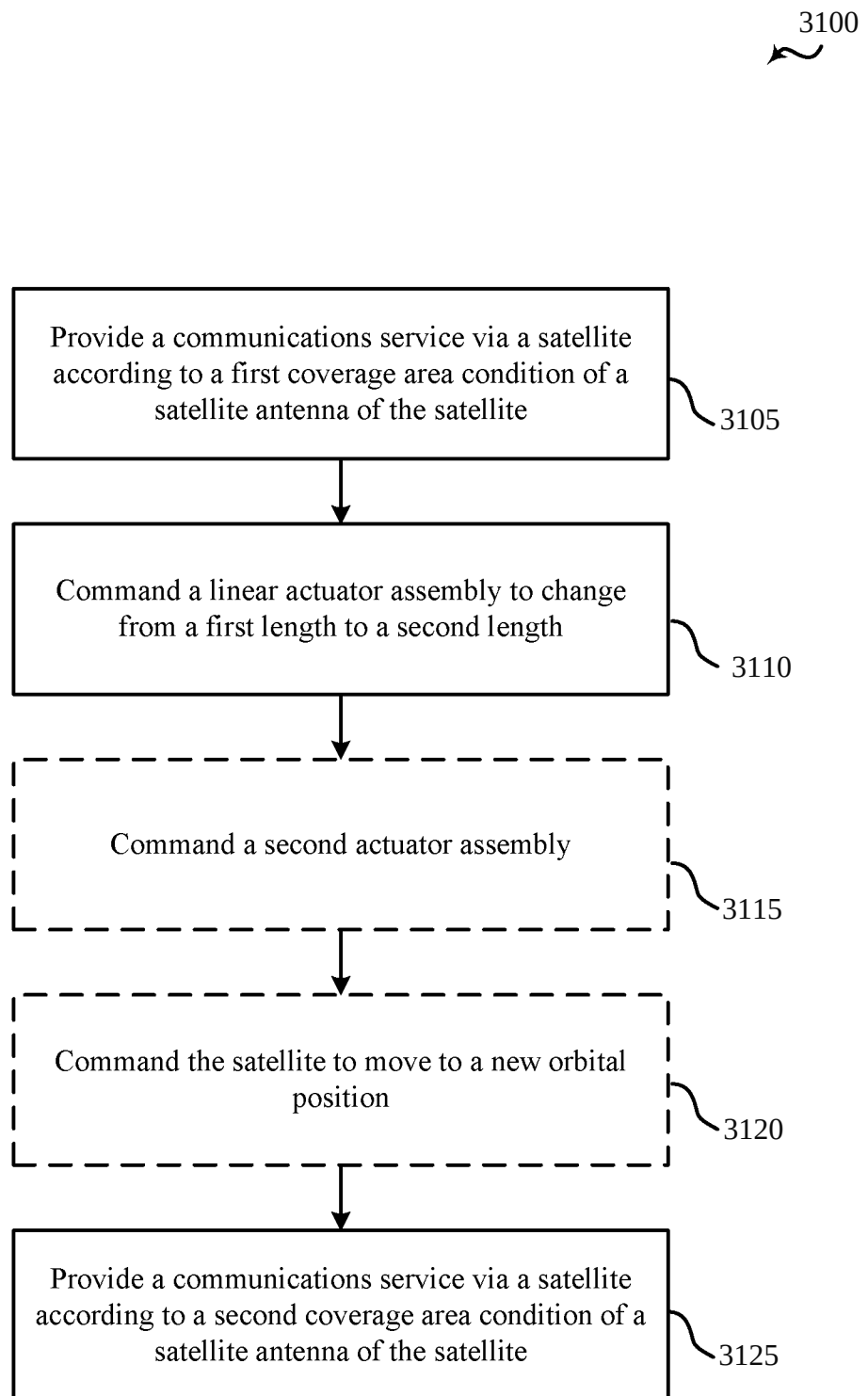


FIG. 31