Method and apparatus for depositing a layer on a semiconductor wafer by vapor deposition in a process chamber

The present invention relates to a method and an apparatus for depositing a layer on a semiconductor wafer by vapor deposition in a process chamber. The invention relates, in particular, to the deposition of an epitaxial layer composed of silicon on a semiconductor wafer composed of monocrystalline silicon, and to an apparatus suitable therefor.

Semiconductor wafers are often provided with a layer produced by means of vapor deposition. The semiconductor wafer is usually held by a rotating susceptor during the deposition of the layer, said susceptor being arranged in a process chamber. Upper and lower covers form boundaries of the process chamber which are transmissive to thermal radiation and through which radiation energy is transmitted into the process chamber and onto the semiconductor wafer. The semiconductor wafer is heated to a specific temperature that is optimal for the deposition of the layer. The process chamber furthermore has on the side walls connections for introducing process gas into the process chamber and for discharging process gas and gaseous products of the process gas from the process chamber. The process gas is conducted over the side area of the semiconductor wafer that is to be coated. Upon contact with the semiconductor wafer heated to deposition temperature, process gas is decomposed and the desired layer is deposited on the semiconductor wafer.

It is necessary to clean the process chamber at specific intervals, because it is not possible to completely prevent products of the process gas from depositing in the interior of the process chamber, for example on parts of the susceptor, the inner surface of the upper cover or the inner side of the side walls. Cleaning is effected by means of vapor phase etching, for example.

Semiconductor wafers cannot be coated during the cleaning of the process chamber. Therefore, there is a great interest in having to carry out the cleaning of the process chamber as infrequently as possible.

For this reason, EP 0 808 917 A1 recommends controlling the temperature of the walls of the process chamber within a narrow temperature range in a control loop. It specifically proposes cooling the process chamber by means of a cooling gas from outside and controlling the temperature of the walls by controlling the inflow of cooling gas to a target temperature.

In accordance with US 2007/0042117 A1 the control of the temperature of the surface of the process chamber can be extended, for example by controlling the temperature of the upper cover of the process chamber and the temperature of the lower cover of the process chamber independently of one another. For controlling the temperature of the covers and the temperature of the substrate to be coated, use is made of pyrometers, inter alia, which measure the temperature of the upper cover on the outer surface of the upper cover, the temperature of the lower cover on the outer surface of the lower cover, the temperature of the substrate in the center of the front side of the substrate and the temperature of the susceptor of the substrate. The control loop also comprises a cooling system that conducts a cooling gas against the upper and lower covers.

The inventor of the present invention has discovered that, despite careful control of the temperature of, for example, the surface of the cover of the process chamber, deficiencies can occur, which concern the properties of the deposited layer or consist in the fact that it is necessary to clean the process chamber comparatively frequently.

Therefore, the object of the present invention is to propose improvements directed against the occurrence of such deficiencies.

The object is achieved by means of a method for depositing a layer on a semiconductor wafer by vapor deposition in a process chamber having an upper and a lower cover, comprising measuring the temperature on the front side of the semiconductor wafer; heating the semiconductor wafer to a deposition temperature; controlling the temperature of the upper cover of the process chamber to a target temperature, wherein the temperature of the upper cover is measured in the center of the outer surface of the upper cover and is used as an actual value of the controlled variable of a control loop for controlling the temperature of the upper cover; setting a gas flow rate with which a process gas for depositing the layer is conducted through the process chamber; and depositing the layer on the front side of the semiconductor wafer heated to the deposition temperature during the control of the temperature of the upper cover of the process chamber to the target temperature.

The invention provides for measuring the temperature of the upper cover in the center of the outer surface of the upper cover and making this temperature available as an actual value of a controlled variable in a control loop by means of which the temperature of the upper cover is controlled to a target temperature. Said target temperature is preferably chosen to lie within an optimum temperature range. The optimum temperature range is a temperature range within which the rate at which products of the process gas deposit on the inner surface of the upper cover is lower than in temperature ranges which adjoin the optimum temperature range. The actual temperature of the upper cover is measured in the center of the outer surface of the cover and hence at a location that

deviates from the location that is disclosed for example in EP 0 808 917 A1.

The present invention takes account of the fact that the coating of the inner surface of the upper cover with products of the process gas begins temporally later in the center of the upper cover than at locations that are distant from the center of the upper cover. The upper and lower covers of the process chamber usually consist of quartz glass, a material that is transmissive to thermal radiation and has a thermal conductivity that is comparatively low. Owing to the latter property, the temperature measured at a location on the outer surface of the upper cover is considerably dependent on the covering of the inner surface of the upper cover at this location by deposits of products of the process gas.

It is therefore advantageous to measure the temperature of the upper cover at a location where there is the lowest probability of the measurement result being corrupted by deposits of products of process gas on the inner surface of the upper cover. This location is the center of the outer surface of the upper cover. Using the measurement of the temperature in the center of the outer surface of the upper cover as an actual value of the controlled variable, the control of the temperature of the upper cover thus ensures that the temperature of the upper cover, regardless of incipient coating of the inner surface of the upper cover, also actually corresponds or virtually corresponds to the target temperature, and thus remains in the optimum temperature range. As a result, this has the effect that the process chamber can be used for depositing a layer on a semiconductor wafer by vapor deposition for a longer period before cleaning has to be effected. If the temperature of the upper cover were measured at a different location, the intervals between two cleanings of the process chamber would have to be shorter.

Preferably, at least one further layer is deposited on at least one further semiconductor wafer before the process chamber is cleaned. The cleaning of the process chamber is preferably effected by means of vapor phase etching.

In accordance with one preferred configuration of the method, the target temperature of the upper cover is chosen in such a way that it correlates with the gas flow rate of the process gas that is set for depositing the layer.

This is because the process gas has a cooling effect on the inner surface of the upper cover. As a result and owing to the low thermal conductivity of the material of the cover, considerable temperature differences between the temperature on the inner and outer surfaces of the upper cover can occur. The temperature measured on the outer surface of the upper cover is then higher than it would be if the thermal conductivity of the material of the upper cover permitted a rapid temperature equalization. If the cooling effect of the process gas were disregarded in the choice of the target temperature, the temperature on the inner surface of the cover, despite the measures for controlling the temperature of the upper cover, could fall out of the optimum temperature range, and the process chamber would have to be cleaned more frequently as a result.

In accordance with a further preferred configuration of the method, after a cleaning of the process chamber, the amount of material deposited on semiconductor wafers is registered in the form of a total thickness, and the process chamber is cleaned again only when a defined total thickness of material has been deposited. The defined total thickness of deposited material corresponds to the sum of the thicknesses of the layers which

are deposited on semiconductor wafers between two cleanings of the process chamber.

Furthermore, provision can be made for cleaning the process chamber again even regardless of the defined total thickness of deposited material after a cleaning in any case when this is advisable on account of the difference between the temperatures on the front side of the semiconductor wafer and on the rear side of the susceptor, particularly when an initial temperature difference that exists during the first deposition after the cleaning of the process chamber has changed by more than 5°C. Such a change in the temperature difference can be regarded as an indicator that indicates that products of the process gas have also deposited in the center of the upper cover on the inner surface of the upper cover. These deposits corrupt the measurement of the temperature of the semiconductor wafer on the front side of the semiconductor wafer. A temperature lying below the true temperature is indicated. Accordingly, the temperature of the semiconductor wafer is already too high if the measurement of the temperature on the front side indicates a temperature corresponding to an envisaged deposition temperature. The measurement of the temperature on the rear side of the susceptor is not impaired by the deposit on the inner surface of the upper cover and indicates the true temperature on the rear side of the susceptor. The increase in this temperature in comparison with the temperature measured on the front side of the semiconductor wafer is therefore an expression of increasing contamination of the inner surface of the upper cover.

In accordance with a further preferred configuration of the method, an epitaxial layer composed of silicon is deposited on a semiconductor wafer composed of monocrystalline silicon by vapor deposition, for example using a mixture of trichlorosilane and hydrogen as process gas.

For the deposition of the epitaxial layer composed of silicon, the process parameters given in the following table are preferably chosen.

Table:

Gas flow rate [slm]	Optimum temperature range [°C]	Second target temperature [°C]
45 - 55	510 - 530	520
56 - 65	525 - 545	535
66 - 80	540 - 560	550

Gas flow rate denotes in the table the gas flow rate of the process gas that is set for depositing the layer.

If the target temperature were set in a manner deviating from the value in the table to a temperature lying below the lower limit of the optimum temperature range, products of the process gas would deposit as deposits having a white hue more rapidly on the inner surface of the upper cover, and more frequent cleaning of the process chamber would be necessary.

If the target temperature were set in a manner deviating from the value in the table to a temperature lying above the upper limit of the optimum temperature range, products of the process gas would deposit as deposits having a brown hue more rapidly on the inner surface of the upper cover, and more frequent cleaning of the process chamber would be necessary.

Preferably, at least one further epitaxial layer composed of silicon is deposited on at least one further semiconductor wafer composed of monocrystalline silicon, and the amount of material that has been deposited on the semiconductor wafers overall since a last cleaning of the process chamber is

registered. The process chamber is cleaned again after the last cleaning only when the total thickness of epitaxially deposited silicon, that is to say the defined total thickness of deposited material, is not less than 50 μm, preferably not less than 80 μm.

The abovementioned object is equally achieved by means of an apparatus for depositing a layer on a semiconductor wafer by vapor deposition, comprising a process chamber having an upper and a lower cover and a first sensor for measuring the temperature of the upper cover in the center of the outer surface of the upper cover, and a controller for controlling the temperature of the upper cover to a predetermined target temperature using the temperature measured by the first sensor as an actual temperature.

Details of a preferred embodiment of the process chamber are explained more specifically below with reference to the figure. The figure shows crucial elements of the invention in a simplified manner.

The process chamber 1 is constructed substantially symmetrically and comprises an upper cover 2, a lower cover 3 and a sidewall 4, which enclose a reactor space, in which a semiconductor wafer is coated by means of vapor deposition. The semiconductor wafer 5 to be coated is held by a susceptor 6 arranged in the reactor space. Radiant heating systems 7 and 8 for heating the semiconductor wafer to a specific deposition temperature are situated above the upper cover 2 and below the lower cover 3. Furthermore, connections 9 and 10 for introducing process gas into the process chamber and for discharging process gas and gaseous products of the process gas from the process chamber through the sidewall 4 of the process chamber are present. The process chamber furthermore comprises a cooling system for cooling the upper cover 2 and the lower

cover 3, for example a fan 18, which conducts a cooling gas against the upper and lower covers, and heat exchangers 11, which draw heat from the cooling gas heated up in contact with the covers. The direction of movement of the cooling gas is indicated by arrows. The cooling system acts as an actuating device of a control loop for controlling the temperature of the upper cover of the process chamber. A sensor 12 forms a measuring element of the control loop. The sensor 12 is preferably a pyrometer with the aid of which the temperature of the upper cover 2 is measured contactlessly. A controller 19 for controlling the temperature of the upper cover to a predetermined target temperature influences the power of the fan 18 depending on the difference between the temperature measured by the sensor 12 and the target temperature. The control loop is directed, in particular, against disturbances that arise as a result of leaks in the housing of the process chamber. Locations at which such leaks can readily occur are highlighted by dashed circles in the figure.

The sensor 12 is arranged according to the invention in such a way that the temperature of the upper cover 2 in the center of the outer surface of the upper cover is measured thereby. This temperature forms the controlled variable of the control loop. The sensor 12 makes available the actual temperature that is compared with the predetermined target temperature.

The target temperature is preferably predetermined by a data memory 15, in which a plurality of temperature values are stored to which are respectively assigned a gas flow rate of the process gas during the deposition of the layer on the semiconductor wafer. The data memory 15 predetermines that temperature value as target temperature which is assigned to the gas flow rate set for depositing the layer.

The apparatus preferably also comprises a measuring unit 16, which registers how much material has been deposited on semiconductor wafers since a last cleaning of the process chamber, and which, after registering a defined total thickness of deposited material, generates a signal for initiating a next cleaning of the process chamber.

A sensor 13 is provided for measuring the temperature of the semiconductor wafer on the front side of the semiconductor wafer. The front side of the semiconductor wafer is that side area on which the layer is deposited. Furthermore, a sensor 14 is provided, which measures the temperature on the rear side of the susceptor 6. The sensors 13 and 14 are preferably likewise embodied as pyrometers and are part of a control loop for controlling the temperature of the semiconductor wafer by means of a controller 20. The sensor 13 is preferably arranged in such a way that it measures the temperature on the front side of the semiconductor wafer in the center of the front side.

The apparatus preferably also comprises a comparison unit 17, which is integrated in the controller 20 and which compares the temperatures measured by the sensors 13 and 14, and which generates a signal for initiating a next cleaning of the process chamber, if the temperature difference between the temperature measured by the sensor 13 on the front side of the semiconductor wafer and the temperature measured by the sensor 14 on the rear side of the susceptor holding the semiconductor wafer deviates by more than 5°C from an initial temperature difference. The initial temperature difference is that which exists during the first deposition after the cleaning of the process chamber which directly precedes the next cleaning.

The controllers 19 and 20, the data memory 15, the measuring unit 16 and the comparison unit 17 can also be parts of an installation control system.

Patent Claims

1. A method for depositing a layer on a semiconductor wafer by vapor deposition in a process chamber having an upper and a lower cover, comprising measuring the temperature on the front side of the semiconductor wafer; heating the semiconductor wafer to a deposition temperature; controlling the temperature of the upper cover of the process chamber to a target temperature, wherein the temperature of the upper cover is measured in the center of the outer surface of the upper cover and is used as an actual value of the controlled variable of a control loop for controlling the temperature of the upper cover; setting a gas flow rate with which a process gas for depositing the layer is conducted through the process chamber; and
depositing the layer on the front side of the semiconductor wafer heated to the deposition temperature during the control of the temperature of the upper cover of the process chamber to the target temperature.

2. The method as claimed in claim 1, wherein the target temperature is chosen in such a way that it correlates with the set gas flow rate of the process gas.

3. The method as claimed in claim 1 or claim 2, wherein at least one further layer is deposited on at least one further semiconductor wafer, and the amount of material that has been deposited on semiconductor wafers since a last cleaning of the process chamber is registered, and the process chamber is cleaned again after the last cleaning only when a defined total thickness of deposited material has been deposited.

4. The method as claimed in claim 3, wherein the temperature is measured on the rear side of a susceptor holding the semiconductor wafer, and wherein at least one further layer is

deposited on at least one further semiconductor wafer, and a next cleaning of the process chamber is initiated, regardless of the defined total thickness of deposited material, if the temperature difference between the temperature on the front side of the semiconductor wafer and the temperature on the rear side of the susceptor has changed by more than 5°C in comparison with an initial temperature difference that exists during the first deposition after the cleaning of the process chamber which directly precedes the next cleaning of the process chamber.

5. The method as claimed in claim 3 or claim 4, wherein the defined total thickness of deposited material is not less than 50 µm, if the semiconductor wafer consists of monocrystalline silicon and the deposited material is epitaxially deposited silicon.

6. The method as claimed in any of claims 1 to 5, wherein an epitaxial layer composed of silicon is deposited on a semiconductor wafer composed of monocrystalline silicon and the target temperature is chosen to lie in a range of 510 to 530°C, if the set gas flow rate of the process gas lies in the range of 45 to 55 slm, wherein the target temperature is chosen to lie in a range of 525 to 545°C, if the set gas flow rate of the process gas lies in the range of 56 to 65 slm, and wherein the target temperature is chosen to lie in a range of 540 to 560°C, if the set gas flow rate of the process gas lies in the range of 66 to 80 slm.

7. An apparatus for depositing a layer on a semiconductor wafer by vapor deposition, comprising a process chamber having an upper and a lower cover and a first sensor for measuring the temperature of the upper cover in the center of the outer surface of the upper cover, and a controller for controlling the temperature of the upper cover to a predetermined target

temperature using the temperature measured by the first sensor as an actual temperature.

8. The apparatus as claimed in claim 7, comprising a data memory, in which a plurality of temperature values are stored which are respectively assigned a gas flow rate of the process gas during the deposition of the layer on the semiconductor wafer, wherein the data memory predetermines that temperature value as target temperature which is assigned to the gas flow rate set for depositing the layer.

9. The apparatus as claimed in claim 7 or claim 8, comprising a measuring unit, which registers how much material has been deposited on semiconductor wafers since a last cleaning of the process chamber, and which, after registering a defined total thickness of deposited material, generates a signal for initiating a next cleaning of the process chamber that follows the last cleaning.

10. The apparatus as claimed in any of claims 7 to 9, comprising a second sensor, which measures the temperature of the semiconductor wafer on the front side of the semiconductor wafer, and a third sensor, which measures the temperature on the rear side of a susceptor holding the semiconductor wafer, and a comparison unit, which generates a signal for initiating a next cleaning of the process chamber, if the temperature difference between the temperature measured by the second sensor and the temperature measured by the third sensor deviates by more than 5°C from an initial temperature difference that exists during the first deposition after the cleaning of the process chamber which directly precedes the next cleaning of the process chamber.