

Description

Method and network component of a communication network for switching low bit rate connections between
5 input assemblies and output assemblies

The invention relates to a method as well as a corresponding network component for switching low bit rate connections between input assemblies and output
10 assemblies of the network component of a communication network.

In communication networks - preferably mobile radio networks or fixed networks - information - for example wanted information or signalling information
15 for voice transmission - is transported at low transmission rates using the time-division multiplex method (TDM) via lines between network components. For example, PCM30 or PCM24 connecting lines can be used for this purpose. ATM transmission (Asynchronous
20 Transfer Mode) is increasingly being used for line information transmission - in fixed networks, but in radio mobile networks as well, particularly for the next generation - with its advantages in terms of broadband applications. Nevertheless, narrowband
25 information transmission via low bit rate connections - for example TDM connections - remains an important application for the majority of mobile network and fixed network subscribers. Thus, if TDM multiplexing technology has to be converted to ATM transmission
30 technology in a network component, a long delay normally occurs - for example 48 ms for 8 kbit/s voice transmission. This leads to a deterioration in the speech quality.

In principle, a way of converting TDM multiplexing
35 technology to ATM transmission technology exists which leads to only short delays - for example by filling the ATM cells with only a small number of bytes - but this results in uneconomic utilization of the ATM bandwidth. For this reason, there has been a problem for some time.

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in providing network components in a telecommunications
network

such that they internally distribute the traffic via an ATM switching device, while at the same time supporting low bit TDM traffic on the external lines.

5 The object of the present invention is to specify
a method and a network component for switching low bit
rate connections on an ATM basis by means of which
method and network component it is possible
simultaneously to achieve as short a delay time as
possible and a high utilization level of the available
10 ATM bandwidth.

This object is achieved according to the invention
by the features of Patent Claim 1 with regard to the
method, and by the features of Patent Claim 18 with
regard to the network component. Developments of the
15 invention are specified in the dependent claims.

The invention relates to the switching of low bit
rate connections between input assemblies and output
assemblies of a network component in a communication
network. According to the invention, the input
20 assemblies and the output assemblies form a first
switching level, and an ATM switching device which is
arranged between the input assemblies and the output
assemblies forms a second switching level. In the first
switching level, a plurality of low bit rate
25 connections which are applied to the input assembly and
are to be transmitted to one and the same output
assembly are in each case combined by the input
assembly to form at least one ATM connection. In the
second switching level, the ATM switching device
30 switches through the ATM connections in order to
transmit information in ATM cells. Then, in the first
switching level, the switched-through ATM connections
of one or more input assemblies are converted by the
output assembly into the low bit rate connections.

35 If the switching process is distributed over two
levels, a plurality of connections are transported
jointly in the same ATM

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connection, so that this results in a short delay and good utilization of the ATM cell capacity as advantages. Combined switching in two switching levels represents a particularly economic solution for functions specific to mobile radios, which at the same time ensures acceptable speech quality with good utilization of the ATM bandwidth. The invention of multi-level switching in an ATM switching device and in input and output assemblies arranged separately from it resolves two contradictory aspects, namely of minimizing the delay resulting from conversion of low bit rate connections into ATM technology, and of increasing the utilization of the ATM bandwidth. The concept of decentralized switching in two levels has the advantage that the switching processes can be carried out at least in a similar manner, or in one and the same way, both in the input/output assemblies and in the ATM switching device. Furthermore, the software and hardware in the switching levels can be matched easily and with little cost by means of a switching controller.

According to a development of the invention, a common control device controls the functions both in the first switching level and in the second switching level. It is particularly advantageous if the ATM switching is operated in the manner of a decentralized switching principle, whose control device initiates setting in the input assemblies and the output assemblies in the first switching level. The combined control of switching levels one and two can be implemented with little hardware and software complexity.

According to alternative developments of the invention, the two-level method can be used for switching irrespective of whether external lines are in each case connected to the input assemblies and output assemblies in the first switching level, via which information is received and transmitted

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by time-division multiplex connections - for example, TDM connections, or whether external ATM lines are in each case connected to the input assemblies and output assemblies in the first switching level, via which
5 external ATM lines the information of a plurality of connections is received and transmitted in structured form in a time-division multiplex frame - for example a TDM frame - or in ATM minipackets.

According to further advantageous refinements of
10 the invention, various methods exist to allow narrowband switching to be carried out in the first switching level. Of these, two methods are based on collecting minipackets in ATM cells, in which case a connection table in the input assembly or output
15 assembly is used to choose which minipackets are inserted into which ATM cell and which minipackets are distributed to which connections of the output assembly. Three methods follow the principle of first combining the connections - for example TDM connections
20 - at common outputs and then of converting them into packet connections, which is equivalent to inputting the information to the ATM cells. This procedure has the advantage that it is possible to achieve a delay reduced by a factor of up 5, while at the same time at
25 least doubling the utilization of the available bandwidth in comparison with the two methods mentioned first of all.

Switching in two levels preferably relates to low bit rate traffic connections, since these make up the
30 majority of the connection traffic, but this can also be applied to signalling connections and to operation and maintenance (O&M) connections.

The invention will be explained in more detail in the following text using exemplary embodiments and with
35 reference to illustrative drawings, in which:

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- Figure 1 shows the block diagram of the network component for switching connections in two switching levels for one connection transmission direction,
- 5 Figures 2, 3 show block diagrams of an input assembly and an output assembly for switching the connections in the first switching level based on the collection of minipackets in ATM cells,
- 10 Figures 4, 5 show block diagrams of an input assembly and an output assembly for switching the connections in the first switching level based on the combination of TDM connections in ATM cells,
- 15 Figure 6 shows the principle of operation of a TDM switching element for the combination of those TDM connections which are associated with the same output assembly, to form common outputs, and
- 20 Figures 7-9 show various principles for filling the ATM cells with the information of the TDM connections.
- 25

Figure 1 shows the block diagram of a network component for switching connections according to the invention in two switching levels for one connection transmission direction, this connection continuing in the following figures. The reverse direction runs parallel to the illustrated transmission direction, so that the following statements apply in a corresponding manner to this reverse direction. The network components in the example is a base station controller BSC or a radio controller RNC (radio network controller) which, as part of GSM mobile radio network or of a universal telecommunications network (UMTS,

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Universal Mobile Telecommunication System), carries out the monitoring and control of radio-engineering tasks - in particular the monitoring of base stations - or a transcoder device (TRAU (Transcoding and Rate
5 Adaptation Unit), as is known for each wanted channel in the GSM mobile radio network,

carries out the matching of the various transmission speeds between the base station controller (BSC) or the radio controller RNC and a switching centre (MSC) connected to it, as well as the transcoder function.

5 In this case, Figure 1 shows the functional structure, which is essentially identical for the network components BSC, RNC, TRAU, for switching the connections, without describing in detail those functions of the respective network component which are
10 not relevant to the invention and are known per se. The switching process according to the invention, characterized by two switching levels, can also be used in the mobile switching centre. Furthermore, the invention is not limited to network components in a
15 mobile radio network but, in principle, [lacuna] in any network component which carries out functions which are specific to fixed networks or mobile radios, such as switching, monitoring, transcoder tasks etc and carries the traffic internally using the ATM transmission
20 technique in this case and supports low bit rate traffic on external lines, for example via TDM connections.

Based on an ATM switching principle, it is possible by means of the proposed invention to produce
25 the network components with the functionalities quoted above by way of example. For this purpose, the network component BSC/RNC/TRAU has an ATM switching device ASW, preferably comprising a plurality of modules ASM (ATM-Switching Module at, for example, 5 Gbps) and a
30 plurality of ATM multiplexers AMX. Line assemblies (line interface circuits) under control device MP-CP are connected to the ATM switching device ASW via multiplexers AMX. The line assemblies carry out the function of an input assembly ILIC or of an output
35 assembly OLIC depending on whether they are arranged on the input side or output side in the transmission path. Thus, in principle, each line assembly covers the function of an input assembly ILIC or an output

assembly OLIC. A plurality of connections TDM-I on the input side are thus

in each case combined by input assemblies ILIC and are passed on via the multiplexers AMX, in the direction I in the illustrated example, to the ATM switching device ASW. The efficiency of narrowband multiplexing in the
5 input assemblies ILIC can be improved by choosing a large number of connections TDM-I, for example eight connections, per assembly.

The ATM switching device ASW in this case forms the second of the two switching levels according to the
10 invention, in which case it operates on the decentralized switching principle, in which the connecting paths are defined by connection tables in the input assemblies ILIC and output assemblies OLIC which are connected, on the input side and output side
15 respectively, to the ATM switching device ASW. The input assemblies ILIC and output assemblies OLIC form the first of the two switching levels according to the invention. A plurality of low bit rate connections TDM-I which are applied to each of the two illustrated
20 input assemblies ILIC and are to be transmitted to the same output assembly OLIC (marked by thick arrows) are in each case combined in the first switching level, by the respective input assembly ILIC, to form at least one ATM connection. In this case, external lines, for
25 example, PCM-30 lines - carry the information for the low bit rate connections TDM-I which, according to the TDM multiplexing method, are contained in a plurality of time slots in a TDM frame.

In the second switching level, the ATM switching
30 device ASW switches through the ATM connections in order to transmit information in ATM cells. Then, in the first switching level, the ATM connections which have been switched through to the output assembly OLIC and come from one or more input assemblies ILIC are
35 converted into low bit rate connections TDM-O by the output assembly OLIC. If the switching process is distributed between two levels according to the invention, one or more

TDM connections on the input side of an input assembly ILIC are transported jointly in the same ATM connection and, on the output side, are correctly assigned to the one output assembly OLIC, thus resulting in a short delay and good utilization of the ATM cell capacity as advantages. A plurality of ATM connections from different input assemblies ILIC can also be passed together to the same output assembly OLIC. Combined switching in two switching levels represents a particularly economic solution, which at the same time ensures acceptable speech quality with good utilization of the ATM bandwidth. The invention of multi-level switching in an ATM switching device and in input and output assemblies ILIC and OLIC arranged separately from it resolves two contradictory aspects, namely minimizing the delay resulting from conversion of low bit rate connections into ATM technology, and of improving the utilization of the ATM bandwidth. The concept of decentralized switching in two levels has the advantage that the switching processes can be carried out at least in a similar manner, or in one and the same way, both in the input/output assemblies and in the ATM switching device ASW. This two-level switching method can also be used if the input and output assemblies ILIC and OLIC are connected to external ATM lines which transmit the information in a structured manner either using the TDM frame structure or as ATM minicells (in accordance with AAL 2, ATM Adaptation Layer 2, minicells).

Control devices or call processing may be distinguished from control devices for signalling and O&M tasks. The switching work in the first switching level and in the second switching level is carried out by the control device MP-CP (Main Processor for Call Processing), which is coupled to the ATM switching device. This has the advantage that, owing to the decentralized switching principle, the control device MP-CP has to make settings only on the input and output assemblies

ILIC and OLIC, in order to provide control at both the first level and the second level. If any of the three switching units were to be left on its own, that is to say corresponding to a network composed of switching
5 nodes, then three control devices would have to coordinate their actions for each signalling activity on each connection. This is avoided by means of the one processor which carries out the entire control task. This combined controller can be produced with
10 relatively low hardware and software complexity and, if required, is easy to adapt to changes, at low cost.

If the network component is in the form of a base station controller/radio controller BSC/RNC with additional functionality comprising the support of data
15 transmission in accordance with a packet data service GPRS (General Packet Radio System) a device SPU (Signal Processing Unit) may be added to the arrangement (illustrated by dashed-dotted lines). The device SPU, which is likewise connected to the modules ASM via a
20 multiplexer AMX, has a line assembly which, as an output assembly OLIC, converts incoming ATM cells into TDM connections TDM-O and, as an input assembly ILIC, converts incoming TDM connections TDM-I to ATM cells. Furthermore, the device SPU has a digital signal
25 processor DSP for processing TDM-oriented functions - for the purposes of the GPRS service - on the basis of the information contained in the TDM connections. In the situation where the GPRS service is operated by the base station controller BSC or radio controller RNC,
30 the connection initially runs from an input assembly ILIC (arrow I marked by a thick line) via the ATM switching device ASW into the device SPU (arrow II marked by a thick line), and, after signal processing by the device SPU (arrow II marked by a thick line),
35 once again runs via the ATM switching device ASW into the output assembly OLIC. If the invention is applied to a transcoder device TRAU as the network component, what has been said above applies in a corresponding manner, in which case the device

SPU is always connected in the transmission path, rather than optionally depending on the additional functionality. In this case, it is operated as a transcoder assembly in order to carry out transcoder functions.

One alternative to passing through the ATM switching device ASW twice for the abovementioned purpose is for the devices ILIC and SPU in the transmission path II to be replaced by a signal device SPU*. This likewise has a digital signal processor DSP for TDM signal processing as well as a line assembly with the functionality of an input assembly ILIC, so that the information on the TDM connections TDM-I on the input side can thus be processed before conversion into ATM cells, and the switching for the output assembly OLIC is carried out via the ATM switching device ASW (arrow III marked by a thick line).

Figure 2 and Figure 3 show block diagrams of an input assembly ILIC and of an output assembly OLIC for switching the connections in the first switching level based on the collection of minipackets in ATM cells. Figure 2 shows the transmission path for the information in the input assembly ILIC from the incoming connections TDM-I on the input side to the outgoing ATM cells on the output side, which are passed on to the ATM switching device. Analogously to this, Figure 3 shows the transmission path for the information in the output assembly OLIC from the incoming ATM cells on the input side to the outgoing connections TDM-O on the output side.

The arriving TDM bit stream is used to form minipackets, which are collected in minipacket collectors MPC, with one such minipacket MPC being available for each connection - for example a wanted connection for voice transmission. Minipackets consist of a packet header and a packet body. The minipacket header contains at least the connection

address for definition of the respective connection. In addition, security fields, details about the length of the minipacket, and sequence numbers etc may also be included. The body contains the connection data which is intended to be transmitted. The minipacket body is formed by collecting from each arriving TDM frame those time slots which are associated with the respective voice connection. The body has a length of a few bytes. The delay time is thus as short as if the ATM cells were partially filled. Since it is possible to accommodate a plurality of minipackets in one ATM cell at the same time, this results in the advantage of better utilization of the transport capacity of the ATM cells. The format of the packet header of the minipackets may preferably be different. This may either be a proprietary format, in order to manage with as few bits as possible, or else the format which has been defined in the Standard for the AAL 2. The smaller number of bits in the proprietary format is feasible if a fixed body length is chosen and checksum bits are dispensed with, since the first switching level provides protection in any case.

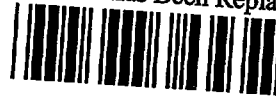
ATM cells may then be composed in ATM cell collectors ACC from the collected minipackets. A connection table CONT1 defines which minipacket is associated with which ATM cell collector ACC. The entries and deletions in this table are carried out by the control processor during the call setting up and clearing procedure, as shown in Figure 1. In parallel with this, the control processor also processes the other connection table CONT2 on the input assembly ILIC, the mirror-image connection table CONT2' on the output assembly OLIC (Figure 3) and its connection table CONT1'. By processing the connection table CONT1 or CONT1', the first switching level is controlled, and by processing the connection table CONT2 or CONT2', the first switching level is controlled. In order to switch the second switching level, the control processor defines, in the connection table CONT2 of the input

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assembly ILIC for each ATM cell collector ACC, the output assembly OLIC to which its ATM cells are intended to be passed. The information about the

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respective output assembly OLIC is contained in the ATM cell header. ATM cells leave the ATM cell collectors ACC when at least one of two conditions is satisfied. Either the ATM cell is full, or the maximum permissible
5 filling time has been reached. The maximum permissible filling time must be observed, since minipackets must arrive at the receiver within a specific tolerance band around the delay, but, at the same time, there is no assurance that a sufficient number of minipacket
10 collectors MPC will serve the ATM cell collector ACC in order to fill the ATM cell sufficiently quickly.

After leaving the ATM cell collector ACC, the ATM cells pass through a delay device DEL, in the simplest case in the form of parallel delay elements for the ATM
15 cells emitted by the ATM cell collectors ACC, with random delay time. This avoids all the ATM cell collectors ACC in the input assembly ILIC emptying their ATM cells into a downstream ATM cell memory ACB at the same time, with the ATM cells being transported
20 onwards from there to the ATM switching device ASW. Simultaneous emission of ATM cells is a risk when, using the principle of TDM transmission, all the external TDM lines which are connected to the input assembly ILIC are synchronized both with regard to the
25 clock and the phase of the TDM frame. If the ATM cell memory ACB is not sufficiently large, cells could be lost or the maximum permissible fluctuation tolerance of the delay could be exceeded. The delay device DEL is with a random delay time is therefore connected between
30 the ATM cell connectors ACC and the ATM cell memory ACB.

Normally, a plurality of ATM connections from different input assemblies ILIC - for example the two illustrated in Figure 1- meet at the output assembly
35 OLIC, switched by the ATM switching device ASW. The associated ATM cells are collected in an ATM cell memory ACB on the input side. The information in the ATM

cell header is used to determine which ATM cells come from which input assembly ILIC, and the connection table CONT2' distributes the ATM cells over a plurality of minipacket generators MPG. The minipackets are
5 deleted from the ATM cells in each minipacket generator MPG, and these are buffer stored in downstream minipacket collectors MPC. From there, the minipackets are converted into the connections TDM-O with a TDM bit stream, in such a manner that the contents of the
10 minipackets are connected to the respective externally connected output line with the corresponding time slot. An information item in the packet header of the minicells provides the correct destination. The connection table CONT1' in the output assembly OLIC
15 ensures correct association between minipackets and minipacket collectors MPC, and the connection (time slot and output line).

In principle, a single ATM connection is sufficient to transport all the minipacket connections
20 from the input assembly ILIC to a specific output assembly OLIC even if the positions of TDM connections on the input side and TDM connections on the output side differ. In order to allow minipacket connections to be distinguished from one another, a sufficiently
25 large address area is preferably used, which can be addressed via the minipacket header. A maximum of 248 minicell addresses are available in the standardized AAL 2 method. If these are exhausted, a further ATM connection is set up between the input and output
30 assembly. As an alternative to this, the proprietary format also allows the address area to be designed to be very much larger, and saves the effort for setting up further ATM connections.

Figure 4 and Figure 5 show block diagrams of an
35 input assembly ILIC and an output assembly OLIC for switching the connections in the first switching level, based on the collection of TDM connections in ATM cells. While the method shown in Figure 2 and Figure 3 follows the principle

of assembling TDM connections into packets byte-by-byte, these connections are processed bit-by-bit in the example shown in Figure 4 and Figure 5. This has the advantage that the delay time is just as short as for
5 conventional line-oriented (circuit switched) [lacuna]. At the same time, the utilization of the available bandwidth is at least twice as great as in the procedure shown in Figure 2 and Figure 3, since no minipacket header is required to identify the
10 narrowband connection, because the position in the TDM frame is used for this purpose. Narrowband switching in the input assembly ILIC, in the same way as in the output assembly OLIC, uses a time and physical position change, which results in TDM frames once again. This
15 task is carried out by a TDM switching element BSW (bit switch) which is able to switch low bit rate connections TDM-I which arrive on the input side in the input assembly ILIC to low bit rate connections TDM-O' on the output side, and to switch low bit rate
20 connections TDM-I' which arrive in the output assembly OLIC on the input side to low bit rate connections TDM-O on the output side.

Specifically, as shown in the illustration in Figure 6, this means that the TDM switching element BSW
25 can switch each individual bit in a TDM frame TDM-FR, split into connecting bits TCHB and synchronization bits SYNBN. For example, for PCM transmission, an 8 kbit/s channel is represented by in each case one bit per PCM frame (frame cycle time 125 μ s). The TDM
30 switching element BSW assigns all the TDM connections TDM-I and TDM-I' at the input which are associated with the same output assembly to one or more common outputs, which carry the TDM connections TDM-O' and TDM-O. A plurality of common outputs are required if more TDM
35 connections have to lead to the same output assembly and than be accommodated by a TDM frame TDM-FR. For example, one PCM30 frame can transport a maximum of 240 sub-multiplex connections at 8 kbit/s each. A connection table CONT1 ensures the assignment

(described above) of the TDM-I connections to the TDM-
O' connections, while the connection

table CONT1' provides the assignment of the TDM-I' connections to the TDM-O connections within the TDM switching element BSW. These connection tables CONT1 and CONT1' are also preferably controlled by the one
5 control device (MP-CP in Figure 1).

According to Figure 4, the information on the bit stream provided by the TDM switching element BSW is combined in the downstream ATM cell collectors ACC to form ATM cells, which are then written to the ATM cell
10 memory ACB - using the connection table CONT2 to switch through the ATM connection or connections in the ATM switching device ASW. The second step, which has to be carried out in the input assembly ILIC after multiplexing of the TDM connections, thus comprises the
15 process of packing the information carried by the TDM connections at the outputs of the TDM switching element BSW into the ATM cells. Alternative principles exist for this second step, and these are illustrated in Figures 7 to 9.

According to Figure 5, the ATM connections from the various input assemblies ILIC are combined in the output assembly OLIC, switched via the ATM switching device ASW. The associated ATM cells are collected in the ATM cell memory ACB on the input side. From there,
20 the ATM cells pass into the respective ACM cell collectors ACC, with the assignment being carried out by the connection table CONT2' in the output assembly OLIC, and with this connection table CONT2' being that which is used to switch through the ATM connection or
25 connections. The ATM cells coming from the ATM cell collectors ACC are then depacketized, so that parallel bit streams of information are supplied to the respective TDM connections TDM-I' on the input side of the TDM switching element BSW and, as shown in the
30 illustration in Figure 6, are switched to the TDM connections TDM-O on the output side in the output assembly OLIC.
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Figure 7 to Figure 9 show different principles for filling the ATM cells with the information of the TDM connections. A common feature of all these figures is that one or more TDM frames TDM-FR arrive, with the
5 connecting bits TCHB and the synchronization bits SYNBN, from the respective output of the TDM switching element BSW, are entered as ATM cells ATM-C in the ATM cell memory, and are passed on from there to the ATM switching device. Each ATM cell ATM-C has, as is known,
10 a header field AHD and a data field ADAT.

In Figure 7, the bits coming from the TDM output are written sequentially into the ATM cell ATM-C. As soon as the ATM cell ATM-C is full, it is despatched. Thus, no consideration is given as to whether a bit
15 belongs to a TDM connection for wanted information or for signalling information from the connecting bits TCHB, or originates from the synchronization bits SYNBN of the TDM frame TDM-FR. There is therefore no relationship between the phase of the TDM frame and the
20 position of the TDM information in the ATM cell. With this method, the TDM frames can easily be packed into ATM cells, and the entire available ATM bandwidth is used.

In an alternative method to this shown in Figure
25 8, all the TDM time slots apart from the synchronization time slot are packed into the ATM cells by means of AAL1 (ATM Adaptation Layer 1). In order that the receiving end can recognize the position of the TDM time slots within the ATM cell, a pointer POI
30 is additionally inserted into every eighth ATM cell ATM-C, indicating the start of the TDM structure, which can be identified from the first information byte DB0. For this situation, the ATM cells ATM-C are referred to as "structured AAL1 cells". The AAL1 method provides
35 for the ATM cells to be despatched periodically. The period is in this case matched to the data rate of the TDM output, such that each ATM cell is completely filled. This method thus uses the entire available ATM bandwidth,

and simplifies synchronization at the ATM receiving end.

In a further alternative method, shown in Figure 9, each ATM cell ATM-C has one, and only one TDM frame TDM-FR. This is positioned in the ATM cell ATM-C such that its synchronization byte SYNBN can always be found at the same point. In this method as well, the ATM cells are dispatched periodically, and the packing process takes account of the TDM frame structure. The ATM bandwidth is thus not fully utilized, but the TDM synchronization at the ATM receiving end can be implemented well and, in addition, operates in the same way for PCM30 and PCM24 connecting lines as carriers for low bit rate TDM connections.



Patent Claims

1. Method for switching low bit rate connections between input assemblies (ILIC) and output assemblies (OLIC) of a network component (for example BSC, RNC, TRAU) of a communication network, in which
- the input assemblies (ILIC) and the output assemblies (OLIC) form a first switching level,
 - an ATM switching device (ASW) which is arranged between the input assemblies (ILIC) and the output assemblies (OLIC) forms a second switching level
 - in the first switching level, a plurality of low bit rate connections (TDM-I) which are applied to the input assembly (ILIC) and are to be transmitted to the same output assembly (OLIC) are in each case combined by the input assembly (ILIC) to form at least one ATM connection,
 - in the second switching level, the ATM connection is switched through by the ATM switching device (ASW) in order to transmit information in ATM cells, and
 - in the first switching level, the switched-through ATM connections of one or more input assemblies (ILIC) are converted by the output assembly (OLIC) into the low bit rate connections (TDM-O).
2. Method according to Claim 1, in which a common control device (MC-CP) is used to control the functions in the first and second switching levels.
3. Method according to Claim 1 or 2, in which the ATM switching device (ASW) is operated in the manner of a decentralized switching principle, whose control device (MP-CP) initiates settings in the input assemblies (ILIC) and the output assemblies (OLIC) in the first switching level.
4. Method according to one of the preceding claims, in which



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external lines, via which information from time-division multiplex connections (TDM) is received and transmitted, are in each case connected to the input assemblies (ILIC) and output assemblies (OLIC) in the first switching level.

5 5. Method according to one of Claims 1 to 3, in which
external ATM lines are in each case connected to the input assemblies (ILIC) and output assemblies (OLIC) in
10 the first switching level, via which external ATM lines the information of a plurality of connections is received and transmitted in structured form in a time-division multiplex frame or in ATM minipackets.

15 6. Method according to one of the preceding claims, in which
minipackets are in each case collected and ATM cells are formed from the collected minipackets in the input assemblies (ILIC) in the first switching level, in which case a connection table (CONT1) is used to select
20 which minipackets are inserted into which ATM cell.

25 7. Method according to Claim 6, in which
the ATM cells pass through a delay device (DEL), which operates with a random delay time, of the input assembly (ILIC), before they are buffer stored in an
ATM cell memory (ACB) and are sent to the ATM switching device (ASW) in the second switching level.

30 8. Method according to Claim 6 or 7, in which
the minipackets each have a packet header having at least one connection address, for which a proprietary header format or a standardized header format is used.

35 9. Method according to one of the preceding claims, in which, in order to switch the connections in the output assemblies (OLIC) in the first switching level, ATM cells are in each case collected and minipackets are generated from the ATM cells and are buffer stored, in which case a connection table



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(CONT1') is used to select which minipackets are distributed to which connections of the output assembly (OLIC).

10. Method according to one of Claims 1 to 5, in which the connections (TDM-I, TDM-I') in the input assemblies (ILIC) and output assemblies (OLIC) in the first switching level are respectively multiplexed and demultiplexed by a switching element (BSW), in which case the connections are assigned to the outputs using a connection table (CONT1, CONT1').

11. Method according to Claim 10, in which ATM cells are formed and collected in the input assemblies (ILIC) from the information multiplexed at the common outputs, before this information is buffer stored in an ATM cell memory (ACB) and is sent to the ATM switching device (ASW) in the second switching level.

12. Method according to Claims 10 or 11, in which incoming ATM cells are buffer stored in an ATM cell memory (ACB) in the output assemblies (OLIC) in the first switching level, and are then collected before they are supplied to the switching element (BSW).

13. Method according to one of the preceding claims, in which a further connection table (CONT2) on the input assembly (ILIC) is used to select which ATM cells are switched through to which output assembly (OLIC) by the ATM switching device (ASW) in the second switching level.

14. Method according to one of the preceding claims, in which a further connection table (CONT2') on the output assembly (OLIC) is used to select which ATM cells are distributed to which ATM cell collector (ACC) or to which minipacket generator (MPG).



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15. Method according to one of Claims 11 to 14, in which

the ATM cells (ATM-C) are filled in such a manner that the information which arrives at a common output is entered in the ATM cell (ATM-C) serially and successively irrespective of whether this is wanted information or signalling information.

16. Method according to one of Claims 11 to 14, in which the ATM cells (ATM-C) are filled, as structured ATM cells, with the information which arrives at a common output and includes a pointer (POI) to identify the start of the structure.

17. Method according to one of Claims 11 to 14, in which some of the ATM cells (ATM-C) are filled with the information which arrives at a common output, and each contain synchronization information located at the same point.

18. Network component (for example BSC, RNC, TRAU) for carrying out the method according to one of Claims 1 to 17.

19. Network component (for example BSC, RNC, TRAU) according to Claim 18, having

- a first switching level which is formed by the input assemblies (ILIC) and the output assemblies (OLIC),
- devices in the input assembly (ILIC) in the first switching level, which each comprises a plurality of low bit rate connections (TDM-I) for at least one ATM connection, which connections (TDM-I) are applied to the input assembly (ILIC) and are to be transmitted to the same output assembly (OLIC),
- a second switching level which is formed by an ATM switching device (ASW) arranged between the input assemblies (ILIC) and the output assemblies (OLIC) and switches through the ATM connections in order to transmit information in ATM cells, and



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- devices in the output assembly (OLIC) in the first switching level, which converts the ATM connections of one or more input assemblies (ILIC), which are switched through to the output assembly (OLIC), into the low bit rate connections (TDM-O).

20. Network component according to Claim 18 or 19, for carrying out a function which is specific to mobile radios.

21. Network component according to one of Claims 18 to 20, designed as a base station control device (for example BSC), or as a radio controller (for example RNC) in order to monitor base stations in a mobile radio network.

22. Network component according to one of Claims 18 to 20, designed as a transcoder for the transcoder device (for example TRAU) of a mobile radio network.

23. Network component according to Claim 18 or 19, for carrying out a function which is specific to fixed networks.



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