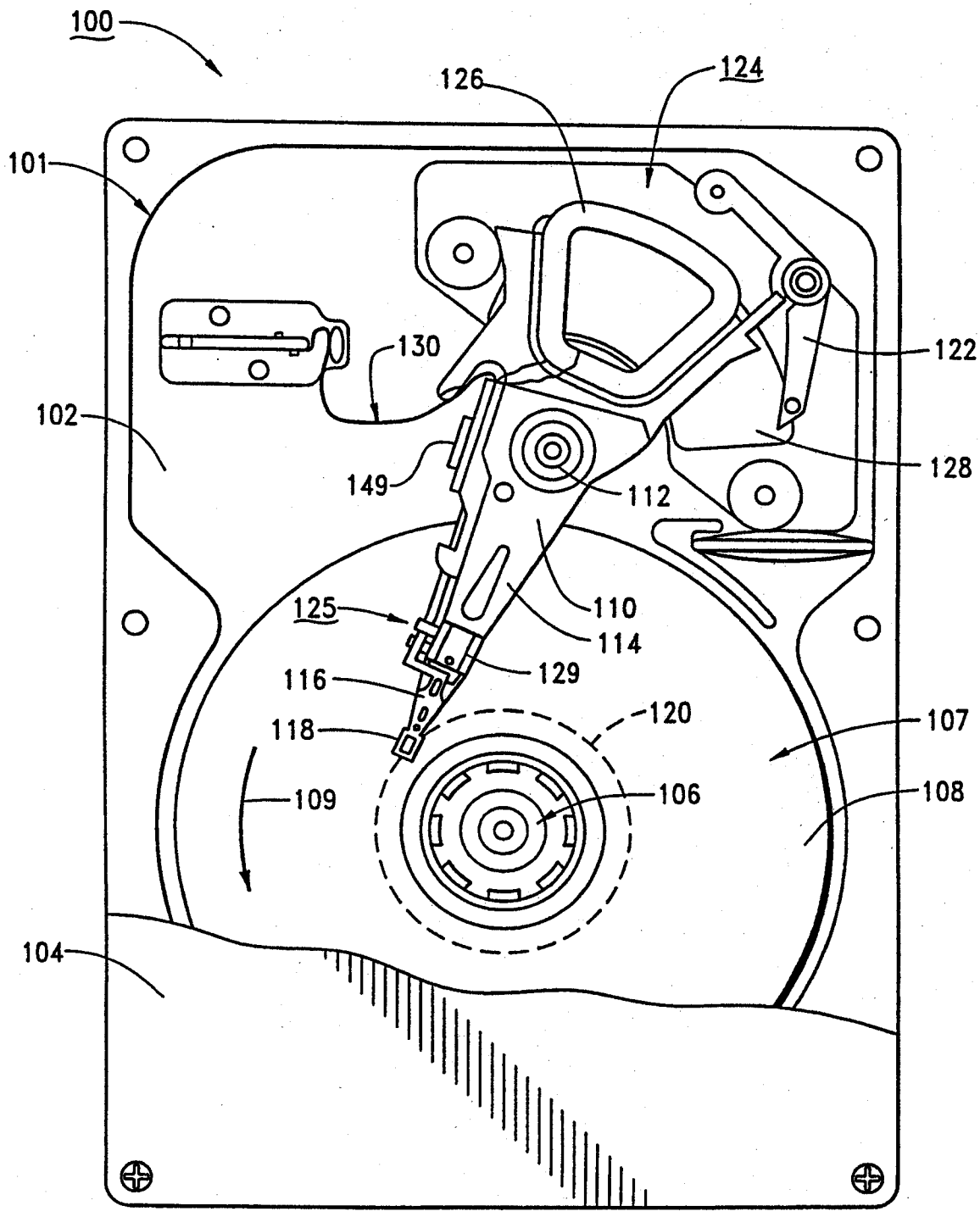

100
126
124
101
130
122
102
149
112
128
125
110
114
116
129
120
118
107
109
106
108
104

FIG. 1

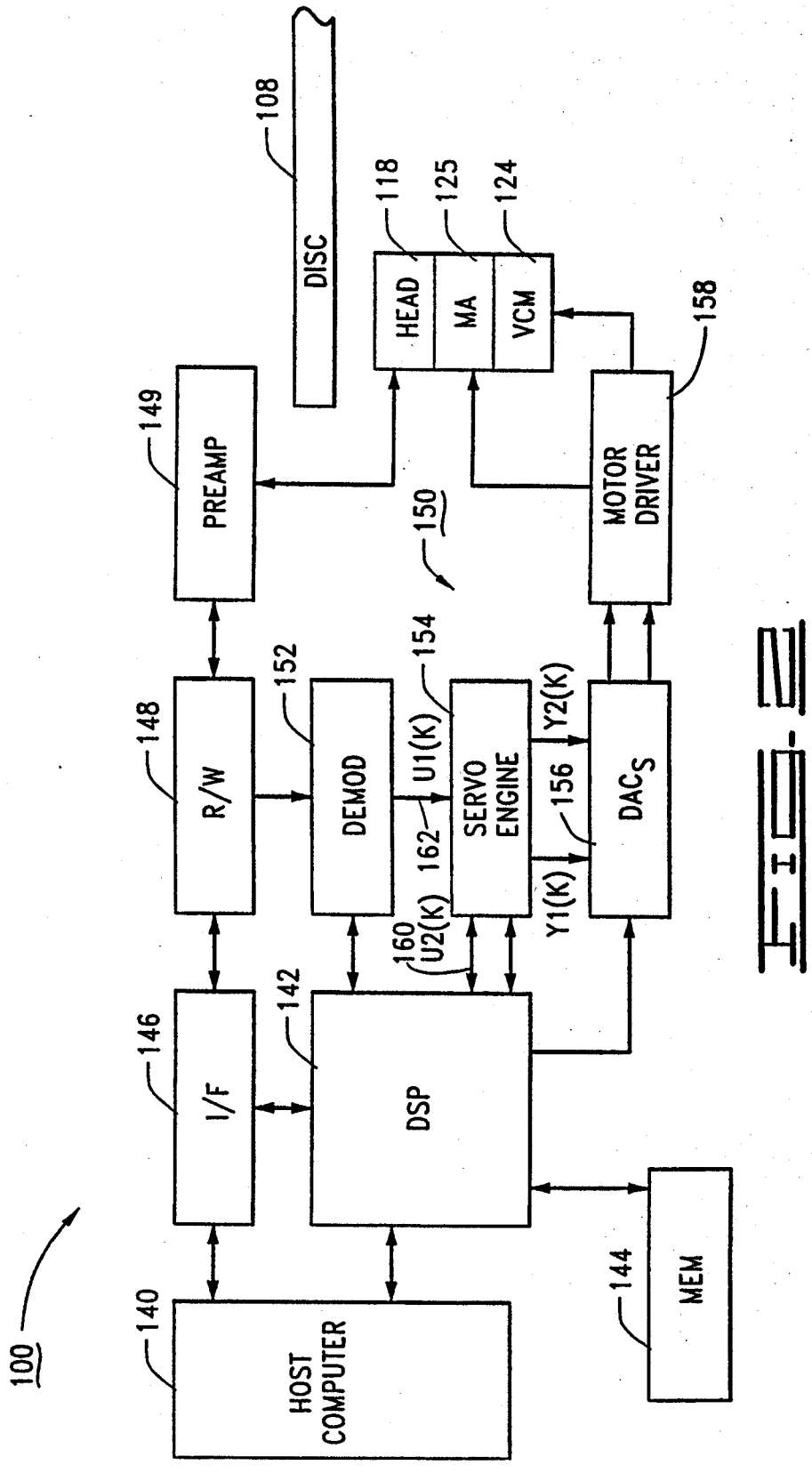
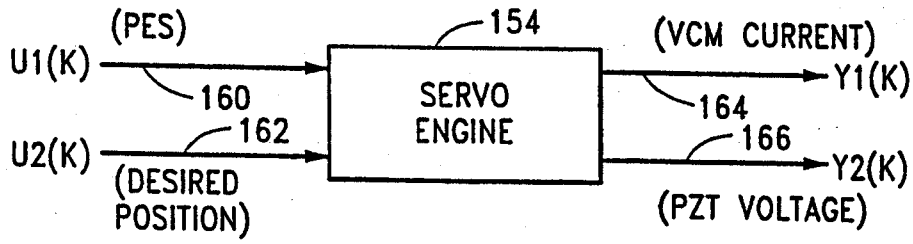

100
HOST COMPUTER
140
I/F
146
DSP
142
MEM
144
R/W
148
DEMOD
152
SERVO ENGINE
154
DACS
PREAMP
149
MOTOR DRIVER
158
HEAD
118
MA
125
VCM
124
DISC
108
150
U1(K)
U2(K)
160
162
Y1(K)
Y2(K)
156

FIG. 2

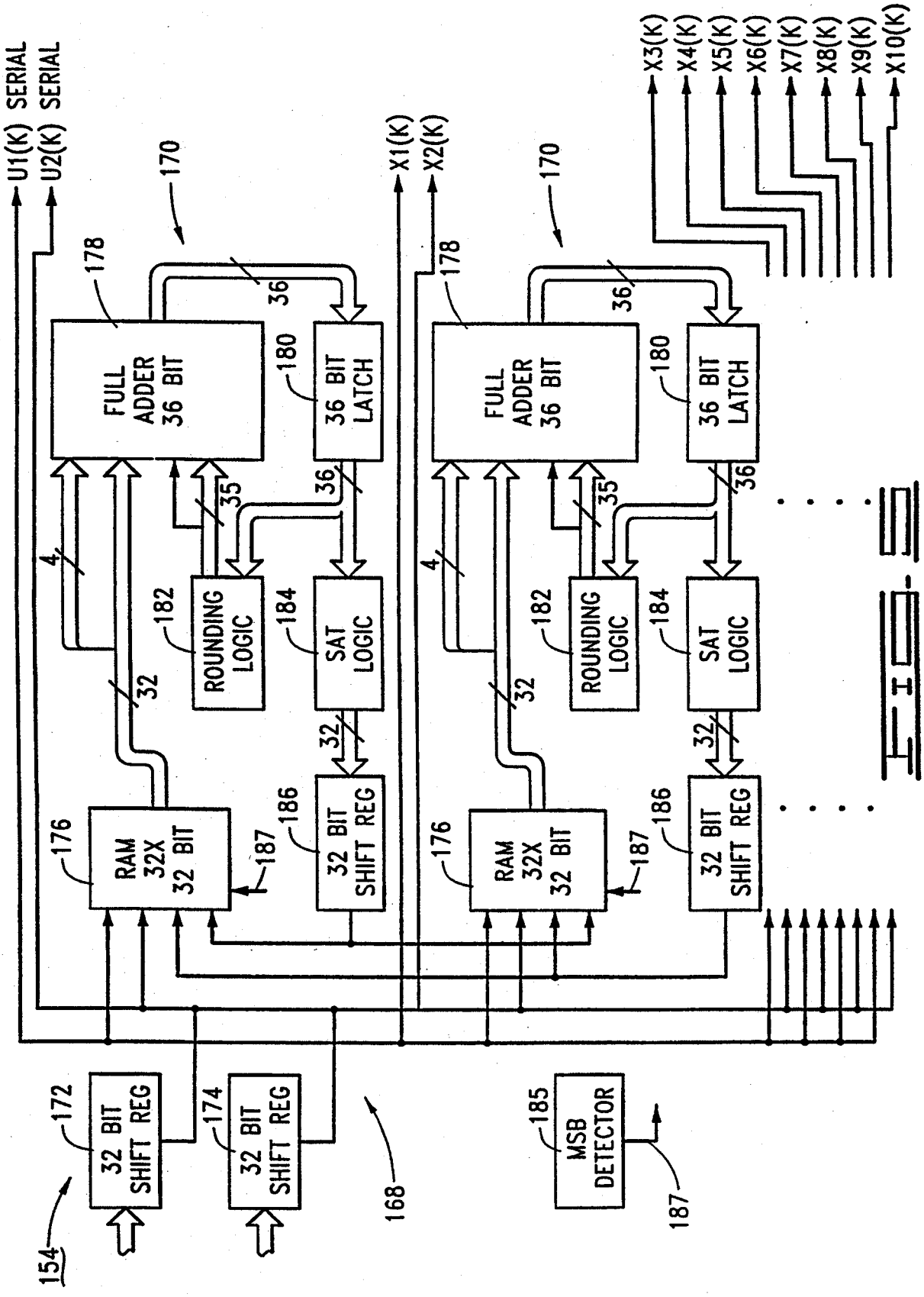


$$A_C = \begin{vmatrix} \alpha_1 & -\alpha_3 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \alpha_3 & \alpha_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \alpha_4 & -\alpha_6 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \alpha_6 & \alpha_5 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \alpha_7 & -\alpha_9 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \alpha_9 & \alpha_8 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \alpha_{10} & -\alpha_{12} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \alpha_{12} & \alpha_{11} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \alpha_{13} & -\alpha_{15} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \alpha_{15} & \alpha_{14} \end{vmatrix}$$

$$B_C = \begin{vmatrix} \beta_1 & \beta_2 \\ \beta_1 & \beta_2 \\ \beta_1 & \beta_2 \\ \beta_1 & \beta_2 \\ \beta_1 & \beta_2 \\ \beta_1 & \beta_2 \\ \beta_1 & \beta_2 \\ \beta_1 & \beta_2 \\ \beta_1 & \beta_2 \\ \beta_1 & \beta_2 \end{vmatrix}$$

$$C_C = \begin{vmatrix} \delta_1 & \delta_3 & \delta_5 & \delta_7 & \delta_9 & \delta_{11} & \delta_{13} & \delta_{15} & \delta_{17} & \delta_{19} \\ \delta_2 & \delta_4 & \delta_6 & \delta_8 & \delta_{10} & \delta_{12} & \delta_{14} & \delta_{16} & \delta_{18} & \delta_{20} \end{vmatrix}$$

$$D_C = \begin{vmatrix} \delta_1 & \delta_3 \\ \delta_2 & \delta_4 \end{vmatrix}$$


U1(K) SERIAL
U2(K) SERIAL
X1(K)
X2(K)
X3(K)
X4(K)
X5(K)
X6(K)
X7(K)
X8(K)
X9(K)
X10(K)
170
178
FULL ADDER 36 BIT
180
36 BIT LATCH
182
ROUNDING LOGIC
184
SAT LOGIC
176
RAM 32X 32 BIT
186
32 BIT SHIFT REG
187
172
32 BIT SHIFT REG
174
32 BIT SHIFT REG
185
MSB DETECTOR
168
154
36
35
32
4

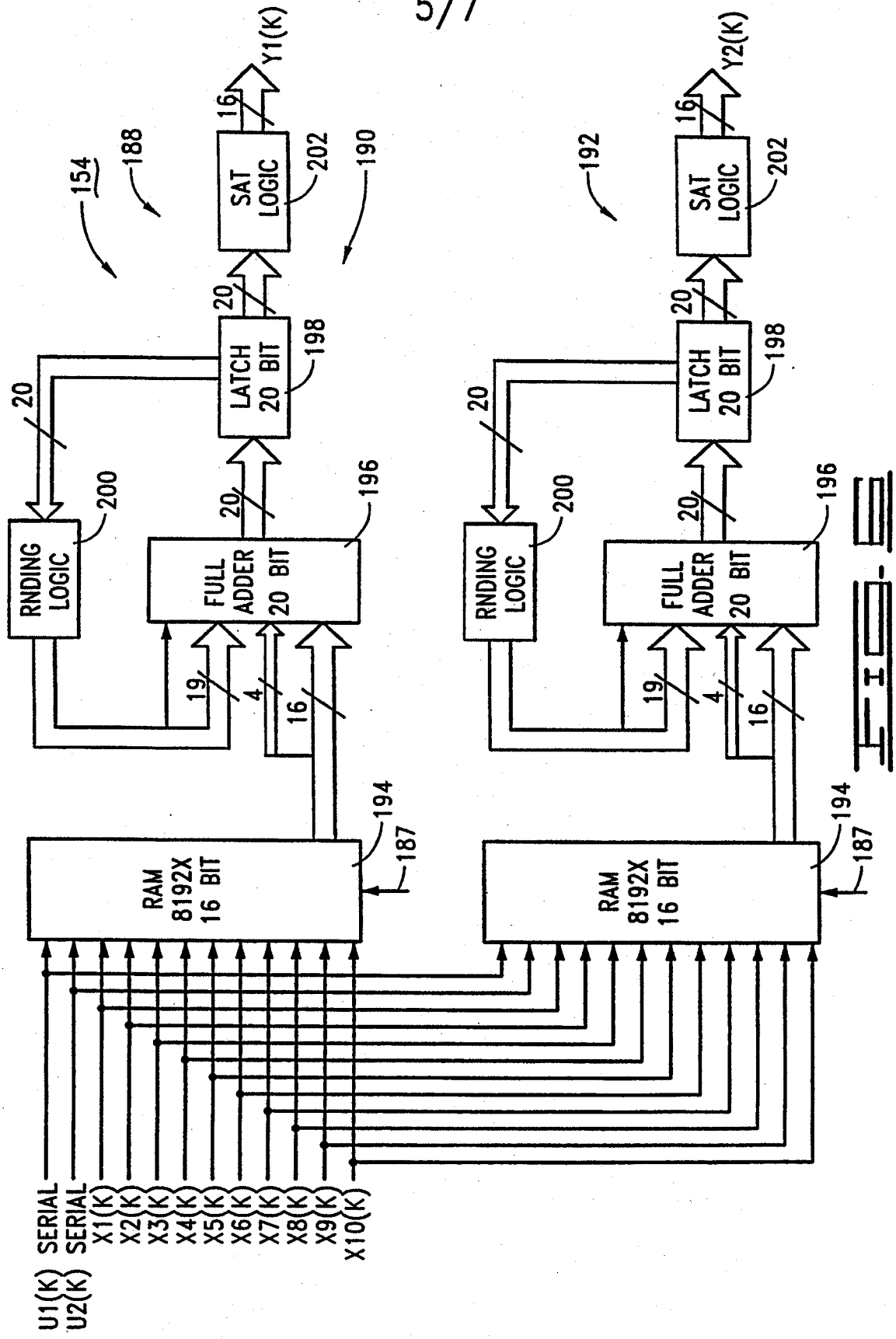

U1(K)
U2(K)
SERIAL
SERIAL
X1(K)
X2(K)
X3(K)
X4(K)
X5(K)
X6(K)
X7(K)
X8(K)
X9(K)
X10(K)
RAM 8192X 16 BIT
187
194
RNDING LOGIC
200
FULL ADDER 20 BIT
196
LATCH 20 BIT
198
SAT LOGIC
202
Y1(K)
Y2(K)
154
188
190
192
20
19
4
16

FIG. 5

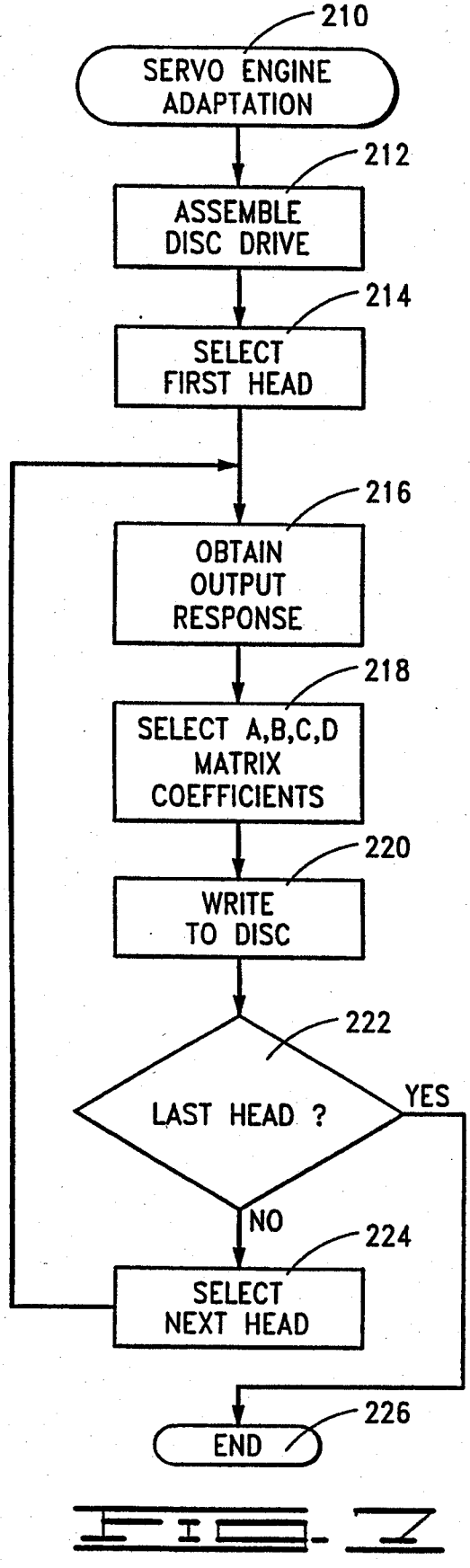

210
SERVO ENGINE ADAPTATION
212
ASSEMBLE DISC DRIVE
214
SELECT FIRST HEAD
216
OBTAIN OUTPUT RESPONSE
218
SELECT A,B,C,D MATRIX COEFFICIENTS
220
WRITE TO DISC
222
LAST HEAD ?
YES
NO
224
SELECT NEXT HEAD
226
END

FIG. 7

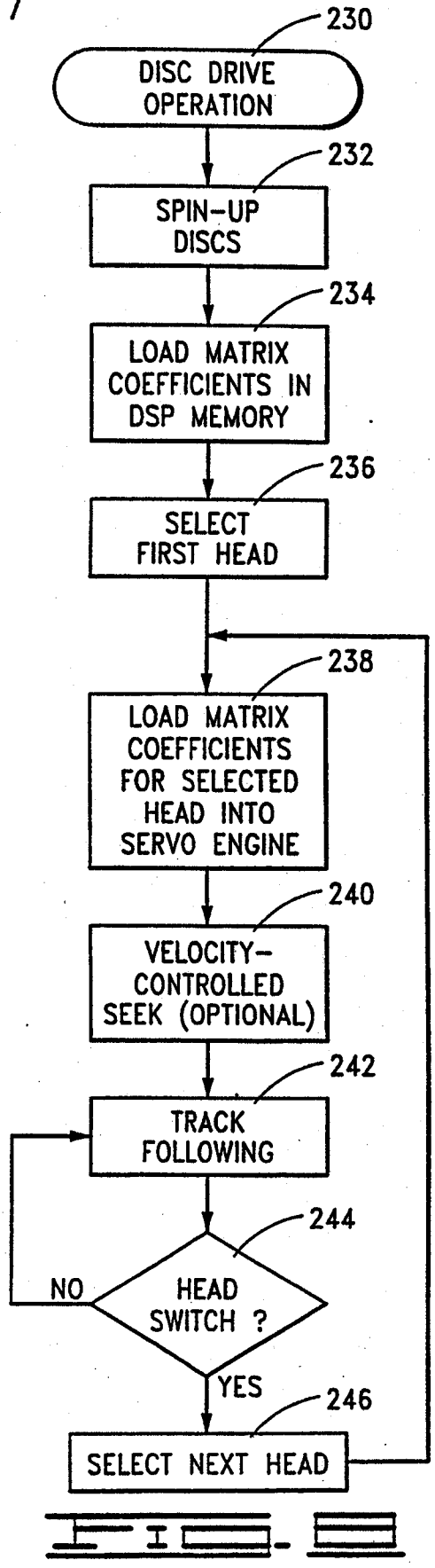
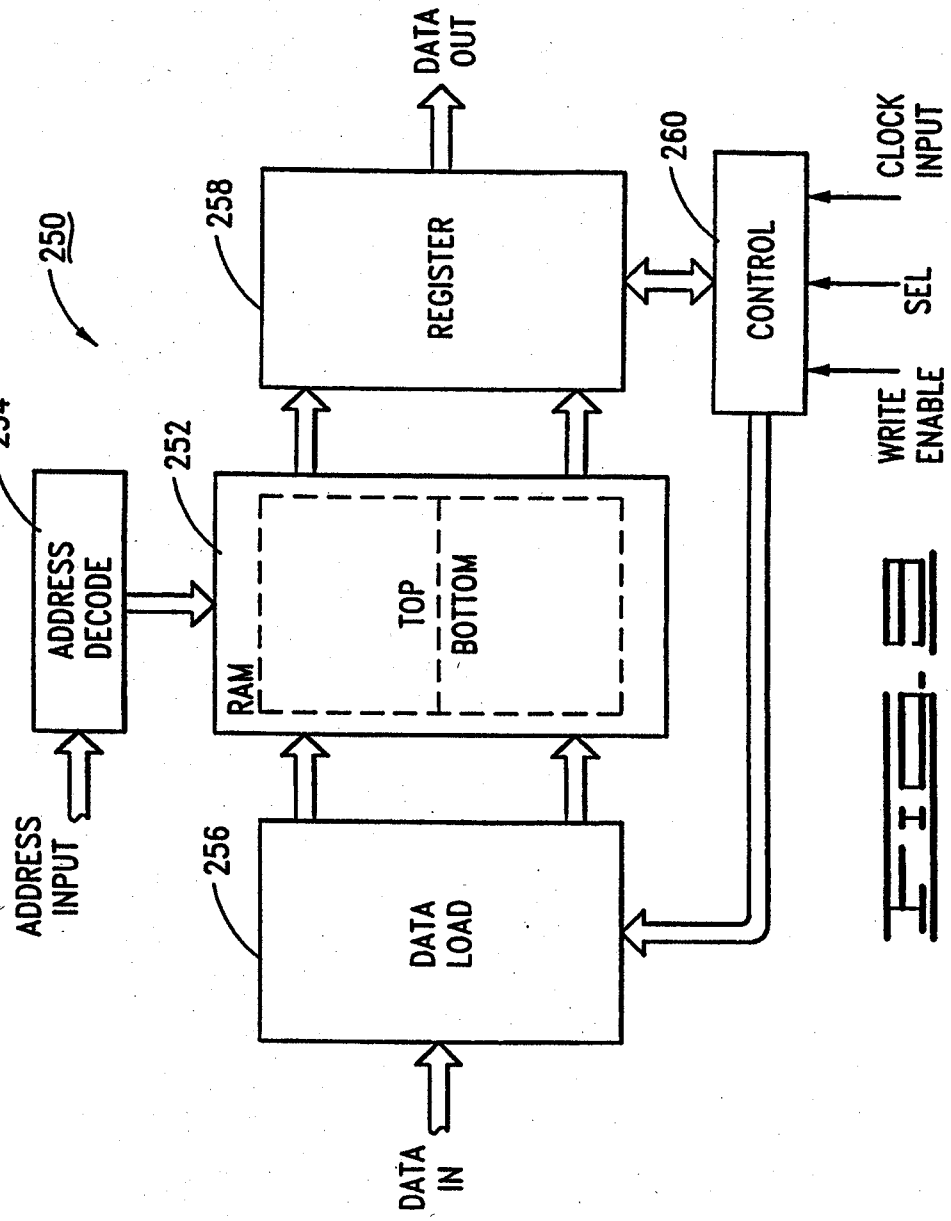

230
DISC DRIVE OPERATION
232
SPIN-UP DISCS
234
LOAD MATRIX COEFFICIENTS IN DSP MEMORY
236
SELECT FIRST HEAD
238
LOAD MATRIX COEFFICIENTS FOR SELECTED HEAD INTO SERVO ENGINE
240
VELOCITY-CONTROLLED SEEK (OPTIONAL)
242
TRACK FOLLOWING
244
HEAD SWITCH ?
NO
YES
246
SELECT NEXT HEAD

FIG. 8


250
254
ADDRESS DECODE
ADDRESS INPUT
252
RAM
TOP
BOTTOM
258
REGISTER
DATA OUT
260
CONTROL
CLOCK INPUT
SEL
WRITE ENABLE
256
DATA LOAD
DATA IN
I/O