CLAIMS

1. A complementary metal-oxide-semiconductor (CMOS) circuit, comprising:

an isolation region on a support substrate that separates a first back gate from a second back gate;

a gate dielectric layer on a first channel region and a second channel region;

a shared conductive gate layer having a work function value on the gate dielectric layer over the first channel region and the second channel region; and

a shared ferroelectric layer on the gate dielectric layer, wherein the first back gate can adjust a threshold voltage for the first channel region, and the second back gate can adjust a threshold voltage for the second channel region.

2. The circuit of claim 1, further comprising a first dielectric layer between the support substrate and the first back gate and between the support substrate and the second back gate.

3. The circuit of claim 1, further comprising a first pair of source/drains on opposite sides of the first channel region.

4. The circuit of claim 3, further comprising a second pair of source/drains on opposite sides of the second channel region.

5. The circuit of claim 4, wherein the first pair of source/drains are n-doped, and the second pair of source/drains are p-doped.

6. The circuit of claim 5, wherein the conductive gate layer has a predetermined work function value in a range of 4.3 to 4.9 eV.

7. The circuit of claim 1, wherein the ferroelectric layer is a ferroelectric material selected from the group consisting of hafnium oxide (HfO), zirconium oxide (ZrO), hafnium zirconium oxide (HZO), hafnium silicon oxide ($HfSiO_x$), barium titanate (BaTiO), potassium niobate (KNbO), bismuth titanate (BiTiO), and combinations thereof.

8. The circuit of claim 7, further comprising a bridging contact on one of the first pair of source/drains on opposite sides of the first channel region and on one of the second pair of source/drains on opposite sides of the second channel region, wherein the bridging contact forms an electrical connection between the one of the first pair of source/drains and the one of the second pair of source/drains to form the complementary metal oxide semiconductor (CMOS) circuit.

9. A complementary metal-oxide-semiconductor (CMOS) circuit, comprising:

a first dielectric layer between a support substrate and a first back gate;

a gate dielectric layer on a first channel region over the first back gate and a second channel region;

a first pair of source/drains on opposite sides of the first channel region;

a shared conductive gate layer having a work function value on the gate dielectric layer over the first channel region and the second channel region; and

a shared ferroelectric layer on the conductive gate layer, wherein the first back gate can adjust a threshold voltage for the first channel region.

10. The circuit of claim 9, further comprising a second back gate on the first dielectric layer, with the second channel region over the second back gate, wherein the second back gate can adjust a threshold voltage for the second channel region.

11. The circuit of claim 10, further comprising a second pair of source/drains on opposite sides of the second channel region, wherein the first pair of source/drains are n-doped, and the second pair of source/drains are p-doped.

12. The circuit of claim 11, further comprising an isolation region on the support substrate that separates the first back gate from the second back gate and separates the first channel region from the second channel region.

13. The circuit of claim 12, wherein the gate dielectric layer is across a top surface of the isolation region.

14. The circuit of claim 13, wherein the conductive gate layer has a predetermined work function value in a range of 4.3 to 4.9 eV on both the first channel region and the second channel region.

15. The circuit of claim 13, further comprising a bridging contact on one of the first pair of source/drains on opposite sides of the first channel region and on one of the second pair of source/drains on opposite sides of the second channel region, wherein the bridging contact forms an electrical connection between the one of the first pair of source/drains and the one of the second pair of source/drains to form the complementary metal oxide semiconductor (CMOS) circuit.

16. A method of fabricating a field effect transistor (FET) device, comprising:

forming a first back gate and a second back gate between a first dielectric layer and a second dielectric layer on a support substrate;

forming a first pair of source/drains on opposite sides of a first channel region, wherein the first channel region is above the first back gate;

forming a second pair of source/drains on opposite sides of a second channel region, wherein the second channel region is above the second back gate;

forming a gate dielectric layer on the first channel region and the second channel region;

forming a conductive gate layer having a work function value on the gate dielectric layer; and

forming a ferroelectric layer on the conductive gate layer.

17. The method of claim 16, further comprising forming a conductive gate electrode layer on the ferroelectric layer, wherein the ferroelectric layer has a range of negative capacitance.

18. The method of claim 17, wherein the conductive gate layer is a work function material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), cobalt (Co), molybdenum (Mo), titanium aluminum (TiAl), titanium nitride (TiN), titanium carbide (TiC), tantalum nitride (TaN), tantalum carbide (TaC), tungsten nitride (WN), titanium aluminum nitride (TiAlN), and combinations thereof.

19. The method of claim 16, further comprising forming a first back gate contact to the first back gate and a second back gate contact to the second back gate,

20. The method of claim 19, further comprising forming a bridging contact on one of the first pair of source/drains on opposite sides of the first channel region and on one of the second pair of source/drains on opposite sides of the second channel region, wherein the bridging contact forms an electrical connection between the one of the first pair of source/drains and the one of the second pair of source/drains to form the complementary metal oxide semiconductor (CMOS) circuit.