

MEMORY FORMING METHOD AND MEMORY

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Chinese Patent Application No. 202010575406.8, filed on June 22, 2020 and entitled “Memory Forming Method and Memory”, the contents of which are hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] The disclosure relates to the technical field of semiconductors, and particularly to a method for forming a memory and a memory.

BACKGROUND

[0003] With the constant decrease of a feature size and line width of a Dynamic Random Access Memory (DRAM), a distance between adjacent bit line structures also constantly decreases. Decrease of the distance between the adjacent bit line structures may cause constant increase of parasitic capacitance between the adjacent bit line structures, affect a saturation current of an array area of the DRAM, and further affect the running efficiency of the DRAM.

[0004] When a line width of a DRAM constantly decreases, how to increase a distance between bit line structures is a problem urgent to be solved at present.

SUMMARY

[0005] Part of examples of the disclosure are intended to provide a method for forming a memory and a memory. Conducting layers in bit line structures are formed at

different heights to increase distances between the conducting layers in the bit line structures without changing an arrangement manner for the bit line structures.

[0006] The examples of the disclosure provide a method for forming a memory, which may include that: a substrate in which at least word line structures and active regions are included, as well as a bottom dielectric layer and bit line contact layers that are on a top surface of the substrate, is provided, bit line contact openings being provided in the bottom dielectric layer, the bit line contact openings exposing the active regions in the substrate, and the bit line contact layers covering the bottom dielectric layer and filling the bit line contact openings; part of the bit line contact layers are etched to form bit line contact layers at different heights; conducting layers are formed on top surfaces of the bit line contact layers, top surfaces of the conducting layers being at different heights in a direction perpendicular to an extension direction of the word line structure, and the top surfaces of the conducting layers being at different heights in the extension direction of the word line structure; top dielectric layers are formed on the top surfaces of the conducting layers; and part of the top dielectric layers, the conducting layers and the bit line contact layers are etched sequentially to form separate bit line structures.

[0007] In addition, the operation that part of the bit line contact layers are etched to form the bit line contact layers at different heights may include that: first photolithographic mask layers are formed on the top surfaces of the bit line contact layers; the first photolithographic mask layers are patterned to form spaced patterns in a preset direction, the preset direction forming an included angle α with the extension direction of the word line structure, and a range of α being $0 < \alpha < 90^\circ$; part of the bit line contact layers are etched based on the spaced patterns to form the bit line contact layers at different heights; and the spaced patterns are removed.

[0008] In addition, the spaced patterns may include spaced and extending strips, or separate ellipses or rectangles.

[0009] In addition, the operation that part of the bit line contact layers are etched to form the bit line contact layers at different heights may include that: second photolithographic mask layers are formed on the top surfaces of the bit line contact layers, the second photolithographic mask layers being in the extension direction of the word

line structure, there being gaps between adjacent second photolithographic mask layers in the direction perpendicular to the extension direction of the word line structure, and spaces between at least two columns of word line structures being comprised in the substrate at bottoms of the bit line contact layers exposed from the gaps; part of the bit line contact layers are etched based on the gaps to form the bit line contact layers at different heights; and the second photolithographic layers are removed.

[0010] In addition, the operation that the conducting layers are formed on the top surfaces of the bit line contact layers may include that: conducting films are formed on the top surfaces of the bit line contact layers; and the conducting films are etched to form the conducting layers with the same thickness on the top surfaces of the bit line contact layers at different heights. The conducting layers with the same thickness are formed to ensure that the conducting layers on the top surfaces of the bit line contact layers at different heights are at different heights.

[0011] In addition, the operation that the top dielectric layers are formed on the top surfaces of the conducting layers may include that: top dielectric films are formed on the top surfaces of the conducting layers; and top surfaces of the top dielectric films are planarized to form the top dielectric layers, top surfaces of the top dielectric layers being at a same height.

[0012] In addition, the bit line contact layer filling the bit line contact opening and covering the bottom dielectric layer may include: a first bit line contact layer fill the bit line contact opening is formed, the first bit line contact layer covering the bottom dielectric layer; a barrier layer is formed on a top surface of the first bit line contact layer at a top of the bottom dielectric layer; and a second bit line contact layer is formed on a top surface of the barrier layer and the top surface of the first bit line contact layer, the second bit line contact layer covering the first bit line contact layer and the barrier layer. The barrier layers are formed in the bit line contact layers in a manner that the conducting layers formed by etching in the bit line structures at the top of the bottom dielectric layer are at the same height as the barrier layers, so that height differences between the conducting layers in different bit line structures are reduced, a connecting line of the conducting layers is waved, and furthermore, the structural stability of the

memory is improved.

[0013] The examples of the disclosure also provide a memory, which may include: a substrate, in which at least word line structures and active regions being included; a bottom dielectric layer, the bottom dielectric layer being at a top of the substrate, bit line contact openings being provided in the bottom dielectric layer, and the bit line contact openings exposing the active regions in the substrate; and separate bit line structures, top surfaces of the bit line structures being at the same height, and the bit line structure including a bit line contact layer at a top of the bottom dielectric layer and in the bit line contact opening, a conducting layer at a top of the bit line contact layer, and a top dielectric layer at a top of the conducting layer. The conducting layers in the same bit line structure may be at different heights in an extension direction of the bit line structure, and the conducting layers in adjacent bit line structures may be at different heights in an extension direction of the word line structure.

[0014] In addition, a connecting line of the conducting layers may be waved in the extension direction of the bit line structure. Height differences of the conducting layers in different bit line structures are reduced to improve the structural stability of the memory.

[0015] In addition, the conducting layers in different bit line structures may be at the same height in a preset direction, the preset direction forming an included angle α with the extension direction of the word line structure, and a range of α being $0 < \alpha < 90^\circ$.

[0016] Compared with the related art, the examples of the disclosure have the following advantages. The bit line contact layers at different heights are formed to make the conducting layers formed on the top surfaces of the bit line contact layers at different heights. The top surfaces of the conducting layers are at the same height in the direction perpendicular to the extension direction of the word line structure, and the top surfaces of the conducting layers are at different heights in the extension direction of the word line structure. That is, in the separate bit line structures that are subsequently formed, the conducting layers in the same bit line structure are at different heights, and the conducting layers in different bit line structures are at different heights. The conducting layers in adjacent separate bit line structures are formed at different heights without changing an arrangement manner for the bit line structures, and compared with the

conducting layers at the same height, distances between the conducting layers at different heights change from horizontal distances to oblique distances, so that the distances between the conducting layers in the bit line structures are increased, furthermore, the parasitic capacitance between the bit line structures is reduced, and a saturation current of the memory is increased. In addition, the method for forming a memory provided in the examples is simple in flow, relatively low in cost, and easy to implement.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0017] Exemplary descriptions are made to one or more examples through the pictures in the corresponding accompanying drawings. Unless otherwise specified, the pictures in the accompanying drawings do not form scale limits.
- [0018] FIG. 1 to FIG. 12 illustrate structure diagrams corresponding to each step of a method for forming a memory according to a first example of the disclosure.
- [0019] FIG. 13 illustrates a schematic section view of a memory formed according to the first example of the disclosure.
- [0020] FIG. 14 illustrates a structure diagram corresponding to another patterning manner in a method for forming a memory according to a second example of the disclosure.
- [0021] FIG. 15 illustrates a schematic section view of a memory formed according to the second example of the disclosure.

DETAILED DESCRIPTION

- [0022] At present, with the constant decrease of a feature size and line width of a DRAM, a distance between adjacent bit line structures also constantly decreases. Decrease of the distance between the adjacent bit line structures may cause constant increase of parasitic capacitance between the adjacent bit line structures, affect a

saturation current of an array area of the DRAM, and further affect the running efficiency of the DRAM.

[0023] For making the objectives, technical solutions and advantages of the disclosure clearer, part of examples of the disclosure will further be described below in detail in combination with the drawings and the examples. It should be understood that specific examples described here are only adopted to explain the disclosure and not intended to limit the disclosure.

[0024] A first example of the disclosure relates to a method for forming a memory, which includes the following operations. A substrate is provided. At least word line structures and active regions are included in the substrate, a bottom dielectric layer and bit line contact layers are provided on a top surface of the substrate, bit line contact openings are formed in the bottom dielectric layer, the bit line contact openings expose the active regions in the substrate, and the bit line contact layers cover the bottom dielectric layer and fill the bit line contact openings. Part of the bit line contact layers are etched to form bit line contact layers at different heights. Conducting layers are formed on top surfaces of the bit line contact layers. Top surfaces of the conducting layers are at different heights in a direction perpendicular to an extension direction of the word line structure, and the top surfaces of the conducting layers are at different heights in the extension direction of the word line structure. Top dielectric layers are formed on the top surfaces of the conducting layers. Part of the top dielectric layers, the conducting layers and the bit line contact layers are etched to form separate bit line structures.

[0025] FIG. 1 to FIG. 12 illustrate structure diagrams corresponding to each step of a method for forming a memory according to a first example of the disclosure. The method for forming a memory of the example will be specifically described below.

[0026] Referring to FIG. 1 to FIG. 5, a substrate 100 is provided. At least word line structures 102 and active regions 101 are included in the substrate 100, a bottom dielectric layer 110 and bit line contact layers 120 are provided on a top surface of the substrate 100, bit line contact openings 111 are provided in the dielectric layer, the bit line contact openings 111 expose the active regions 101 in the substrate 100, and the bit line contact layers 120 cover the bottom dielectric layer 110 and fill the bit line contact

openings 111.

[0027] FIG. 1 to FIG. 5 will be described below in detail in combination with the drawings.

[0028] Referring to FIG. 1, the substrate 100 is provided. At least the word line structures 102 and the active regions 101 are included in the substrate 100.

[0029] FIG. 1 shows an extension direction 10 of the word line structure, i.e., the dotted line 10 in the figure.

[0030] Multiple active regions 101 are spaced in parallel. The active regions 101 of an i^{th} column and the active regions 101 of an $(i+3)^{\text{th}}$ column are at the same horizontal position in a direction perpendicular to the extension direction 10 of the word line structure. The active regions 101 of the i^{th} column and the active regions 101 of adjacent columns (the $(i+1)^{\text{th}}$ column and an $(i-1)^{\text{th}}$ column) are at different horizontal positions in the direction perpendicular to the extension direction 10 of the word line structure. Bit line contact points are formed at middle portions of the active regions 101 spaced by the alternately arranged word line structures 102, and are used to connect bit line structures that are subsequently formed.

[0031] It is to be noted that other memory structures, except the word line structures 102 and the active regions 101, are also included in the substrate 100, such as shallow trench isolation structures, etc. The other memory structures do not involve the core technology of the disclosure, and will not be elaborated herein. Those skilled in the art can understand that the other memory structures for normal running of the memory, except the word line structures 102 and the active regions 101, may also be included in the substrate 100.

[0032] A material for the substrate 100 may include sapphire, silicon, silicon carbide, gallium arsenide, aluminum nitride, zinc oxide, etc. In the example, the substrate 100 is formed from silicon. Those skilled in the art knows that silicon is used as the substrate 100 in the example for a purpose of making it convenient for those skilled in the art to understand the subsequent forming method, no limits are formed, and a suitable material may be selected as the substrate as required in a practical application process.

- [0033] Referring to FIG. 2 to FIG. 5, the bottom dielectric layer 110 and the bit line contact layers 120 are formed on the top surface of the substrate 100, the bit line contact openings 111 are provided in the bottom dielectric layer 110, the bit line contact openings 111 expose the active regions 101 in the substrate 100, and the bit line contact layers 120 cover the bottom dielectric layer 110 and fill the bit line contact openings 111.
- [0034] Referring to FIG. 2, the bottom dielectric layer 110 is formed on the top surface of the substrate 100, the bit line contact openings 111 are provided in the bottom dielectric layer 110, and the bit line contact openings 111 are formed to expose the active regions 101 in the substrate 100. Specifically, the bit line contact openings 111 are formed to expose bit line contact points, namely exposing middle portions of the active regions 101 spaced by the word line structures 102.
- [0035] The bottom dielectric layer 110 is used to isolate the bit line structures 200 not at the bit line contact points from contacting the active regions 101. In the example, a material for the bottom dielectric layer is silicon nitride. In another example, the material for the bottom dielectric layer may also be an insulating material such as silicon oxide or silicon oxynitride.
- [0036] Referring to FIG. 3, FIG. 3 illustrates a top view of the substrate 100. FIG. 3 presents positions where the bit line structures 200 are required to be subsequently formed based on formation of the bottom dielectric layer in FIG. 2. FIG. 3 shows an extension direction 20 of the bit line structure, i.e., the dotted line 20 in the figure. The bit line structure 200 is connected with the bit line contact points of the active regions 101 of a column.
- [0037] Referring to FIG. 4, the bit line contact layers 120 are formed on the top surface of the substrate 100, and the bit line contact layers 120 cover the bottom dielectric layer 120 and fill the bit line contact openings 111. FIG. 4 presents positions where the bit line structures are required to be subsequently formed. In any section in the extension direction 10 of the word line structure, bit lines connected with the active regions 101 and bit lines on the bottom dielectric layer 110 are alternately arranged.
- [0038] In the example, the bit line contact layer 120 includes a first bit line contact

layer 122 and a second bit line contact layer 123. Specifically, the first bit line contact layer 122 filling the bit line contact opening 111 is formed, the first bit line contact layer 122 covering the bottom dielectric layer 110. A barrier layer 124 is formed on a top surface of the first bit line contact layer 122 at a top of the bottom dielectric layer 110. The second bit line contact layer 123 is formed on a top surface of the barrier layer 124 and the top surface of the first bit line contact layer 122, the second bit line contact layer 123 covering the first bit line contact layer 122 and the barrier layer 124. The barrier layers 124 are formed in the bit line contact layers 120 in a manner that the conducting layers subsequently formed by etching in the bit line structures at the top of the bottom dielectric layer are at the same height as the barrier layers, so that height differences between the conducting layers in different bit line structures are reduced, a connecting line of the conducting layers is waved, and furthermore, the structural stability of the formed memory is improved.

[0039] In the example, a material for the barrier layer 124 is the same as that for the bottom dielectric layer 110. In another example, it is only necessary to ensure that the material for the barrier layer is different from a material for the bit line contact layer to ensure that the barrier layers are etched when the bit line contact layers are etched. In addition, in the example, both the first bit line contact layer 122 and the second bit line contact layer 123 use a polysilicon material, and are used to connect the subsequently formed bit line structures 200 with the active regions 101 in the substrate through the bit line contact openings 111.

[0040] It is to be noted that, in another example, the bit line contact layer 120 may also be formed by a single-layer structure. The specific layer number of the bit line contact layer 120 is not limited in the example. Those skilled in the art can know that the multilayer structure solution provided in the abovementioned example is intended to ensure that height differences between the subsequently formed conducting layers at different heights are relatively small and the connecting line of the conducting layers is waved to improve the stability of the memory.

[0041] Referring to FIG. 5 to FIG. 8, part of the bit line contact layers 120 are etched to form bit line contact layers 121 at different heights.

[0042] A reason for forming the bit line contact layers 121 at different heights includes that the bit line contact layers 121 are used to ensure that the conducting layers are at different heights after the conducting layers are subsequently formed.

[0043] Specifically, referring to FIG. 5, a first photolithographic mask layer 130 is formed on top surface of the bit line contact layer 120, and a photoresist 140 is formed on a top surface of the first photolithographic mask layer 130.

[0044] Referring to FIG. 6, the first photolithographic mask layers 130 are patterned to form spaced patterns 131 in a preset direction. The spaced patterns 131 include spaced and extending strips, or separate ellipses or rectangles.

[0045] The first photolithographic mask layer 130 is patterned based on the photoresist. Referring to FIG. 7, the first photolithographic mask layers 130 are patterned to form the spaced patterns 131 in the preset direction, the preset direction forming an included angle α with the extension direction 10 of the word line structure, and a range of α being $0 < \alpha < 90^\circ$ (the included angle α between straight lines refers to an included angle between a straight line 40 and the straight line 10, and if it is an included angle of rays, the range of α is $0 < \alpha < 360^\circ$, $\alpha \neq 90^\circ$, $\alpha \neq 180^\circ$, and $\alpha \neq 270^\circ$). The example is illustrated with the condition that α is 25° as an instance. In another example, α may be 10° , 20° , 30° , 40° , 50° , 60° , 70° , 80° , etc. In the figure, the circles 401 represent the line bit contact points covered by the spaced patterns 131. It can be seen by those skilled in the art that the bit line contact points covered by the spaced patterns 131 and the bit line contact points not covered by the spaced patterns 131 are alternately arranged in sectional directions of the dotted line 30 and the dotted line 31.

[0046] It is to be noted that, in the example, the spaced patterns 131 are exemplarily described with spaced and extending strips as an instance. In another example, the spaced patterns 131 may also be separate ellipses or rectangles.

[0047] Referring to FIG. 8, part of the bit line contact layers 120 are etched based on the spaced patterns 131 to form the bit line contact layers 121 at different heights.

[0048] Referring to FIG. 9, the spaced patterns 131 and the barrier layers 124 are removed.

[0049] In the figure, the direction of the dotted line 30 and the direction of the dotted line 31 are two sectional positions presented in FIG. 3, and are used for those skilled in the art to understand the principle of the disclosure.

[0050] FIG. 9 illustrates a schematic section view in the direction of the dotted line 30 and the direction of the dotted line 31. In the direction perpendicular to the extension direction 10 of the word line structure (the same vertical position in the two figures), the bit line contact layers 121 are at different heights. In the extension direction 10 of the word line structure (the shown sectional direction), the bit line contact layers 121 are at different heights, and protruding portions at a first height and sunken portions at a second height in the bit line contact layers 121 at the bit line contact openings 111 are alternately arranged.

[0051] In another example, masks may further be continued to be formed. The bit line contact layers at different heights are further etched to ensure that heights of the top surfaces of the left bit line contact layers may be alternately arranged according to a preset height sequence.

[0052] Referring to FIG. 10 to FIG. 11, conducting layers 140 are formed on the top surfaces of the bit line contact layers 121 at different heights.

[0053] Specifically, referring to FIG. 10, conducting films 141 are formed on the top surfaces of the bit line contact layers 121 at different heights.

[0054] Referring to FIG. 11, the conducting films 141 are etched (referring to FIG. 10) to form the conducting layers 140 with the same thickness on the top surfaces of the bit line contact layers 121 at different heights. The conducting layers 140 with the same thickness are formed to ensure that the conducting layers 140 on the top surfaces of the bit line contact layers 121 at different heights are at different heights.

[0055] In another example, the conducting layers on the top surfaces of the bit line contact layers at different heights may have different thicknesses, but it is necessary to ensure that the top surfaces of the conducting layers are at different heights, so that the connecting line of the conducting layers between different bit line structures is an oblique line, and distances between the conducting layers of the bit line structures are increased

without changing an arrangement manner for the bit line structures.

[0056] In the direction perpendicular to the extension direction 10 of the word line structure, the top surfaces of the formed conducting layers 140 are at different heights, and the connecting line is waved. In the extension direction 10 of the word line structure, the top surfaces are at different heights, and the connecting line is waved.

[0057] In the example, the conducting layer 140 is formed from one conducting material or more conducting materials, for example, doped with polysilicon, titanium, titanium nitride, tungsten, and a composite of tungsten.

[0058] Referring to FIG. 12, top dielectric layers 150 are formed on top surfaces of the conducting layers 140.

[0059] Specifically, top dielectric films are formed on the top surfaces of the conducting layers, and surfaces of the top dielectric films are planarized to form the top dielectric layers 150, top surfaces of the top dielectric layers 150 being at a same height.

[0060] Specifically, the top surfaces of the top dielectric films are planarized in a chemical mechanical polishing manner. Compared with an etching process, a chemical mechanical polishing process is higher in removal rate and favorable for shortening the process cycle.

[0061] In the example, a material for the top dielectric layer 150 includes silicon nitride, silicon oxynitride, silicon oxide, etc. In the example, the material for the top dielectric layer 150 is a nitrogen-containing insulating material, namely silicon nitride is used for the top dielectric layer 150.

[0062] Referring to FIG. 13, part of the top dielectric layers 150, the conducting layers 140 and the bit line contact layers 121 at different heights are sequentially etched to form separate bit line structures 200.

[0063] In the direction perpendicular to the extension direction 10 of the word line structure, the connecting line of the conducting layers 140 in the separate bit line structures 200 is waved. In the extension direction 10 of the word line structure, the

conducting layers 140 in adjacent separate bit line structures 200 are at different heights, and the connecting line of the conducting layers 140 is waved.

[0064] Compared with the related art, the method for forming a memory provided in the examples of the disclosure has the following advantages. The bit line contact layers at different heights are formed to make the conducting layers formed on the top surfaces of the bit line contact layers at different heights. The top surfaces of the conducting layers are at the same height in the direction perpendicular to the extension direction of the word line structure, and the top surfaces of the conducting layers are at different heights in the extension direction of the word line structure. That is, in the separate bit line structures that are subsequently formed, the conducting layers in the same bit line structure are at different heights, and the conducting layers in different bit line structures are at different heights. The conducting layers in adjacent separate bit line structures are formed at different heights without changing an arrangement manner for the bit line structures, and compared with the conducting layers at the same height, distances between the conducting layers at different heights change from horizontal distances to oblique distances, so that the distances between the conducting layers in the bit line structures are increased, furthermore, the parasitic capacitance between the bit line structures is reduced, and a saturation current of the memory is increased. In addition, the method for forming a memory provided in the examples is simple in flow, relatively low in cost, and easy to implement.

[0065] The above steps are divided only for clear description. During implementation, the steps can be combined into one step, or some steps may be split into multiple steps, and any solution including the same logical relationship falls within the scope of protection of the disclosure. Adding insignificant modifications to the flow or introducing insignificant designs without changing the core design of the flow falls within the scope of protection of the disclosure.

[0066] A second example of the disclosure relates to a method for forming a memory. The difference from the first example is that the example provides another manner for forming photolithographic masks. Referring to FIG. 14 and FIG. 15, the method for forming a memory of the example will be specifically described below.

[0067] Second photolithographic mask layers are formed on the top surfaces of the bit line contact layers.

[0068] The example provides two manners for forming the second photolithographic mask layers, specifically as follows.

[0069] The first manner for forming second photolithographic mask layers 500: the formed second photolithographic mask layer 500 is in the extension direction 10 of the word line structure, there are gaps formed between adjacent second photolithographic mask layers 500 in the direction perpendicular to the extension direction 10 of the word line structure, and spaces between at least two columns of word line structures 102 are exposed in the substrate at bottoms of the bit line contact layers exposed from the gaps.

[0070] The second manner for forming second photolithographic mask layers 501: the second photolithographic mask layers 501 are formed, the second photolithographic mask layer 501 covering the two bit line contact points 502 in the space between the two columns of word line structures 102, and the second photolithographic mask layers 501 being sequentially arranged in the extension direction 10 of the word line structure.

[0071] In the example, the second manner for forming the second photolithographic mask layers 501 is used, part of the bit line contact layers are etched based on the gaps to form the bit line contact layers at different heights, and then the second photolithographic mask layers are removed. The other process steps are the same as the first example. The bit line structure 200 formed according to the method for forming a mask provided in the example refers to FIG. 15.

[0072] The conducting layers in the bit line structures 200 formed in the bit line contact points covered by the second photolithographic mask layers are relatively high, and the conducting layers in the bit line structures 200 formed in the bit line contact points not covered by the second photolithographic mask layers are relatively low (not shown in the figure). In such case, the conducting layers in the bit line structures 200 on the bit line contact points are at the same height in the direction perpendicular to the extension direction 10 of the word line structure. However, since the barrier layers are formed in the bit line contact layers, the bit line structures on the bottom dielectric layer

110 and the bit line structures on the bit line contact points are at different heights. In such case, in the extension direction 10 of the word line structure, the conducting layers in different bit line structures 200 are at different heights. In the extension direction 20 of the bit line structure, the conducting layers in the same bit line structure 200 are at different heights due to the distribution of the second photolithographic mask layers.

[0073] Compared with the related art, the method for forming a memory provided in the second example of the disclosure has the following advantages. The bit line contact layers at different heights are formed to make the conducting layers formed on the top surfaces of the bit line contact layers at different heights. The top surfaces of the conducting layers are at the same height in the direction perpendicular to the extension direction of the word line structure, and the top surfaces of the conducting layers are at different heights in the extension direction of the word line structure. That is, in the separate bit line structures that are subsequently formed, the conducting layers in the same bit line structure are at different heights, and the conducting layers in different bit line structures are at different heights. The conducting layers in adjacent separate bit line structures are formed at different heights without changing an arrangement manner for the bit line structures, and compared with the conducting layers at the same height, distances between the conducting layers at different heights change from horizontal distances to oblique distances, so that the distances between the conducting layers in the bit line structures are increased, furthermore, the parasitic capacitance between the bit line structures is reduced, and a saturation current of the memory is increased. In addition, the method for forming a memory provided in the examples is simple in flow, relatively low in cost, and easy to implement.

[0074] The first example corresponds to the present example, so that the present example can be matched with the first example for implementation. The related technical details mentioned in the first example are still effective in the present example, and the technical effects that may be achieved in the first example may also be achieved in the present example. For reducing repetitions, elaborations are omitted herein. Correspondingly, related technical details mentioned in the present example may also be applied to the first example.

[0075] A third example of the disclosure relates to a memory.

[0076] Referring to FIG. 13, the memory provided in the example will be described below in detail in combination with the drawing. Parts the same as or corresponding to the first example will not be elaborated below.

[0077] The memory includes: a substrate 100, at least word line structures 102 and active regions 101 being included in the substrate 100; a bottom dielectric layer 110, the bottom dielectric layer 110 being at a top of the substrate 100, bit line contact openings 111 being provided in the bottom dielectric layer 110, and the bit line contact openings 111 exposing the active regions 101 in the substrate 100; and separate bit line structures 200, top surfaces of the bit line structures 200 being at the same height, and the bit line structure 200 including a bit line contact layer 121 at a top of the bottom dielectric layer 110 and in the bit line contact opening 111, a conducting layer 140 at a top of the bit line contact layer 121, and a top dielectric layer 150 at a top of the conducting layer 140. The conducting layers 140 in the same bit line structure are at different heights in an extension direction 20 of the bit line structure, and the conducting layers 140 in adjacent bit line structures are at different heights in an extension direction 10 of the word line structure.

[0078] It is to be noted that other memory structures, except the word line structures 102 and the active regions 101, are also included in the substrate 100, such as shallow trench isolation structures, etc. The other memory structures do not involve the core technology of the disclosure, and will not be elaborated herein. Those skilled in the art can understand that the other memory structures for normal running of the memory, except the word line structures 102 and the active regions 101, may also be included in the substrate 100.

[0079] In the example, the conducting layers 140 have the same thickness. In another example, the conducting layers 140 on the top surfaces of the bit line contact layers 121 at different heights may have different thicknesses, but it is necessary to ensure that the top surfaces of the conducting layers 140 are at different heights, so that the connecting line of the conducting layers between different bit line structures is an oblique line, and distances between the conducting layers of the bit line structures are increased without

changing an arrangement manner for the bit line structures.

[0080] In the example, a connecting line of the conducting layers 140 is waved in the extension direction 20 of the bit line structure, namely the conducting layers 140 in the same bit line structure 200 are at different heights. The conducting layers 140 in different bit line structures 200 are at the same height in a preset direction, the preset direction forming an included angle α with the extension direction 10 of the word line structure, and a range of α being $0 < \alpha < 90^\circ$ (the included angle α between straight lines refers to an included angle between a straight line 40 and the straight line 10, and if it is an included angle of rays, the range of α is $0 < \alpha < 360^\circ$, $\alpha \neq 90^\circ$, $\alpha \neq 180^\circ$, and $\alpha \neq 270^\circ$).

[0081] Compared with the related art, the example has the following advantages. Through the bit line contact layers at different heights, the conducting layers on the top surfaces of the bit line contact layers are at different heights. The top surfaces of the conducting layers are at the same height in the direction perpendicular to the extension direction of the word line structure, and the top surfaces of the conducting layers are at different heights in the extension direction of the word line structure. That is, in the separate bit line structures that are subsequently formed, the conducting layers in the same bit line structure are at different heights, and the conducting layers in different bit line structures are at different heights. The conducting layers in adjacent separate bit line structures are formed at different heights without changing an arrangement manner for the bit line structures, and compared with the conducting layers at the same height, distances between the conducting layers at different heights change from horizontal distances to oblique distances, so that the distances between the conducting layers in the bit line structures are increased, furthermore, the parasitic capacitance between the bit line structures is reduced, and a saturation current of the memory is increased. In addition, the method for forming a memory provided in the examples is simple in flow, relatively low in cost, and easy to implement.

[0082] The first example corresponds to the present example, so that the present example can be matched with the first example for implementation. The related technical details mentioned in the first example are still effective in the present example, and the technical effects that may be achieved in the first example may also be achieved in the

present example. For reducing repetitions, elaborations are omitted herein. Correspondingly, related technical details mentioned in the present example may also be applied to the first example.

[0083] Those of ordinary skill in the art can understand that each example is a specific example implementing the disclosure, and in practical applications, various variations about the form and details can be made thereto without departing from the spirit and scope of the disclosure.

CLAIMS

1. A method for forming a memory, comprising:

providing a substrate, in which at least word line structures and active regions are comprised, as well as a bottom dielectric layer and bit line contact layers that are on a top surface of the substrate, bit line contact openings being provided in the bottom dielectric layer, the bit line contact openings exposing the active regions in the substrate, and the bit line contact layers covering the bottom dielectric layer and filling the bit line contact openings;

etching part of the bit line contact layers to form bit line contact layers at different heights;

forming conducting layers on top surfaces of the bit line contact layers, top surfaces of the conducting layers being at different heights in a direction perpendicular to an extension direction of the word line structure, and the top surfaces of the conducting layers being at different heights in the extension direction of the word line structure;

forming top dielectric layers on the top surfaces of the conducting layers; and

sequentially etching part of the top dielectric layers, the conducting layers and the bit line contact layers to form separate bit line structures.

2. The method for forming a memory of claim 1, wherein etching part of the bit line contact layers to form the bit line contact layers at different heights comprises:

forming first photolithographic mask layers on the top surfaces of the bit line contact layers;

patterning the first photolithographic mask layers to form spaced patterns in a preset direction,

the preset direction forming an included angle α with the extension direction of the

word line structure, and a range of α being $0 < \alpha < 90^\circ$;

etching part of the bit line contact layers based on the spaced patterns to form the bit line contact layers at different heights; and

removing the spaced patterns.

3. The method for forming a memory of claim 2, wherein the spaced patterns comprise spaced and extending strips, or separate ellipses or rectangles.

4. The method for forming a memory of claim 1, wherein etching part of the bit line contact layers to form the bit line contact layers at different heights comprises:

forming second photolithographic mask layers on the top surfaces of the bit line contact layers,

the second photolithographic mask layers being in the extension direction of the word line structure, and there being gaps formed between adjacent second photolithographic mask layers in the direction perpendicular to the extension direction of the word line structure,

wherein spaces between at least two columns of word line structures are comprised in the substrate at bottoms of the bit line contact layers exposed from the gaps;

etching part of the bit line contact layers based on the gaps to form the bit line contact layers at different heights; and

removing the second photolithographic mask layers.

5. The method for forming a memory of claim 1, wherein forming the conducting layers on the top surfaces of the bit line contact layers comprises:

forming conducting films on the top surfaces of the bit line contact layers; and

etching the conducting films to form the conducting layers with a same thickness on the top surfaces of the bit line contact layers at different heights.

6. The method for forming a memory of claim 1, wherein forming the top dielectric layers on the top surfaces of the conducting layers comprises:

forming top dielectric films on the top surfaces of the conducting layers; and

planarizing top surfaces of the top dielectric films to form the top dielectric layers, top surfaces of the top dielectric layers being at a same height.

7. The method for forming a memory of any one of claims 1-6, wherein the bit line contact layer filling the bit line contact opening and covering the bottom dielectric layer comprises:

forming a first bit line contact layer filling the bit line contact opening, the first bit line contact layer covering the bottom dielectric layer;

forming a barrier layer on a top surface of the first bit line contact layer at a top of the bottom dielectric layer; and

forming a second bit line contact layer on a top surface of the barrier layer and the top surface of the first bit line contact layer, the second bit line contact layer covering the first bit line contact layer and the barrier layer.

8. A memory, comprising:

a substrate, at least word line structures and active regions being comprised in the substrate;

a bottom dielectric layer, the bottom dielectric layer being at a top of the substrate, bit line contact openings being provided in the bottom dielectric layer, and the bit line contact

openings exposing the active regions in the substrate; and

separate bit line structures, top surfaces of the bit line structures being at the same height, and the bit line structure comprising a bit line contact layer at a top of the bottom dielectric layer and in the bit line contact opening, a conducting layer at a top of the bit line contact layer, and a top dielectric layer at a top of the conducting layer,

wherein the conducting layers in the same bit line structure are at different heights in an extension direction of the bit line structure, and the conducting layers in adjacent bit line structures are at different heights in an extension direction of the word line structure.

9. The memory of claim 8, wherein a connecting line of the conducting layers is waved in the extension direction of the bit line structure.

10. The memory of claim 8, wherein the conducting layers in different bit line structures are at the same height in a preset direction, the preset direction forming an included angle α with the extension direction of the word line structure, and a range of α being $0 < \alpha < 90^\circ$.