What is claimed is:

1. A method for combining a plurality of downlink signals representative of a communication signal, the method comprising:

receiving samples of the plurality of downlink signals from a plurality of antenna feeds;

generating first symbols for a first signal of the plurality of downlink signals based on performing a first timing recovery operation on first samples of the first signal;

generating second symbols for a second signal of the plurality of downlink signals based on performing a second timing recovery operation on second samples of the second signal;

generating time and phase offset information based on performing a correlator operation on the first and second symbols; and

combining the first signal and the second signal based on (i) the first and second symbols, (ii) aligning timing and phase of the first symbols with the second symbols based on the time and phase offset information, and (iii) performing a weighted combiner operation that applies scaling to each of the first and second data packets based on corresponding signal quality,

wherein at least one of the first timing recovery operation, the second timing recovery operation, the correlator operation, and the combining are performed in a plurality of processing blocks in one or more processors, wherein the first and second processing block operate in parallel.

2. The method of claim 1, wherein the plurality of processing blocks comprises a plurality of central processing unit (CPU) cores.

3. The method of claim 1, wherein the one or more processors comprises a plurality of processors, wherein in a first one or more processing blocks of the plurality of processing blocks are comprised in a first processor of the plurality of processors and a second one or more processing blocks of the plurality of processing blocks are comprised in a second processor of the plurality of processors.

4. The method of claim 1, wherein the one or more processors comprises a single processor comprising a first one or more processing blocks of the plurality of processing blocks and a second one or more processing blocks of the plurality of processing blocks.

5. The method of claim 1, wherein the first timing recovery operation is performed in the plurality of processing blocks, the plurality of processing blocks comprising at least a first processing block and a second processing block, wherein the first processing block performs the first timing recovery operation on a first portion of the first samples and the second processing block performs the first timing recovery operation on a second portion of the first samples, wherein the first and second processing block operate in parallel.

6. The method of claim 1, wherein the plurality of processing blocks comprises:

at least a first processing block that performs at least one of the first timing recovery operation, the second timing recovery operation, the correlator operation, and the combining; and

at least a second processing block that performs the at least one of the first timing recovery operation, the second timing recovery operation, the correlator operation, and the combining, wherein the first and second processing block operate in parallel.

7. The method of claim 1, further comprising:

generating first corrected symbols based on performing a first carrier recovery operation on the first symbols; and

generating second corrected symbols based on performing a second carrier recovery operation on the second symbols.

8. The method of claim 7, wherein the plurality of processing blocks performs the first timing recovery operation and the first carrier recovery operation, wherein the plurality of processing blocks comprises at least:

a first processing block that performs the first timing recovery operation and the first carrier operation on a first portion of the first samples; and

a second processing block that performs the first timing recovery operation and the first carrier operation on a second portion of the first samples.

9. The method of claim 7, wherein the plurality of processing blocks comprises a first one or more processing blocks that performs the first timing recovery operation and first carrier recovery operation and a second one or more processing blocks that performs the second timing recovery operation and second carrier recovery operation.

10. The method of claim 7, wherein

the first timing recovery operation and the first carrier recovery operation are part of a first match filter, and

the second timing recovery operation and the second carrier recovery operation are part of a second match filter.

11. The method of claim 1, further comprising generating corrected symbols based on performing a carrier recovery operation on the combined first and second signals.

12. The method of claim 1, wherein

the first timing recovery operation, the second timing recovery operation, the carrier recovery operation are part of a match filter.

13. The method of claim 1, wherein the one or more processors are one or more general-purpose central processing units (CPU).

14. The method of claim 1, wherein the one or more processors employ single instructions, multiple data (SIMD) techniques to achieve high throughput.

15. A system for combining a plurality of downlink signals representative of a communication signal, the system comprising:

a plurality of antennas configured to receive the plurality of downlink signals; and

one or more processors communicatively coupled to the plurality of antennas, the one or more processors having a plurality of processing blocks and operable to:

receive samples of the plurality of downlink signals from a plurality of antenna feeds;

generate first symbols for a first signal of the plurality of downlink signals based on performing a first timing recovery operation on first samples of the first signal;

generate second symbols for a second signal of the plurality of downlink signals based on performing a second timing recovery operation on second samples of the second signal;

generate time and phase offset information based on performing a correlator operation on the first and second symbols; and

combine the first signal and the second signal based on (i) the first and second symbols, (ii) aligning timing and phase of the first symbols with the second symbols based on the time and phase offset information, and (iii) performing a weighted combiner operation that applies scaling to each of the first and second data packets based on corresponding signal quality,

wherein at least one of the first timing recovery operation, the second timing recovery operation, the correlator operation, and the combining are performed in a plurality of processing blocks in one or more processors, wherein the first and second processing block operate in parallel.

16. The system of claim 15, wherein the plurality of processing blocks comprises a plurality of central processing unit (CPU) cores.

17. The system of claim 15, wherein the one or more processors comprises a plurality of processors, wherein in a first one or more processing blocks of the plurality of processing blocks are comprised in a first processor of the plurality of processors and a second one or more processing blocks of the plurality of processing blocks are comprised in a second processor of the plurality of processors.

18. The system of claim 15, wherein the one or more processors employ single instructions, multiple data (SIMD) techniques to achieve high throughput.

19. An apparatus for combining a plurality of downlink signals representative of a communication signal, the apparatus comprising:

a means for receiving samples of the plurality of downlink signals from a plurality of antenna feeds;

a means for generating first symbols for a first signal of the plurality of downlink signals based on performing a first timing recovery operation on first samples of the first signal;

a means for generating second symbols for a second signal of the plurality of downlink signals based on performing a second timing recovery operation on second samples of the second signal;

a means for generating time and phase offset information based on performing a correlator operation on the first and second symbols; and

a means for combining the first signal and the second signal based on (i) the first and second symbols, (ii) aligning timing and phase of the first symbols with the second symbols based on the time and phase offset information, and (iii) performing a weighted combiner operation that applies scaling to each of the first and second data packets based on corresponding signal quality,

wherein at least one of the means for generating first symbols, the means for generating second symbols, the means for generating time and phase offset information, and the means for combining are performed in a plurality of processing blocks in one or more processors, wherein the first and second processing block operate in parallel.