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TITLE

PROCESS FOR MODIFIED OXIDATION OF A SEMICONDUCTOR SUBSTRATE USING CHLORINE PLASMA

TECHNICAL FIELD

The present invention relates generally to oxidation of semiconductor substrates and, more specifically, to oxidation of silicon, germanium, or a combination thereof during fabrication of semiconductors.

BACKGROUND OF THE INVENTION

At various stages during the manufacture of an integrated circuit on a semiconductor substrate it may be necessary to create an area of oxide coating. Traditionally, semiconductor substrates are silicon and the desired oxide coating is silicon dioxide. Oxidation of silicon is a thermally dependant process, generally performed at temperatures of between 900-1050°C. It is known that the thermal oxidation rate of silicon at those temperatures is further dependent on many parameters, including, but not limited to: the crystallographic orientation of the Si; the Si doping level; the presence of halogen impurities (Cl, HCl, TCA, TCE) in the gas phase; the pressure during growth; the presence of a plasma during growth; and the presence of a photon flux during growth. In addition to the use of halogens in the gas phase during an oxidation step, it is also known to use ion implantation to

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selectively implant halogen ions in silicon to provide simultaneous differential (greater) oxidation of the implanted regions vs. non-implanted regions during an oxidation step.

The high temperatures traditionally used for silicon oxidation have drawbacks, however, at certain stages of semiconductor manufacture. For instance, high temperatures may cause undesired diffusion of dopants, which in turn may degrade performance of the semiconductor device. Thus, for any oxidation step performed after well dopants are in place, or after source and drain diffusion regions have been created, the oxidation step creates the undesired effect of redistributing dopants by diffusion.

For example, after pattern etching, such as reactive ion etching (RIE) of a polygate, certain features in the device structure require an oxidation step to repair undesired etch features or defects. These defects often occur on sidewalls or non-planar structures of the device.

Referring now to Figs. 1 - 4, there is illustrated a process for etching a gate structure 20. As shown in Fig. 1, a typical semiconductor wafer 9 may comprise a doped well 10 in substrate 11, a gate dielectric or oxide layer 12 above the well, and a polysilicon layer 14 disposed on top of the gate oxide layer. The typical process for making a patterned gate structure 20 (shown in Fig. 4) comprises applying a photoresist 18 over the polysilicon layer 14 as shown in Fig. 1. The photoresist 18 is then exposed and

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developed in a pattern that exposes regions 22, as shown in Fig. 2. The layers under the exposed regions 22 will be removed in an etching process such as RIE, while the layers under protective photoresist 18' will not be removed.

RIE removes the exposed regions 22 in an essentially anisotropic, or vertical, manner to create isolated gate structure 20 under protective photoresist 18', as shown in Fig. 3. Often, to fully remove all the unwanted polysilicon gate material from topographic features in the device structures, a timed or end-pointed "over-etch" is used. During this over-etch, the thin gate oxide layer 12 under the gate polysilicon layer 14 may be etched out from under the edge 15 of the gate polysilicon layer, causing undercut 24 in sidewall 26. The sidewall 26 is critical for device reliability (electric fields, and therefore oxide damage, are most severe here), so the gate oxide 12 must be re-grown on sidewall 26 before any further processing is done. Typically, the photoresist 18 is removed, and a sidewall oxidation process oxidizes the polysilicon gate edge 15 and the adjacent area. The sidewall oxidation fills in undercut 24 in gate oxide 12 of Fig. 3, generally resulting in a repaired gate oxide 112, as shown in Fig. 4. Gate oxide 112 as shown in Fig. 4 after sidewall oxidation, is generally thicker than the original gate oxide 12 of Fig 3. Excess portions of the repaired gate oxide 12 beyond the portion directly under gate polysilicon layer 14, may later be removed.

A high-temperature oxidation (900 - 1050°C) is

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conventionally used for this sidewall oxidation. Because the high-temperature oxidation is done after all the doping is completed in well 10, the high-temperatures may diffuse the dopants, potentially resulting in degraded device performance.

In view of the shortcomings of the prior art, there is a need for a silicon oxidation process that minimizes dopant diffusion.

SUMMARY OF THE INVENTION

The present invention relates to a process for thermal oxidation of a semiconductor substrate, the process comprising exposing the substrate to a chlorine plasma, and then heating the substrate in an oxidizing ambient. The heating step may further comprise heating at a temperature of between 750°C and 850°C.

The present invention further relates to simultaneous thermal oxidation of a plurality of crystallographic orientations, the process comprising the steps of exposing the plurality of crystallographic orientations simultaneously to a chlorine plasma, and then heating the plurality of crystallographic orientations simultaneously in an oxidizing ambient.

It is to be understood that both the foregoing general description and the following detailed description are exemplary, but are not restrictive, of the invention.

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BRIEF DESCRIPTION OF DRAWING

The invention is best understood from the following detailed description when read in connection with the accompanying drawing. It is emphasized that, according to common practice, the various features of the drawing are not to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Included in the drawing are the following figures:

Fig. 1 is a cross-sectional illustration of the layers of a prior art semiconductor device;

Fig. 2 is a cross-sectional illustration of the semiconductor device of Fig. 1 following exposure and developing of the photoresist;

Fig. 3 is a cross-sectional illustration of the semiconductor device of Fig. 2 following a RIE step;

Fig. 4 is a cross-sectional illustration of the semiconductor device of Fig. 3 following re-growth of the oxide layer;

Fig. 5 is a flowchart depicting an exemplary process of the present invention;

Fig. 6 is a cross-sectional illustration of the semiconductor device of Fig. 3 being treated in accordance with an exemplary embodiment of the present invention;

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Fig. 7 is a graph representing the concentration of dopants with respect to the depth of a doped region after oxidation;

Fig. 8 is a cross-sectional illustration of a pFET and an nFET structure on a substrate, having a p+ diffusion region adjacent to the pFET gate;

Fig. 9 is a cross-sectional illustration of the pFET and nFET structures of Fig. 8 following creation of a protective oxide layer over the p+ diffusion region in accordance with an exemplary embodiment of the present invention;

Fig. 10 is a cross-sectional illustration of the structures of Fig. 9 following further process steps;

Fig. 11 is a flowchart depicting the process of the present invention as applied to the exemplary embodiment illustrated in Figs. 8-10.

Fig. 12 is a cross-sectional illustration of a cylindrical, vertical gate structure according to a second exemplary embodiment of the present invention; and

Fig. 13 is a plan view of the cylindrical, vertical gate structure of Fig. 12.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to the drawing, wherein like

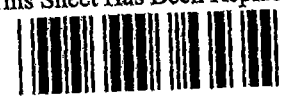
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reference numerals refer to like elements throughout, Fig. 5 depicts a flowchart of a thermal oxidation process according an exemplary embodiment of the present invention. Essentially, the invention comprises exposing a substrate, or a portion of a substrate, to a chlorine plasma in step 500, and then heating the substrate in an oxidizing ambient in step 502. The invention may be further understood with respect to specific examples.

Referring now to Fig. 6, there is shown an illustration of gate 20', similar to gate 20 of Fig. 2, undergoing an exemplary process of the present invention. In accordance with the present invention, first the wafer 9, including undercut 24 in gate oxide 12, is exposed to an unbiased, isotropic chlorine plasma 36. The chlorine plasma 36 introduces chlorine at high concentrations into the near surface of the exposed silicon, to depths of about 10 - 20 Angstroms. Then the silicon is exposed to an oxidizing ambient for a predetermined time period at a temperature of between about 750°C and about 850°C. Preferably, the temperature may be about 800°C.

The time period required for an 800°C oxidation step following treatment with the chlorine plasma is equivalent to the time period required for a 1025°C oxidation without the chlorine plasma. The resulting gate structure 20' having re-grown oxide layer 12, is similar to gate structure 20 constructed in accordance with the prior art as shown in Fig. 4. The gate structure 20' constructed in accordance with the exemplary process of the present

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invention, however, includes chlorine ions in the oxide layer.

Alternatively, a high-temperature oxidation step following exposure to chlorine plasma could be conducted in less time than a high-temperature oxidation step without prior chlorine exposure. This may also result in the reduced diffusion of dopant distributions in the well.

The use of plasma to deliver chlorine to the silicon surface provides a much higher chlorine concentration at the silicon surface than the use of HCl gas (or other halogen-containing gases) during the oxidation process. Furthermore, the higher chlorine concentration at the surface provides for an increased oxidation rate at the low oxidation temperatures of the present invention as compared to the oxidation rate using a halogen-containing gas during the oxidation process. It may be possible to achieve 30-40% chlorine in the surface with the plasma process, while the gas phase method is restricted to a few percent because the surface is oxidized simultaneously with the chlorine exposure, thus preventing further chlorine penetration.

In addition, an unbiased, isotropic plasma is essential when it is necessary for the chlorine to contact structures having non-planar topography, such as an undercut gate sidewall. For planar structures, a biased or anisotropic plasma may be used.

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Referring now to Fig. 7, there is shown a graph depicting well depth in Angstroms vs. the log_{10} of dopant concentration in atoms/cubic centimeter, after oxidation. Curve 27 represents the well doping distribution after a low-temperature oxidation step of the present invention. Curve 27 has distinct peaks 28 and a distinct valley 29 of dopant concentration at selected depths, essentially the same as the desired peaks and valleys prior to oxidation (not shown). Such peaks and valleys represent an optimal distribution of dopants necessary for maximized device performance, such as for threshold-adjust and anti-punchthrough implants for buried channel devices, for example.

Curve 27', on the other hand, depicts the well doping distribution after a high-temperature oxidation. Curve 27', as shown in Fig. 7, has a flattened distribution devoid of distinct peaks or valleys, due to diffusion of the dopants during the high-temperature step. The flattened dopant distribution may have a negative impact on device performance.

The use of the process of the present invention for sidewall oxidation is especially advantageous, because sidewall oxidation is one of the remaining long, high-temperature processes that diffuses the dopants. Stabilization anneals used after the dopants are implanted can minimize the dopant movement in subsequent anneals when the subsequent anneals are short, as in the activation of source/drain implants and in contact silicide formation.

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Thus, sidewall oxidation presents a greater dopant diffusion risk than the subsequent anneals, and requires additional protection such as the process of the present invention.

The process of exposing silicon to a chlorine plasma and then exposing the silicon to an oxidizing ambient at a lower-than-normal oxidation temperature may be applied to any silicon oxidation process step where it is desired to keep temperatures low for any reason.

The process of the present invention may further be used in a process for integration of n- and p-type diffusion sources into a silicon substrate. Referring now to Figs. 8 - 11, there is shown a schematic illustration in Figs. 8 - 10 of a portion of a wafer 28 undergoing steps in an exemplary process depicted in the flowchart of Fig. 11. Wafer 28 comprises a silicon substrate 30 having a pFET gate 32 and an nFET gate 34 thereon, and a p+ diffusion region 33 adjacent to pFET gate 32. The process generally comprises (a) at Step 1100, exposing the wafer 28 to a chlorine plasma 36 as illustrated in Fig. 8; (b) at Step 1102, exposing the wafer to an oxidizing ambient for a predetermined time period at a temperature of between about 650°C and about 750°C to provide an oxide layer 40 over the p+ diffusion region 33 as illustrated in Fig. 9; (c) at Step 1104, creating an n+ diffusion region 35 (shown in Fig. 10) adjacent to nFET gate 34; and (d) at Step 1106, etching away the oxide layer 40, achieving the resulting structure shown in Fig. 10.

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The above process may also be performed where the n+ diffusion region 35 is created first and protected with the oxide layer grown in accordance with the present invention, and the oppositely-charged p+ region 33 is created second.

The diffusion regions 33 and 35 may be created by a solid state diffusion process using an applied layer of appropriately doped glass (boronsilica glass (BSG) for the p+ region 33 and arsenicsilica glass (ASG) for the n+ region 35, for example) and annealing. The presence of oxide layer 40 over the p+ diffusion region 33 while the n+ diffusion region 35 is being formed protects the p+ region.

The diffusion regions 33 and 35 may be created by any process known in the art, which may include protecting the nFET gate 34 and future n+ diffusion region 35 with a layer of tetraethylorthosilicon (TEOS) 38 (shown in Fig. 8) during the creation of p+ diffusion region 33, treatment with chlorine plasma 36, and subsequent creation of oxide layer 40. Conversely, if the n+ diffusion region 35 is created first, the TEOS layer 38 would protect the pFET gate 32 and future p+ diffusion region 33 during creation of the n+ region 35 and creation of a protective oxide layer in accordance with the present invention.

The order and manner of creation of the diffusions is unimportant, however, to the present invention. What is important, is that the protective oxide is created by a low-temperature oxidation step enabled by prior exposure to a

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chlorine plasma 36. With TEOS layer 38 over the nFET gate 34 and n+ diffusion region 35, only the p+ diffusion region 33 and adjacent pFET gate 32 are exposed, so the protective oxide 40 will only grow over the silicon diffusion region 33 during the oxidation step. Low-temperature oxidation is important because creating protective oxide 40 by a high-temperature oxidation step would cause undesired diffusion of the dopants deeper into diffusion region 33 while oxide 40 is being created.

In both the exemplary process embodiments for sidewall oxidation and for integration of the diffusion sources, the process steps of the present invention are used to create what may be referred to as a "sacrificial oxide". A sacrificial oxide is sacrificial in the sense that it serves a particular purpose, such as to protect one diffusion source while another one is created, and then all or a part of it is later removed. Sacrificial oxides may also be used to remove residual pad nitride from active device regions, to protect the exposed silicon surface from contamination and plasma ion damage during mask and etch processing, and/or to remove damaged or contaminated silicon prior to gate oxidation. Using the chlorine plasma step prior to oxidation avoids the need for a high-temperature oxidation process that may redistribute the well-doping concentrations.

Yet another application of the present invention is in the development of vertical gate structures in high-density applications. Referring now to Figs. 12 and 13,

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there is shown a substrate 50 having a vertical FET 52 with a cylindrical structure disposed thereon. Because of the cylindrical geometry, FET 52 has both a <110> crystallographic orientation and a <100> crystallographic orientation around its circumference. Different crystallographic orientations have different surface reaction rate constants, and thus different oxidation rates. As a result, the <110> orientation oxidizes faster than the <100> orientation. The differing oxidation rates may result in gate oxides with non-uniform thickness around the cylinder. This effect can be minimized by reducing the surface reaction rate constant by the use of an impurity. Reduction of the surface reaction rate constant overall, minimizes its impact on the oxidation rate.

In accordance with the present invention, the impurity introduced to the silicon is chlorine. The chlorine is introduced by exposing the silicon to an isotropic chlorine plasma. The isotropic plasma is particularly useful for assuring the non-planar topography of the cylindrical structure of FET 52 is evenly bombarded with chlorine. Chlorine also increases the parabolic rate constant -- the rate at which the oxygen diffuses through the oxide to the oxide/silicon interface -- further reducing the difference in oxidation rates between <100> and <110> silicon. Thus, when the wafer is exposed to the oxidizing ambient, the oxidation rates are more similar for each silicon orientation, and the resulting oxide thickness around the cylinder is more nearly uniform.

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Although a reduced temperature may be used with this process, because there is no particular need to have a reduced temperature due to doping considerations, a normal temperature of 900-1200° C may be used, resulting in a faster oxidation step.

Although the exemplary processes described herein have been described with respect to silicon substrates, the process according to the present invention is not limited to silicon. Other semiconductive, oxidizable materials, such as germanium or germanium/silicon alloys, may also benefit from the process steps of the present invention.

Although illustrated and described herein with reference to certain specific embodiments, the present invention is nevertheless not intended to be limited to the details shown. Rather, various modifications may be made in the details within the scope and range of equivalents of the claims and without departing from the spirit of the invention.

What is Claimed is:

1. *A process for thermal oxidation of a semiconductor substrate, the process comprising the steps of:*

a) exposing the substrate to a chlorine plasma, and then

b) heating the substrate in an oxidizing ambient.

2. The process according to claim 1, wherein the semiconductor substrate comprises silicon, germanium, or a combination thereof.

3. The process according to claim 2, wherein in step (b) the semiconductor substrate is heated at a temperature of between about 750°C and about 850°C.

4. The process according to claim 1, wherein step (a) includes exposing the semiconductor substrate to an unbiased, isotropic chlorine plasma.

5. The process according to claim 1, wherein step (b) includes the step of creating a sacrificial oxide.

6. The process according to claim 1, wherein said semiconductor substrate further comprises a gate having a gate oxide, and said process further comprises prior to step (a) the step of exposing said gate to an etching

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process that forms an undercut in said gate oxide, and wherein step (b) further comprises the step of growing an oxide layer for repairing said undercut.

7. The process according to claim 2, wherein said semiconductor substrate has a first diffusion region therein, and step (b) further comprises heating said substrate at a temperature of between about 650°C and about 750°C and thereby growing a protective oxide layer over said first diffusion region.

8. The process according to claim 7, wherein the process further comprises the steps of:

c) creating a second diffusion region; and

d) removing the protective oxide layer.

9. *A process for simultaneous thermal oxidation of a plurality of crystallographic orientations, the process comprising the steps of:*

a) exposing the plurality of crystallographic orientations simultaneously to a chlorine plasma, and then

b) heating the plurality of crystallographic orientations simultaneously in an oxidizing ambient.

10. The process according to claim 9, wherein the plurality of crystallographic orientations comprise silicon, germanium, or a combination thereof.

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11. The process according to claim 9, wherein the chlorine plasma is an unbiased, isotropic chlorine plasma.

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