PRINZ & PARTNER

PATENTANWÄLTE
EUROPEAN PATENT ATTORNEYS

Manzingerweg 7
D-81241 München

September 6, 1993

Texas Instruments Incorporated
13500 North Central Expressway
Dallas, Texas 75265
United States of America

Our file: T 6493 EP

REDUCED CAPACITANCE LEAD FRAME FOR LEAD ON CHIP PACKAGE

ABSTRACT

In a lead on chip, LOC, integrated circuit packaging arrangement (10), the conductors (46) terminate in fingers (50) that receive the bond wires (20). Adjacent the fingers (50), the conductors (46) have arm parts (52) extending over the major face of the integrated circuit (12). These arm parts (52) are formed by stamping, rolling or otherwise to present an upwardly opening channel with at least the bottom lateral margins (54, 56) of the arm part (52) raised above the plane of the bottom surface (58) of the arm part (52). This reduces sagging of the arm part (52) and capacitive interaction with the integrated circuit.

Fig. 3

This Sheet Has Been Replaced

