Claims

1. A non-volatile semiconductor memory device comprising a plurality of word lines formed in a matrix to which either one of a charge storage gate voltage and a charge storage inhibition gate voltage is applied, a plurality of memory cells connected to the respective word lines, and a bit line that applies a selective voltage to the plurality of memory cells, a charge being stored in selected one of the plurality of memory cells due to a voltage difference between the charge storage gate voltage applied to the word line and the voltage applied to the bit line,

further comprising power supply units respectively provided for word line columns and common wirings respectively provided for word line rows, each of the common wirings applying a predetermined common voltage to the power supply units on a word-line-row basis,

each of the power supply units including

switching mechanisms that are respectively provided for the word lines and respectively connect the word lines to the common wirings, and

a unit wiring that uniformly applies different unit voltages to each of the switching mechanisms in the power supply unit depending on whether or not the selected memory cell exists in the word line column, wherein

the switching mechanisms in each of the power supply units are turned on or off based on a voltage difference between the unit voltages applied to each of the power supply units and the common voltage, to individually apply the charge storage gate voltage or the charge storage inhibition gate voltage to each of the word lines via the power supply unit.

2. The non-volatile semiconductor memory device according to claim 1, wherein

the switching mechanism includes at least a PMOS switch and an NMOS switch, and

the PMOS switch and the NMOS switch are individually turned on or off based on a voltage difference between the common voltage and the unit voltages occurring when the common voltage and the unit voltage are respectively applied thereto.

3. The non-volatile semiconductor memory device according to claim 2, wherein

the common wiring includes a common PMOS control line connected to a control gate of the PMOS switch and a common NMOS control line connected to a control gate of the NMOS switch,

the unit wiring includes a first power supply line connected to a source of the PMOS switch and a second

power supply line connected to a source of the NMOS switch, and

the word line is connected to each of drains of the PMOS switch and the NMOS switch.

4. The non-volatile semiconductor memory device according to claim 2 or claim 3, wherein

in the selected power supply unit to which the selected word line having the selected memory cell thereon is connected among the power supply units,

the NMOS switch is turned off and the PMOS switch having the source to which the charge storage gate voltage is applied is turned on so that the charge storage gate voltage is applied to the selected word line from the drain of the PMOS switch.

5. The non-volatile semiconductor memory device according to claim 3, wherein

a first PMOS power supply line and a second PMOS power supply line are connected to the common PMOS control line via first selection means,

the common PMOS control line applies a control voltage on either one of the first PMOS power supply line and the second PMOS power supply line to the PMOS switch in each of the power supply units using the first selection means,

a first NMOS power supply line and a second NMOS power supply line are connected to the common NMOS control line via second selection means, and

the common NMOS control line applies a control voltage on either one of the first NMOS power supply line and the second NMOS power supply line to the NMOS switch in each of the power supply units using the second selection means.

6. The non-volatile semiconductor memory device according to claim 2, wherein

the common wiring is a common power supply line connected to each of the sources of the PMOS switch and the NMOS switch,

the unit wiring includes

a PMOS power supply line connected to the control gate of the PMOS switch, and

an NMOS power supply line connected to the control gate of the NMOS switch, and

the word line is connected to each of the drains of the PMOS switch and the NMOS switch.

7. The non-volatile semiconductor memory device according to any one of claims 1 to 6, wherein

the power supply unit includes

auxiliary switches that are respectively provided for the switching mechanisms and are connected to the unit wiring, and

an auxiliary switching power supply line that uniformly applies different auxiliary control voltages, respectively, to the auxiliary switches in the power supply unit depending on whether or not the selected memory cell exists in the word line column, and

the auxiliary switch is turned on based on a voltage difference between the unit voltages and the auxiliary control voltages when only the non-selected memory cells exist in the word line column, to apply the unit voltages to a non-selected word line to which only the non-selected memory cells other than the selected memory cell are connected as the charge storage inhibition gate voltage.

8. The non-volatile semiconductor memory device according to any one of claims 1 to 7, wherein

a control voltage difference between one control voltage applied as the common voltage to the common wiring in the selected word line row to which the selected memory cell is connected and another control voltage that is applied as the common voltage to the common wiring in the non-selected word line row to which only the non-selected memory cells other than the selected memory cell are connected is selected as a

voltage difference between the charge storage gate voltage and the charge storage inhibition gate voltage.

9. The non-volatile semiconductor memory device according to claim 8, wherein

the control voltage difference is 6[V] or less.

10. The non-volatile semiconductor memory device according to claim 8, wherein

the control voltage difference is 4[V] or less.

11. The non-volatile semiconductor memory device according to any one of claims 1 to 10, wherein

wells having the switching mechanisms formed therein are formed in the respective power supply units to electrically separate from each other.

12. The non-volatile semiconductor memory device according to any one of claims 1 to 11, wherein

each of the word line columns includes P-type memory wells, which electrically separate from one another, and the memory cell has an N-channel type configuration, and

the switching mechanism applies the unit voltage having a higher voltage value than the voltage applied to the bit line as the charge storage gate voltage to the selected word line to which the selected memory cell is connected.

Claims

1. A non-volatile semiconductor memory device comprising a plurality of word lines arranged in a row direction and a column direction to which either one of a charge storage gate voltage and a charge storage inhibition gate voltage is applied, a plurality of memory cells connected to the respective word lines, and a bit line that applies a selective voltage to the plurality of memory cells, a charge being stored in selected one of the plurality of memory cells due to a voltage difference between the charge storage gate voltage applied to the word line and the voltage applied to the bit line,

further comprising power supply units respectively provided for word line columns in which the plurality of word lines are arranged in the column direction, and common wirings extending in the row direction so as to intersect the power supply units and respectively provided for word line rows in which the plurality of word lines are arranged in the row direction, each of the common wirings applying a predetermined common voltage to the power supply units on a word-line-row basis,

each of the power supply units including

switching mechanisms that are respectively provided for the word lines and respectively connect the word lines to the common wirings, and

a unit wiring that extends in the column direction, connects to the switching mechanisms and uniformly applies unit voltage to the switching mechanisms, the unit voltage being different for each of the power supply units depending on whether or not the selected memory cell exists in the word line column, wherein

the switching mechanisms in each of the power supply units are turned on or off based on a voltage difference between the unit voltages applied to each of the power

supply units and the common voltage, to individually apply the charge storage gate voltage or the charge storage inhibition gate voltage to each of the word lines via the power supply unit.

2. The non-volatile semiconductor memory device according to claim 1, wherein

the switching mechanism includes at least a PMOS switch and an NMOS switch, and

the PMOS switch and the NMOS switch are individually turned on or off based on a voltage difference between the common voltage and the unit voltages occurring when the common voltage and the unit voltage are respectively applied thereto.

3. The non-volatile semiconductor memory device according to claim 2, wherein

the common wiring includes a common PMOS control line connected to a control gate of the PMOS switch and a common NMOS control line connected to a control gate of the NMOS switch,

the unit wiring includes a first power supply line connected to a source of the PMOS switch and a second power supply line connected to a source of the NMOS switch, and

the word line is connected to each of drains of the PMOS switch and the NMOS switch.

4. The non-volatile semiconductor memory device according to claim 2 or claim 3, wherein

in the selected power supply unit to which the selected word line having the selected memory cell thereon is connected among the power supply units,

the NMOS switch is turned off and the PMOS switch having the source to which the charge storage gate

voltage is applied is turned on so that the charge storage gate voltage is applied to the selected word line from the drain of the PMOS switch.

5. The non-volatile semiconductor memory device according to claim 3, wherein

a first PMOS power supply line and a second PMOS power supply line are connected to the common PMOS control line via first selection means,

the common PMOS control line applies a control voltage on either one of the first PMOS power supply line and the second PMOS power supply line to the PMOS switch in each of the power supply units using the first selection means,

a first NMOS power supply line and a second NMOS power supply line are connected to the common NMOS control line via second selection means, and

the common NMOS control line applies a control voltage on either one of the first NMOS power supply line and the second NMOS power supply line to the NMOS switch in each of the power supply units using the second selection means.

6. The non-volatile semiconductor memory device according to claim 2, wherein

the common wiring is a common power supply line connected to each of the sources of the PMOS switch and the NMOS switch,

the unit wiring includes

a PMOS power supply line connected to the control gate of the PMOS switch, and

an NMOS power supply line connected to the control gate of the NMOS switch, and

the word line is connected to each of the drains of the PMOS switch and the NMOS switch.

7. The non-volatile semiconductor memory device according to any one of claims 1 to 6, wherein

the power supply unit includes

auxiliary switches that are respectively provided for the switching mechanisms and are connected to the unit wiring, and

an auxiliary switching power supply line that uniformly applies different auxiliary control voltages, respectively, to the auxiliary switches in the power supply unit depending on whether or not the selected memory cell exists in the word line column, and

the auxiliary switch is turned on based on a voltage difference between the unit voltages and the auxiliary control voltages when only non-selected memory cells exist in the word line column, to apply the unit voltages to a non-selected word line to which only the non-selected memory cells other than the selected memory cell are connected as the charge storage inhibition gate voltage.

8. The non-volatile semiconductor memory device according to any one of claims 1 to 7, wherein

a control voltage difference between one control voltage applied as the common voltage to the common wiring in the selected word line row to which the selected memory cell is connected and another control voltage that is applied as the common voltage to the common wiring in the non-selected word line row to which only the non-selected memory cells other than the selected memory cell are connected is selected as a voltage difference between the charge storage gate voltage and the charge storage inhibition gate voltage.

9. The non-volatile semiconductor memory device according to claim 8, wherein

the control voltage difference is 6[V] or less.

10. The non-volatile semiconductor memory device according to claim 8, wherein

the control voltage difference is 4[V] or less.

11. The non-volatile semiconductor memory device according to any one of claims 1 to 10, wherein

wells having the switching mechanisms formed therein are formed in the respective power supply units to electrically separate from each other.

12. The non-volatile semiconductor memory device according to any one of claims 1 to 11, wherein

each of the word line columns includes P-type memory wells, which electrically separate from one another, and the memory cell has an N-channel type configuration, and

the switching mechanism applies the unit voltage having a higher voltage value than the voltage applied to the bit line as the charge storage gate voltage to the selected word line to which the selected memory cell is connected.