

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO INTER- CONNECTION OF ELECTRICAL DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York, State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to methods for making interconnection patterns.

In microelectronics it is often necessary to provide in one device a high density of electrically isolated conductive paths to interconnect various regions of the device. This usually requires the crossover by one conductive path of a different conductive path. Typical of the problem is the interconnection of different circuit elements in a monolithic integrated circuit. Here a single semiconductive wafer houses a plurality of circuit elements, which internally are isolated from one another by p-n junction isolation techniques, and interconnection there-between is effected externally by the formation of a plurality of conductive paths on the surface of the wafer, which cross over one another. Similar requirements arise in the fabrication of micromagnetic circuits.

A common method for achieving the desired interconnection involves providing over the wafer an insulating layer and then depositing a continuous conductive layer over the insulating layer, provision being made to reduce the thickness of the insulating layer where electrical connection of the wafer is desired to this first conductive layer. Then portions of this conductive layer are selectively removed to leave behind the first conductive pattern desired. After forming an insulating layer over the conductive pattern just formed

and providing regions of reduced thickness of any insulation at regions where the second conductive pattern is to make electrical connection to the wafer, a second continuous conductive layer is deposited and portions of this layer are selectively removed to leave behind the second conductive pattern desired, typically involving portions which cross over portions of the first conductive pattern.

In processes of this kind, low cost and high densities make it important to employ thin insulating layers between separate conductive patterns. However, it is found that the use of thin insulating layers tends to result in a high incidence of faulty crossovers. Some of the faults are attributable to edge effects, the insulating layer being especially prone to defects where it extends over the edges of an underlying conductive pattern, presumably because of the discontinuities produced at such edges.

An object of the present invention is to provide an interconnection technique which reduces this edge effect and so results in fewer defects.

According to the present invention there is provided a method for making an interconnection pattern comprising forming a layer of conductive material capable of being converted into an insulative material, masking a region of the layer such that the masked region corresponds to a first required conductive pattern, completely converting the unmasked regions of the layer into the insulative material, and forming over the resulting layer of conductive and insulating material a second conductive pattern insulated from the first pattern.

The invention will be better understood from the following more detailed description taken in conjunction with the accompanying drawing in which FIGS 1 to 3 illustrate a semiconductive wafer in various

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stages in the process of providing electrical interconnections thereto in accordance with an exemplary embodiment of the invention.

With reference now to the drawing, there will now be described the fabrication of a simple two level interconnection pattern for a silicon monolithic integrated circuit with specific attention to the novel features of the fabrication.

It will be assumed that there has been prepared in known fashion a monolithic silicon integrated circuit device which includes a number of circuit elements appropriately isolated internally within the silicon wafer by any of the known techniques, such as p-n junction isolation. The details of the circuit elements are not being shown. The emphasis herein will be on the interconnection of these elements externally by conductive patterns deposited on the surface of the silicon wafer.

Typically the surface of the wafer where connections are to be made will include an insulating layer thereover, typically silicon oxide, whose thickness needs to be modified where connection is to be made. Any single connection can be either d-c, in which case the insulating layer needs to be essentially completely removed where such connection is desired, or the connection can be capacitive, as the gate of an insulated gate field effect transistor, in which case the insulating layer is merely thinned appropriately. Moreover even when the connection is to be of the direct current form it may be either ohmic or rectifying, as of the Schottky barrier type. If a Schottky barrier type connection is desired, the area of the wafer where connection is to be made is treated appropriately before the interconnection pattern is deposited. For example, a localized platinum silicide layer may be formed, in known manner, in an opening in the oxide layer.

As shown in FIG. 1, after the silicon oxide layer 11 has been appropriately thinned and any metallizing of exposed areas completed, there is deposited over the wafer 12 a conductive layer 13 of the kind described. Advantageously, the layer is of polycrystalline doped silicon deposited by evaporation or sputtering. In some instances, it may be preferred to utilize a film-forming metal, such as aluminum, tantalum, titanium zirconium, or niobium which can readily be oxidized to form an insulator.

Typically, the thickness of a silicon layer would be between 0.1 to 1 μ . After deposition of the layer, a mask 14 is provided thereover to define the first conductive pattern as shown in FIG. 2. This can be done in conventional fashion and typically involves photolithographic techniques. In some instance it will prove advantageous

to utilize as the final mask a layer of a material, which can be left in place to serve at least in part as the insulation between the first conductive pattern and subsequently formed conductive patterns. Typical of such materials are silicon nitride, silicon dioxide and aluminum oxide.

After the mask is in place, the surface of the wafer is treated to convert the exposed portions of the conductive layer to the insulator as desired in a manner appropriate to the particular material. If the layer is of silicon, conversion to the oxide can be effected in any suitable manner, as for example by exposure to an oxygen plasma for appropriate periods of time as described in US patent No. 3,476,971, or by oxygen bombardment as disclosed in Patent No. 1,291,450. In the latter case it is important that the mask be sufficiently thick to avoid substantial ion penetration. If the conductive layer is of a film-forming metal, it may be preferable to convert the unmasked portion to an insulating oxide by electrolytic techniques, for example as is common in the solid electrolytic capacitor art.

It can be appreciated that by this technique of formation, the conductive pattern 13 is left imbedded in an insulating matrix 15, as seen in FIG. 3. The conversion to an insulator will generally involve an increase in bulk with a consequent increase in height of the insulator portion. However, the discontinuity presented at the transitions from conductive material to insulating material typically will be less than would be the case if the insulating portion were completely removed.

Moreover, if the mask is of a material suitable for use as an insulator between the first conductive pattern and a second conductive pattern to be formed thereover, as is the case when it is of silicon nitride, the mask thickness advantageously can serve to reduce still further any discontinuity in planarity occurring at the transition between the converted and unconverted material as is illustrated in FIG. 3.

If the mask is not to be used in this way, it can be removed and a new layer of additional insulating material formed over both the converted and unconverted material. In some instances, it may be feasible to convert a surface portion of the conducting pattern to form the insulator, or alternatively insulating material may be deposited. In some instances, it may be advantageous both to retain the mask and to deposit an additional insulating layer over it and the converted material.

Next there are formed by conventional techniques regions of reduced thickness, as was done before deposition of the first conductive pattern, where connection either

d-c or capacitive is to be made to the wafer by the second conductive pattern.

Then there is deposited uniformly over the wafer a second conducting layer of a material suitable for use in the second conductive pattern. If there is to be a third conductive pattern, which is to cross over this second pattern and if it is important to avoid crossover problems, then the second conducting layer advantageously is of a material chosen in the light of the same considerations affecting the choice of the first layer, and the second conductive pattern is formed therefrom in a manner analogous to the formation of the first conductive pattern. If there is no need to be concerned about subsequent crossovers, the material for the second conductive layer and the formation therefrom of the second conductive pattern can follow the practice presently in the art. This typically involves deposition of a metal layer, such as aluminum or titanium or a composite, the formation thereof by photo-lithographic techniques of an etch-resistant mask defining the desired conductive pattern, and the selective removal by etching of the unmasked material to leave behind the desired second conductive pattern 16 as seen in FIG. 3. It is significant to recognize that the composite layers in the vicinity of the crossover are essentially planar so as to minimize the occurrence of the edge defects alluded to before.

It will be apparent that the various embodiments described are merely illustrative of the general principles of the invention. In particular, a variety of other materials can be used. For example, it is unnecessary that the conductive layer be converted into an oxide and in some instances as when the conductive layer is silicon to convert it to a nitride as by treatment in a nitrogen plasma, or to a carbide in known fashion. Also in some instances, it may be feasible to convert the desired portion of the conductive layer by irradiation in accordance with the desired pattern by a laser, ion or electron beam.

WHAA WE CLAIM IS:—

1. A method for making an

interconnection pattern, comprising forming a layer of conductive material capable of being converted into an insulative material, masking a region of the layer such that the masked region corresponds to a first required conductive pattern, completely converting the unmasked regions of the layer into the insulative material and forming over the resulting layer of conductive and insulative material a second conductive pattern insulated from the first pattern.

2. A method according to Claim 1, wherein the layer of conductive material is electrically coupled with an electrical device element at selected points and the second conductive pattern is electrically coupled with the element at different selected points.

3. A method according to Claim 2, wherein the said layer of conductive material comprises polycrystalline conductive silicon, and the device element is of semiconductive material.

4. A method according to Claim 1 or 2, wherein the conductive layer comprises a film forming metal.

5. A method according to any one preceding claim, wherein the material used for masking is silicon nitride.

6. A method according to Claim 5, wherein the silicon nitride mask serves as insulation between the first and second conductive patterns.

7. A method according to any one preceding claim, wherein a continuous layer of insulating material is formed over said resulting layer before the formation of said second conductive pattern.

8. A method for forming interconnection patterns, substantially as herein described with reference to the accompanying drawing.

9. An electrical device comprising an interconnection pattern made by the method according to any one of the preceding claims.

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2. A method according to Claim 1, wherein the layer of conductive material is electrically coupled with an electrical device element at selected points and the second conductive pattern is electrically coupled with the element at different selected points.

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