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LAYOUT FOR CMOS IMAGE SENSOR

Abstract of the Disclosure

In this invention, a shielding metal is simultaneously defined in an active area of a pixel region while defining the metal layers of peripheral circuits so as to prevent transistors on the active area from irradiation while the pixels are irradiated and thus to be consistent with the requirement of the SPICE model for transistors. Furthermore, the load effect of non-uniform etching can be improved. The defects that the surrounding metal layer is over-etched, the metal lines with narrower widths are liable to be etched off and the process window becomes narrow in the prior art are therefore solved. In addition, the process for simultaneously defining a shielding metal in the active area needs almost no additional costs but the operation performances and effects of the elements are enhanced.

Fig. 6