

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
13 April 2006 (13.04.2006)

PCT

(10) International Publication Number
WO 2006/039377 A1

(51) International Patent Classification⁷: **H01L 21/8238**,
21/336

Road, Poughquag, NY 12570 (US). **UTOMO, Henry, K.**
[ID/US]; 134 Innis Avenue, #C4, Poughkeepsie NY 12601
(US).

(21) International Application Number:
PCT/US2005/034948

(74) **Agent: LI, Todd M.C.**; IBM Corporation, Bldg. 321/Zip
482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

(22) International Filing Date:
29 September 2005 (29.09.2005)

(81) **Designated States** (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,
KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY,
MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO,
NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK,
SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ,
VC, VN, YU, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/711,637 29 September 2004 (29.09.2004) US

(71) **Applicants** (*for all designated States except US*):
INTERNATIONAL BUSINESS MACHINES COR-
PORATION [US/US]; New Orchard Road, Armonk, NJ
10504 (US). **KABUSHIKI KAISHA TOSHIBA** [JP/JP];
1-1, Shibaura 1-chome, Minato-ku, Tokyo (JP).

(84) **Designated States** (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT,
RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA,
GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(72) **Inventors; and**

(75) **Inventors/Applicants** (*for US only*): **CHEN, Huajie**
[CN/US]; 622 Avalon Lake Road, Danbury, CT 06810
(US). **CHIDAMBARRAO, Dureseti** [US/US]; 29 Old
Mill Road, Weston, CT 06883 (US). **OH, Sang-Hyun**
[KR/US]; 1309 Anacapa Street, Unit #32, Santa Barbara,
CA 93101 (US). **PANDA, Siddhartha** [IN/US]; 15 Van
Horn Circle, #C, Beacon, NY 12508 (US). **RAUSCH,**
Werner, A. [US/US]; 317 Judith Drive, Stormville, NY
12582 (US). **SATO, Tsutomu** [JP/US]; 56 Vanderburgh

Published:

— *with international search report*

*For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*

(54) **Title:** STRAINED CHANNEL FET USING SACRIFICIAL SPACER

(57) **Abstract:** A field effect transistor (FET) (10) is provided which includes a gate stack (29), a pair of first spacers (32) disposed over sidewalls of the gate stack (29) and a pair of semiconductor alloy regions (39) disposed on opposite sides of and spaced a first distance from the gate stack (29). Source and drain regions (24) of the FET (10) are at least partly disposed in the semiconductor alloy regions (39); and spaced a second distance from the gate stack (29) by a corresponding spacer of the pair of first spacers (32), which may be different from the first distance. The FET (10) may also include second spacers (34) disposed on the first spacers (32), and silicide regions (40) at least partly overlying the semiconductor alloy regions (39), wherein the silicide regions (40) are spaced from the gate stack (29) by the first and second spacers (32, 34).

WO 2006/039377 A1