# Silicon-on-Insulator Chip with Multiple Crystal Orientations

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The following U.S. patents and/or commonly assigned patent applications are hereby incorporated herein by reference:

| Patent or Serial No. | Filing Date | Issue Date | Attorney Docket No. |
|---|---|---|---|
| 10/379,873 | March 5, 2003 | | TSMC2002-1384 |
| 10/384,859 | March 10, 2003 | | TSMC2002-1385 |

## TECHNICAL FIELD

[0002] The present invention relates generally to semiconductor devices, and, in particular embodiments, to a silicon-on-insulator chip including silicon islands with multiple crystal plane orientations to enhance the performances of n-channel and p-channel transistors and several methods for the formation of such a silicon-on-insulator chip.

## BACKGROUND

[0003] Complementary metal-oxide-semiconductor (CMOS) technology is the dominant semiconductor technology used for the manufacture of ultra-large scale integrated (ULSI) circuits today. Conventional CMOS technology employs (100) silicon wafer as the starting material for volume production. Such silicon wafers have a surface that is (100) oriented, i.e., the normal to the silicon wafer surface is in the [100] direction. Hence, conventional planar metal-oxide-semiconductor field-effect transistors (MOSFETs) formed on (100) silicon wafers have a gate dielectric-channel interface plane that is in the (100) plane of the silicon substrate.

[0004] Commercial CMOS technology universally uses (100) oriented silicon wafers because of their low surface state density on the order of $10^{10}$ per square centimeter on thermally oxidized surfaces. This compares with surface state densities in the order of $10^{11}$ per square centimeter on thermally oxidized surfaces with other crystal orientations such as the (110) and (111) planes. Another advantage is the high surface mobility of electrons on the (100) plane, as disclosed in "Mobility anisotropy of electrons in inversion layers in oxidized silicon surfaces," Physical Review B, vol. 4, no. 6, (15 September 1971), pp. 1953.

[0005] As a result, an n-channel transistor formed on a silicon substrate with (100) surface provides the largest source-to-drain current. Another benefit of using (100) wafers is the ease of cleavage or cutting along (110) planes. This property is useful when dicing up processed wafers into separate dies prior to packaging, since the equivalent (110) planes intersect with the (100) silicon surface to form squarish shapes. However, the measured mobility of holes in a p-channel transistor is nearly the smallest when the gate dielectric-channel interface is in the (100) plane as compared to other crystal planes.

[0006] Size reduction of the transistor has provided significant improvement in the speed performance, circuit density, and cost per unit function of semiconductor chips over the past few decades. Significant challenges are faced when transistors are scaled into the sub-100 nm regime. This has resulted in research efforts on further improvement of n-channel and p-channel transistor performance using alternative techniques besides transistor scaling, such as the use of strain-induced band-structure modification and mobility enhancement to increase the transistor drive current. Another potential way to improve transistor performance is to explore the use of silicon substrates with non-conventional crystal orientations as the starting wafer.

[0007] U.S. Patent No. 4,857,986, entitled "Short channel CMOS on (110) crystal plane" issued to M. Kinugawa, discloses the formation of CMOS transistors on a monocrystalline silicon substrate having a (110) crystal orientation. In U.S. Patent No. 6,335,231, entitled "Method of fabricating a high reliable SOI substrate" issued to S. Yamazaki *et al.*, a silicon-on-insulator substrate is fabricated having a main crystal surface that is (110) oriented. Both of these references use a (110) oriented silicon surface for both, the n-channel and p-channel planar transistors fabricated on these substrates have a gate dielectric-channel interface that is in the (110) plane.

[0008] In U.S. Patent No. 4,768,076 ('076), entitled "Recrystallized CMOS with different crystal planes" issued to M. Aoki et al., a CMOS integrated chip is formed on a semiconductor crystalline surface having a plane azimuth (110) or (023) in order to increase the speed of operation. The semiconductor devices described in the '076 patent are stacked.

[0009] In U.S. Patent No. 6,483,171 entitled "Vertical sub-micron CMOS transistors on (110), (111), (311), (511), and higher order surfaces of bulk, SOI and thin film structures and method of forming the same" issued to L. Forbes *et al.*, a method for forming n-channel and p-channel transistors that includes cutting a substrate along a higher order orientation and fabricating vertical deep sub-micron n-channel and p-channel transistors on the substrates is provided. In this patent, the vertical transistors have a source-to-drain direction that is perpendicular to the surface of the wafer.

[0010] In U.S. Patent No. 5,384,473, entitled "Semiconductor body having element formation surfaces with different orientations," issued to S. Yoshikawa *et al.*, a semiconductor body is constructed such that a portion of a semiconductor substrate has a first surface plane and another portion of a second semiconductor substrate has a second surface plane.

[0011] In U.S. Patent No. 4,933,298, entitled "Method of making high speed semiconductor device having a silicon-on-insulator structure" issued to M. Hasegawa, a CMOS silicon-on-insulator structure is fabricated by using a silicon substrate with (110) orientation and a silicon layer with (100) orientation. Openings are formed in the insulator to expose the (110) oriented substrate. Silicon regions are then formed with (110) orientation using the (110) substrate as a template. This method uses solid phase epitaxial growth rate.

## SUMMARY OF THE INVENTION

[0012] The preferred embodiment of the present invention relates to a semiconductor device that includes active areas with different crystal orientations. This configuration is useful because the crystal plane orientation can be selected to enhance the performance of n-channel and p-channel transistors. For example, n-channel transistors can be formed in silicon regions with a (100) orientation and p-channel transistors can be formed in regions with a (110) orientation. In the preferred embodiment, the semiconductor device is a silicon-on-insulator device.

[0013] For example, in a first embodiment a silicon-on-insulator device includes an insulator layer, typically formed over a substrate. A first silicon island with a surface of a first crystal orientation overlies the insulator layer and a second silicon island with a surface of a second crystal orientation also overlies the insulator layer. The islands can be isolated from one another by an isolation technique such as shallow trench isolation or mesa isolation.

[0014] The present invention also provides several methods for the formation of such a silicon-on-insulator chip. Each of these methods is compatible with current CMOS processing and, therefore, are good candidates for commercialization.

[0015] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent

constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0016] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0017] Figure 1 is a three-dimensional perspective of a silicon-on-insulator chip with silicon islands of different surface crystal orientations;

[0018] Figure 2a is a specific example showing the use of (110) oriented islands for p-channel transistors and (100) oriented islands for n-channel transistors;

[0019] Figure 2b is another specific example showing the use of (023) oriented islands for p-channel transistors and (100) oriented islands for n-channel transistors;

[0020] Figure 3 is a specific example showing that at least one of the silicon islands may be comprised of a stack of silicon layers;

[0021] Figure 4a-4e show a first embodiment method of forming regions with different silicon crystal orientations;

[0022] Figure 5a-5f show a second embodiment method of forming regions with different silicon crystal orientations;

[0023] Figure 6a-6c show a third embodiment method of forming regions with different silicon crystal orientations;

[0024] Figure 7a-7c show a fourth embodiment method of forming regions with different silicon crystal orientations;

[0025] Figure 8a-8c show a fifth embodiment method of forming regions with different silicon crystal orientations; and

[0026] Figure 9a-9c provide illustrations where concepts of the present invention are applied to a bulk semiconductor substrate.

## DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0027] The preferred embodiment of the present invention relates to a silicon-on-insulator chip that includes silicon islands with multiple surface crystal plane orientations to enhance the performances of n-channel and p-channel transistors. The present invention also provides several methods for the formation of such a silicon-on-insulator chip. In one aspect, the present invention provides optimized crystal orientations separately for the n-channel transistors and the p-channel transistors.

[0028] Transistors formed on silicon-on-insulator may be further improved by optimizing the surface crystal orientations of the islands on which the transistors are formed. This disclosure will first describe a silicon-on-insulator substrate that may be formed such that silicon islands with two or more surface crystal orientations are obtained.

[0029] Figure 1 illustrates a three-dimensional perspective of a silicon-on-insulator substrate 100. The substrate 100 has been processed up to the step of silicon island formation. In this example, three islands (labeled with reference numerals 110 and 112) are formed on buried insulator 114. The islands are isolated from one another by trenches 118. In another embodiment, shallow trench isolation (STI) or other isolation can be used.

[0030] In Figure 1, first silicon islands 110 have an (h k l) surface crystal orientation and second islands 112 have an (h' k' l') surface crystal orientation. In general, (h k l) and (h' k' l') are not equivalent crystal orientations. The crystal orientations may be such orientations as (110), (100), (023), (311), (511), (111), or any other crystal orientation given by (h k l) where h, k, and l are integers. In the preferred embodiment, islands 110 and 112 with surface crystal planes of the (100) and (110) crystal orientations are formed on the insulator layer 114. More

preferably, silicon islands 110 (or 112) with (100) oriented surfaces are used for forming n-channel transistors (not shown) and silicon islands 112 (or 110) with (110) oriented surfaces are used for forming p-channel transistors (not shown).

[0031] Cross-sections of two specific embodiments are schematically shown in Figures 2a and 2b. By forming n-channel transistors 122 on the (100) oriented silicon surfaces 110, maximum electron mobility and drive current can be obtained as compared to other crystal orientations. By forming p-channel transistors 124 on the (110) oriented silicon surfaces 112, maximum hole mobility and drive current can be obtained as compared to other crystal orientations. Therefore, the embodiment shown in Figure 2a will achieve maximum mobilities and drive currents in p-channel and n-channel transistors based on optimal crystal orientations. While one goal of certain embodiments of the present invention is to optimize the performances of the n-channel and p-channel transistors, it is understood, for example, that not all p-channel transistors in the silicon-on-insulator chip need to be formed on the (110) oriented silicon surfaces, and that not all n-channel transistors in the silicon-on-insulator chip need to be formed on the (100) oriented silicon surfaces.

[0032] In another preferred embodiment, as shown in Figure 2b, silicon islands 110 and 112 with (100) and (023) oriented surfaces are formed on the insulator layer, where n-channel transistors 122 are formed on (100) oriented silicon surfaces 110 and p-channel transistors 124 are formed on (023) oriented silicon surfaces 112. While not illustrated, yet other orientations can be included.

[0033] In general, the silicon islands 110 and 112 may not be of the same thickness. This is shown in the figure where the thickness of the silicon islands 110 with (100) oriented surface may be $t_{Si1}$, and the thickness of the silicon islands 112 with (023) oriented surface may be $t_{Si2}$.

It is possible that these thicknesses $t_{si1}$ and $t_{si2}$ are the same. In addition, silicon islands of the same surface crystal orientations need not have the same thickness. The silicon islands 110 and 112 preferably have a thickness in the range of about 10 angstroms to about 1000 angstroms. It is also understood that the cross-sectional views of the silicon islands 110 and 112 are only for the purpose of illustration. For example, the silicon islands 110 and/or 112 need not have sharp corners. The corners of the silicon islands 110 and/or 112 may be rounded or faceted.

[0034] In one example, a silicon island 110 and/or 112 with a surface of a predetermined crystal orientation may be formed from a stack of two or more layers of silicon, where the topmost silicon layer has a surface of the predetermined crystal orientation. Such a stack may have a total or combined thickness in the range of about 10 angstroms to about 1000 angstroms. This embodiment is more clearly illustrated in Figure 3.

[0035] In the example illustrated in Figure 3, the silicon island 110 includes two layers of silicon, the topmost layer 126 having a (h k l) crystal orientation, e.g., (100) oriented silicon surface, and the bottom layer 128 having a (h' k' l') crystal orientation where (h' k' l') may be (110), as an example. It is known that the charge carriers in the transistor inversion layer has a thickness of less than 50 angstroms. Therefore, in the example of Figure 3, as long as the electrons in the inversion layer of the n-channel transistors 122 are entirely (or mostly) contained in the topmost (100) oriented silicon layer, it will have the maximum mobility or transport properties as desired.

[0036] In general, the insulator layer 114 as shown in Figures 1-3 may be comprised of any dielectric material or insulating material such as silicon oxide, silicon nitride, and aluminum oxide (also known as sapphire). The thickness of the insulator may range from about 100 angstroms to about 2000 angstroms. The insulator layer may also be a composite layer

comprising of a stack combination of dielectric materials, such as an aluminum oxide on a silicon oxide stack, or a silicon nitride on a silicon oxide stack. The insulator layer may be in an amorphous state, poly-crystalline state, or in crystalline state.

[0037] The insulator layer 114 overlies a substrate 116. The substrate 116 may be any substrate commonly used in semiconductor processing, such as a silicon substrate with (100) orientation or (110) orientation or any other orientation. The substrate 116 may also be comprised of an alloy semiconductor such as silicon-germanium or any compound semiconductor such as gallium arsenide and indium phosphide. Non-semiconductor substrates such as quartz or glass could alternatively be used.

[0038] Next, the present invention provides several methods of forming the silicon-on-insulator chip with multiple surface crystal orientations. Several of these embodiments will be described now.

[0039] The first embodiment method will now be described with respect to Figures 4a-4e. As shown in Figure 4a, a silicon-on-insulator wafer 102 is provided where the crystalline silicon layer 130 has a first crystal orientation (h k l). Therefore, the surface of the silicon layer is of the (h k l) crystal orientation. Such a silicon-on-insulator 102 wafer may be formed by a wafer bonding and wafer separation technique, or by an oxygen implantation (SIMOX) technique, as examples.

[0040] Selected portions 134 of the silicon layer 130 are amorphosized, i.e., transformed to the amorphous state. This transformation can be performed by masking the wafer 102, opening the mask 132 at the selected portions 134 of the silicon layer 130 to be amorphosized, and implanting ions 136 into the selected portions 134 of the silicon layer 130 to create an amorphous region as shown in Figure 4b. The ion implantation can be done by conventional ion

implantation techniques such as beam-line ion implantation or plasma immersion ion implantation (PIII). Preferably, the implanted ions are silicon ions and implanted to a depth close to the half the thickness of the silicon layer 130. However, other ions such as germanium ions and argon ions may be used.

[0041] The wafer 102 is then heated at elevated temperatures, such as between about 500 to about 600 degrees Celsius, to initiate solid phase epitaxy. Solid phase epitaxy is essentially a re-crystallization process where the amorphous silicon region is transformed into a crystalline region. The amorphous silicon portion 134 re-crystallizes using the underlying crystalline insulator surface 138 as a seed as shown in Figure 4c . The insulator114 can serve as a seed if the insulator 114 is crystalline or if the insulator 114 has a surface 138 that is crystalline. For example, the insulator layer 114 may be crystalline aluminum oxide, i.e., sapphire. In another example, the insulator layer 114 is in fact a stack comprising of a sapphire layer on a silicon oxide layer.

[0042] After the re-crystallization of the amorphous portion 134 of silicon layer 130, a silicon layer portion 134 with a (h' k' l') crystal orientation is formed. The (h' k' l') crystal orientation is different from the original (h k l) crystal orientation of the silicon layer 130. In the preferred embodiment, (h k l) is (110), (h' k' l') is (100), and the insulator layer 114 is (0,1,-1,2) oriented sapphire.

[0043] The preferred embodiment is now described in further detail. This embodiment begins with a (110) oriented silicon layer 130 on a (0,1,-1,2) oriented sapphire layer 114, where the sapphire layer 114 overlies a substrate 116. Such a wafer may be formed by a wafer bonding and wafer separation technique. Selected regions 134 of the (110) oriented silicon layer 130 are amorphosized by a masked implantation of silicon ions. Re-crystallization of the amorphosized

silicon 134 using (0,1,-1,2) oriented sapphire as a seed yields (100) oriented silicon in the selected regions. The silicon layer 130 now comprises of regions 134 and 140 with different crystal orientation.

[0044] Silicon islands 110 and 112 with different crystal orientations may be formed by selective masking and etching as shown in Figure 4d. Transistors 122 and 124 may then be formed on these islands as shown in Figure 4e. The transistors 122 and 124 can be formed by depositing a gate dielectric layer, and gate conductor layer(s), and then patterning these to form a gate dielectric 144 and gate 146. Source and drain regions (not explicitly shown) can then be formed using standard implantation steps. While not shown, the gate 146 may include a gate spacer to form lightly doped source and/or drain portions.

[0045] Figures 5a-5f show a second embodiment method of the present invention. A silicon-on-insulator wafer 104 is provided as shown in Figure 5a. The silicon layer in Figure 5a includes at least two layers 148 and 150 of silicon with different crystal orientations. As shown in Figure 5, a topmost silicon layer 148 with the (h k l) crystal orientation overlies a silicon layer 150 with the (h' k' l') crystal orientation. The thickness of the topmost silicon layer 148 may vary from about 10 angstroms to about 500 angstroms, but is preferably less than about 50 angstroms. The thickness of the silicon layer 150 may be in the range of about 10 to about 500 angstrom and is once again less than about 50 angstroms.

[0046] In one example, the topmost silicon layer 148 can be formed by a layer transfer technique, which comprises of a wafer bonding process and a wafer separation process. For example, we may begin with a silicon-on-insulator target wafer which comprises of a (100)-oriented silicon layer overlying an insulator layer. A donor wafer with a (110)-oriented silicon surface layer may be provided. The donor wafer may, for example, be a (110)-oriented bulk

silicon substrate. It is desired to transfer a top portion of donor wafer to the target wafer. This transfer can be accomplished by implanting hydrogen into the donor wafer, bonding the top surface of the donor wafer to the top surface of the target wafer, and performing an anneal to separate a portion of the donor wafer. The top portion of the donor wafer, i.e., a (110)-oriented silicon layer, then adheres to the target wafer. A bond-strengthening anneal may subsequently be performed.

[0047] Similar processes for wafer bonding and separation are taught in co-pending applications Serial No. 10/379,873 (TSMC2002-1384) and Serial No. 10/384,859 (TSMC2002-1385), both of which are incorporated herein by reference. As examples, the wafer bonding and separation process can be a Smartcut™ process, or a Nanocleave™ process, both available from Silicon Genesis Corporation. Details of bonding and separation processes are also provided in U.S. Patent Nos. 5,013,681, 5,374,564, 5,863,830, 6,355,541, 6,368,938, and 6,486,008, each of which is incorporated herein by reference.

[0048] A patterned mask 132 is formed to expose a selected portion 152 of the topmost (h k l) silicon layer 148 as shown in Figure 5b. The exposed portion 152 topmost (h k l) oriented silicon layer 148 is then etched as shown in Figure 5c. For example, the etch can be a wet etch that is selective with respect to silicon crystal orientations. As a more specific example, etchants such as potassium hydroxide and caesium hydroxide may be used to etch (110) oriented silicon at a much faster rate compared to (100) oriented silicon. Potassium hydroxide etches (110) oriented silicon at twice the rate of (100) oriented silicon.

[0049] Following the etching of the topmost (h k l) oriented silicon layer, the mask 132 is then removed as shown in Figure 5d. According to the second embodiment method, it is preferred that topmost (h k l) oriented silicon is (110) oriented silicon, and the (h' k' l') oriented silicon is

(100) oriented silicon. Another mask (not shown) may be formed to pattern silicon islands 110 and 112, as shown in Figure 5e. N-channel and p-channel transistors 122 and 124 may then be formed on the patterned silicon islands 110 and 112, as shown in Figure 5f.

**[0050]** Referring now to Figure 6a -6c, a third embodiment method will now be described. The initial steps of the third embodiment method are similar to those of the second method embodiment. The third embodiment method employs a silicon-on-insulator substrate 104 where the silicon layer comprises at least two layers of silicon 148 and 150 with different crystal orientations. Continuing from Figure 5c, the topmost (h k l) oriented silicon layer 148 has been selectively etched in a predetermined region 152, exposing the underlying (h' k' l') oriented silicon layer 150, as shown in Figure 6a.

**[0051]** Subsequently, a selective epitaxial growth is performed. This can be a chemical vapor deposition process where silane and hydrogen chloride gases are used and the process temperature may range from about 500 degrees Celsius to about 900 degrees Celsius. The epitaxial growth occurs selectively in the exposed (h' k' l') oriented surface. The cross-section of the substrate is shown in Figure 6b.

**[0052]** Referring now to Figure 6c, the mask can then be removed. As can be seen, a first region 152 comprises of silicon with a (h k l) orientation and a second region 152 comprises of silicon with a (h' k' l') orientation. Silicon islands 110 and 112 may then be patterned and transistors 122 and 124 be formed on the islands (not shown with Figure 6; see Figures 4d-4e or Figures 5e-5f).

**[0053]** Referring now to Figures 7a-7c, a fourth embodiment method will now be described. Once again, the initial steps of the fourth embodiment method are similar to those of the second embodiment method. Continuing from Figure 5b, the topmost (h k l) oriented silicon layer 148

has been selectively exposed in a predetermined region 152. Ion implantation 156 is then performed to transform the exposed (h k l) oriented silicon into an amorphous phase, as shown in Figure 7a. The ion implantation may employ silicon, germanium or argon ions. The implantation energy is chosen such that the amorphosized region is restricted to the surface region where the silicon crystal orientation is (h k l). The crystallinity of the underlying (h' k' l') oriented silicon layer 150 in the exposed region 152 is retained so that it will serve as a seed layer for re-crystallization of the amorphous region 158. This is shown in Figure 7b. The mask 132 is then removed.

**[0054]** Next, the wafer is heated at elevated temperatures, such as between about 500 to about 600 degrees Celsius, to initiate solid phase epitaxy. Re-crystallization of the amorphosized silicon occurs using the underlying (h' k' l') oriented silicon 150 as a seed layer. Silicon islands 110 and 112 with different crystal orientations may be formed by selective masking and etching and transistors 122 and 124 may then be formed on these islands as discussed above.

**[0055]** Referring now to Figure 8a-8c, a fifth embodiment method is discussed. A silicon-on-insulator wafer 106 is provided where the crystalline silicon layer has a first crystal orientation (h k l), as shown in Figure 8a. Referring to Figure 8b, selected portions of the silicon layer 130 are etched to expose the crystalline surface 138 insulator 114. This can be done by masking the wafer with a mask 132, opening the mask 132 at the selected portions of the silicon layer 130 to be etched, and etching the selected portions of the silicon layer 130 by dry or wet etching.

**[0056]** Epitaxy is then performed to grown a silicon layer 164 with a (h' k' l') crystal orientation on the exposed crystalline insulator surface. The epitaxy step can be performed before the mask 132 is removed, as shown in Figure 8c, or after the mask 132 is removed. This step will result in a first region 166 with a (h k l) crystal orientation and a second silicon region

164 with a (h' k' l') crystal orientation. Silicon islands 110, 112 with different crystal orientations may be formed by selective masking and etching and transistors 122 and 124, can then be formed on these islands.

[0057] Each of the embodiments described to here were directed to a silicon-on-insulator substrate. The present invention, however, also includes embodiments applicable to bulk substrate devices. Referring to Figure 9a, as an example, the starting substrate includes a silicon substrate 170 that has a (h' k' l') crystal orientation. No insulator layer is included. A silicon layer 172, which has a (h k l) crystal orientation, is formed over substrate 170.

[0058] This substrate can then be processed to formed semiconductor regions of different crystal orientations as shown in Figures 9b and 9c. For example, any of the embodiments shown in Figures 5, 6 or 7 can be used to form regions 174 and 176 of different crystal orientations. Figure 9b shows an embodiment made by a process similar to that of Figure 5, and Figure 9c shows an embodiment made by a process similar to that of Figure 6. The different crystal orientation regions 174 and 176 can be separated by any isolation technique. Shallow trench isolation 178 is shown. As described above, and as shown in the embodiments of Figures 9b and 9c, p-channel transistors 124 can be formed in the regions 112 with (h k l) crystal orientation and n-channel transistors 122 can be formed in the regions 110 with (h' k' l') crystal orientation.

[0059] Although particular embodiments of the invention have been described in detail, it is understood that the invention is not limited correspondingly in scope, but includes all changes, modifications, and equivalents coming within the spirit and terms of the claims appended hereto. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense.

WHAT IS CLAIMED IS:

1. A silicon-on-insulator chip comprising:

an insulator layer;

a first silicon island with a surface of a first crystal orientation, the first silicon island overlying the insulator layer; and

a second silicon island with a surface of a second crystal orientation, the second silicon island overlying the insulator layer.

2. The silicon-on-insulator chip of claim 1 and further comprising a first transistor of a first conduction type formed on the first silicon island, and a second transistor of a second conduction type formed on the second silicon island.

3. The silicon-on-insulator chip of claim 2 wherein the first crystal orientation is (110) and the first transistor is a p-channel transistor, and wherein the second crystal orientation is (100) and the second transistor is a n-channel transistor.

4. The silicon-on-insulator chip of claim 2 wherein the first crystal orientation is (023) and the first transistor is a p-channel transistor, second crystal orientation is (100) and the second transistor is a n-channel transistor.

5. The silicon-on-insulator chip of claim 1 wherein the first silicon island comprises a plurality of silicon layers, each with a different crystal orientation.

6. The silicon-on-insulator chip of claim 5 wherein the plurality of silicon layers comprises a (110) silicon layer overlying a (100) silicon layer.

7. The silicon-on-insulator chip of claim 6 wherein the (110) silicon layer has a thickness of about 10 to about 500 angstroms.

8. The silicon-on-insulator chip of claim 1 wherein the first and second silicon islands each have a thickness in the range of about 10 angstroms to about 1000 angstroms.

9. The silicon-on-insulator chip of claim 1 wherein the first and second silicon islands have different thicknesses.

10. The silicon-on-insulator chip of claim 1 wherein the first and second silicon islands each have rounded or faceted corners.

11. The silicon-on-insulator chip of claim 1 wherein the insulator layer comprises a dielectric.

12. The silicon-on-insulator chip of claim 11 wherein the insulator layer comprises a crystalline dielectric.

13. The silicon-on-insulator chip of claim 1 wherein the insulator layer has a crystalline layer at the interface with the silicon islands.

14. The silicon-on-insulator chip of claim 1 wherein the insulator layer comprises silicon oxide.

15. The silicon-on-insulator chip of claim 1 wherein the insulator layer comprises aluminum oxide.

16. A silicon-on-insulator chip comprising:

an insulator layer;

a first silicon island with a surface of the (110) crystal orientation, the first silicon island overlying the insulator layer; and

a second silicon island with a surface of the (100) crystal orientation, the second silicon island overlying the insulator layer.

17. The silicon-on-insulator chip of claim 16 and further comprising a p-channel transistor formed on the first silicon island, and a n-channel transistor formed on the second silicon island.

18. The silicon-on-insulator chip of claim 16 wherein the first and second silicon islands each have a thickness in the range of about 10 angstroms to about 1000 angstroms.

19. The silicon-on-insulator chip of claim 16 wherein the first and second silicon islands have different thicknesses.

20. The silicon-on-insulator chip of claim 16 wherein the first and second silicon islands each have rounded or faceted corners.

21. The silicon-on-insulator chip of claim 16 wherein the insulator layer comprises a crystalline dielectric.

22. The silicon-on-insulator chip of claim 16 wherein the insulator layer has a crystalline layer at the interface with the first and second silicon islands.

23. The silicon-on-insulator chip of claim 16 wherein the insulator layer comprises silicon oxide.

24. The silicon-on-insulator chip of claim 16 wherein the insulator layer comprises aluminum oxide.

25. A method of forming silicon-on-insulator chip, the method comprising:

providing a silicon-on-insulator substrate including a silicon layer of a first crystal orientation overlying an insulator layer with a crystalline surface, the silicon layer including a first and a second region;

forming an amorphous silicon region over the second region of the silicon layer; and

recrystallizing the amorphous silicon region to form a region with a second crystal orientation.

26. The method of claim 25 and further comprising, after the recrystallizing the amorphous silicon region:

forming a first silicon island of the first crystal orientation and a second silicon island of the second orientation; and

forming a transistor of the first conduction type on the first silicon island and a transistor of the second conduction type on the second silicon island.

27. The method of claim 25 wherein the first crystal orientation is (110) and the second crystal orientation is (100) and wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

28. The method of claim 25 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

29. The method of claim 25 wherein the insulator layer comprises aluminum oxide.

30. The method of claim 29 wherein the aluminum oxide has a crystal orientation of (0, 1, -1, 2).

31. The method of claim 25 wherein the silicon layer has a thickness in the range of about 10 angstroms to about 500 angstroms.

32. A method of forming semiconductor device, the method comprising:

providing a workpiece including a first silicon layer of a first crystal orientation overlying a second silicon layer of a second crystal orientation, the second silicon layer overlying a semiconductor layer; and

removing a portion of the first silicon layer to expose the second silicon layer in a predetermined region.

33. The method of claim 32 wherein the semiconductor device comprises a silicon-on-insulator device, and wherein the insulator layer overlies a semiconductor substrate.

34. The method of claim 33, further comprising:

forming a first silicon island with a surface of the first crystal orientation and a second silicon island with a surface of the second orientation; and

forming a transistor of the first conduction type on the first silicon island and a transistor of the second conduction type on the second silicon island.

35. The method of claim 34 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

36. The method of claim 35 wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

37. The method of claim 33 wherein the first silicon layer has a thickness in the range of about 10 angstroms to about 100 angstroms.

38. The method of claim 33 wherein the second silicon layer has a thickness in the range of about 10 angstroms to about 1000 angstroms.

39. The method of claim 33 wherein the insulator layer comprises a dielectric.

40. The method of claim 33 wherein the insulator layer comprises silicon oxide.

41. The method of claim 33, wherein the first silicon layer is formed by epitaxial growth of silicon on the second silicon layer, the method further comprising:

forming a first silicon island with a surface of the first crystal orientation and second silicon island with a surface of the second orientation; and

forming a transistor of the first conduction type on the first silicon island and a transistor of the second conduction type on the second silicon island.

42. The method of claim 41 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

43. The method of claim 42 wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

44. The method of claim 32 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

45. A method of forming silicon-on-insulator chip, the method comprising:

providing a silicon-on-insulator substrate including a first silicon layer of a first crystal orientation overlying a second silicon layer of a second crystal orientation, said second silicon layer overlying an insulator layer;

amorphosizing a portion of the first silicon layer in a predetermined region to form an amorphous silicon region; and

recrystallizing the amorphous silicon region to form a region with a second crystal orientation.

46. The method of claim 45, further comprising:

forming a first silicon island with a surface of the first crystal orientation and a second silicon island with a surface of the second orientation; and

forming a transistor of a first conduction type on the first silicon island and a transistor of a second conduction type on the second silicon island.

47. The method of claim 46 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

48. The method of claim 47 wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

49. The method of claim 45 wherein the first silicon layer has a thickness in the range of about 10 angstroms to about 100 angstroms.

50. The method of claim 45 wherein the second silicon layer has a thickness in the range of about 10 angstroms to about 1000 angstroms.

1 51. The method of claim 45 wherein the insulator layer comprises a dielectric.

1 52. The method of claim 45 wherein the insulator layer comprises silicon oxide.

53. A method of forming silicon-on-insulator chip, comprising:

providing a silicon-on-insulator substrate including a silicon layer of a first crystal orientation overlying an insulator layer with a crystalline surface, the silicon layer including a first region and a second region;

removing a portion of the silicon layer in the second region to expose the insulator layer; and

performing epitaxial growth of silicon of a second crystal orientation on the insulator layer.

54. The method of claim 53 further comprising, after performing the epitaxial growth of silicon:

forming a first silicon island of the first crystal orientation and a second silicon island of the second orientation; and

forming a transistor of the first conduction type on the first silicon island and a transistor of the second conduction type on the second silicon island.

55. The method of claim 54 wherein the first crystal orientation is (110) and the second crystal orientation is (100).

56. The method of claim 55 wherein the transistor of the first conduction type is a p-channel transistor and the transistor of the second conduction type is a n-channel transistor.

57. The method of claim 53 wherein the insulator layer comprises of aluminum oxide.

58. The method of claim 57 wherein the aluminum oxide has a crystal orientation of (0, 1, -1, 2).

59. The method of claim 53 wherein the silicon layer has a thickness in the range of about 10 angstroms to about 500 angstroms.