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Description

Method for minimizing the vapor deposition of tungsten oxide during the selective side wall oxidation of tungsten-silicon gates

The invention relates in general terms to the field of fabrication of metallization structures, in particular gate structures, which include at least one layer of polycrystalline silicon and at least one tungsten layer. The invention relates in particular to a selective oxidation method for a metallization structure of this type, in accordance with the preamble of patent claim 1.

As part of the ongoing reduction in the size of MOS transistors, tungsten is increasingly being used as a constituent of the gate stack. Tungsten has considerable advantages as a gate material compared to tungsten silicide, which is likewise already in widespread use. The lower resistivity of tungsten compared to tungsten silicide makes it possible to reduce the resistance of the gate and thereby achieve improved electrical properties of the transistors. On account of the lower resistivity, it is also possible to significantly reduce the height of the layered gate stack, with the result that the various filling and etching steps are considerably simplified, since the aspect ratio (ratio of the height of gates to the distance between adjacent gates) is reduced.

During the fabrication of the multilayer gate stack, first of all it is usual for a gate oxide layer, a polycrystalline silicon layer, a tungsten nitride layer, a tungsten layer and a silicon nitride layer to be applied to a silicon substrate. Then, individual gate regions, which are intended to be located in each case above a channel of a MOS transistor, are defined

by photolithography and vertical etching. To electrically insulate the etched side walls of the gate stacks and to anneal etching damage, suitable insulation layers have to be applied to the side walls. An SiO_2 layer, which is produced by thermal oxidation, is most suitable for the polycrystalline silicon layer. At the same time, however, it is necessary to prevent oxidation of the tungsten layer, since experience has shown that this oxidation is not restricted to the surface, but also continues in the lateral direction in the layer and thereby produces high-impedance tungsten oxide, with the result that the electrical functionality of the gate is impeded.

Various methods for producing side walls of a gate electrode which includes a tungsten layer have become known.

US-A-6,165,883 describes a method which is based on selective oxidation of the gate stack. This method is explained in more detail below with reference to figures 1A to 1C in the drawing.

A gate oxide layer 1 is formed on a silicon substrate 10 by thermal oxidation, and then a polycrystalline silicon layer 2, a barrier layer 3 of tungsten nitride or titanium nitride, a tungsten layer 4 and a silicon nitride layer 5 are deposited on the gate oxide layer. Then, the silicon nitride layer 5 is patterned in order to define the gate regions, so that the structure shown in fig. 1A is obtained for a gate region. The mesa-etched structure 5 of the silicon nitride layer subsequently serves as an etching mask. Then, in a vertical etching step, the layers 1 to 4 are removed in the regions between the gate structures, so that only individual, defined gate regions of the layer stack remain in position. Next, selective oxidation in an atmosphere containing water and hydrogen is carried out

at 800°C, with silicon oxide layers 6 being formed only on the silicon substrate 10 and at the side walls of the polycrystalline silicon layer 2. By contrast, the tungsten layer 4 is not oxidized. The structure which is thereby obtained is illustrated in fig. 1B. Finally, a silicon nitride layer 7 is applied as an insulating layer to the side walls of the silicon nitride layer 5, of the tungsten layer 4, of the tungsten nitride layer 3 and of the silicon oxide layer 6. As a result, the gate structure is now surrounded on all sides by electrically insulating side walls. For the sake of simplicity, the following process steps, which are explained in the abovementioned document, will not be considered in further detail in the present document.

To carry out the selective oxidation, it is important for a defined mixing ratio of the hydrogen/water mixture to be established in the region chamber. The pressure ratio of H_2O/H_2 which is set at the flow controllers of the reaction chamber, i.e. the corresponding concentration ratio which is set in the reaction chamber, is plotted against the process temperature in fig. 2. The figure shows reaction equilibrium curves, on which defined oxidation reactions are in equilibrium with the associated reduction reactions. The oxidation or reduction of tungsten is illustrated by the upper equilibrium curve, while the oxidation or reduction of silicon is characterized by the lower equilibrium curve. In both cases, starting from the respective equilibrium curve, a rise in the water vapor content and/or a fall in the process temperature lead/leads to equilibrium being lost in favor of the corresponding oxidation reaction. It is important for the process conditions wafer temperature and mixing ratio to be set in such a way that the operating point in the diagram shown in fig. 2 lies in the central region between the equilibrium curves illustrated.

However, for selective oxidation, which is carried out in accordance with fig. 1B with a view to forming the silicon oxide layers 6 by wet oxidation in a hydrogen-rich atmosphere, hitherto, there has still been considerable formation of tungsten oxide in the atmosphere which surrounds the gate region.

This tungsten oxide is volatile at the process temperatures and is deposited on the walls of the process chamber, where it is reduced to form metallic tungsten by the hydrogen. Since these deposits of tungsten, in the case of lamp-heated RTP (rapid thermal processing) installations, which are preferably used for selective oxidation, are therefore located on the quartz parts between the lamps and the wafer and, on account of their optical properties partially absorb the lamp radiation, they have a very considerable influence on the temperature homogeneity of the wafer and drastically impair this homogeneity. In addition, tungsten deposits may also be formed on the quartz parts in front of the pyrometers and may thereby have an adverse effect on the optical measurement of the wafer temperature. During processing under production conditions, i.e. repeated processing with the same process on large numbers of production wafers, the increasing deposition of tungsten leads to such rapid degradation of the layer thickness homogeneity above the wafer and from wafer to wafer that the process is not currently sufficiently stable for production applications.

Moreover, the loss of tungsten caused by the vapor deposition of tungsten oxide may cause damage to the electrical functionality of the interconnects. Furthermore, the redeposition of tungsten oxide, followed by reduction to form tungsten, may lead to the formation of undesirable conductive compounds and

therefore to short-circuiting of components on the wafer. These problems are not restricted to lamp-heated RTP installations, but rather occur in all conditioning installations which can be used for selective oxidation, for example including conventional furnaces. In the latter case, however, the deposition of tungsten oxide on the chamber walls and the subsequent reduction of this tungsten oxide to form tungsten does not constitute such a serious problem.

Accordingly, it is an object of the present invention to provide a method for the selective oxidation of a metallization structure, in particular of a gate structure, which includes at least one silicon layer, which is to be oxidized, and at least one tungsten layer, which is not to be oxidized, in which method vapor deposition of tungsten oxide from the atmosphere surrounding the metallization structure does not occur at all or occurs only to a greatly reduced extent.

This object is achieved by the characterizing features of patent claim 1. Advantageous embodiments and refinements of the method according to the invention are described in the subclaims.

The present invention describes an improved procedure for the selective oxidation of a metallization structure which includes at least one polycrystalline silicon layer and at least one tungsten layer, the metallization structure being acted on by a mixture of hydrogen and water in a manner which is known per se in a treatment step in which heat is supplied and, during this step, being selectively oxidized. A significant aspect of the procedure according to the invention is that the metallization structure is acted on by a nonaqueous hydrogen-containing substance, in particular pure hydrogen or a hydrogen/inert gas mixture, before and, if appropriate, after this treatment step. As

tests have shown, this measure makes it possible to considerably reduce the vapor deposition of tungsten oxide, and in some cases even to eliminate it altogether. In this context, it is advantageous, although not absolutely imperative, for hydrogen or the hydrogen/inert gas mixture also to be applied after the treatment step. By way of example, the hydrogen/inert gas mixture may be a hydrogen/nitrogen mixture.

The temperature which prevails at or in the immediate vicinity of the metallization structure which is to be treated is referred to in the text which follows as the wafer temperature. During the treatment step with the hydrogen/water mixture, the supply of heat is used to set a wafer temperature, which is referred to below as the process temperature.

The extent to which the vapor deposition of tungsten oxide can be reduced is dependent on the implementation of further measures, such as the setting of defined wafer temperatures, rise and fall times (ramp times) for the wafer temperature and the hydrogen/water concentration ratio.

For example, it is advantageous if, during a first section of a treatment with the hydrogen-containing substance before the treatment step with the hydrogen/water mixture, the supply of heat is set in such a way that the wafer temperature is increased from a first temperature T_1 to a second temperature T_2, the first temperature preferably lying in a range between room temperature and 200°C, and the second temperature preferably also lying in a range between 700°C and 900°C. In this case, it is possible for the wafer temperature initially to be kept constant at the first temperature and then to be increased continuously or in steps to the second temperature.

A further advantageous measure of the method consists in, during a section of the treatment step with the hydrogen/water mixture, setting of the supply of heat in such a way that said wafer temperature is increased from a defined temperature to a process temperature. In this case, it is possible for the wafer temperature initially to be kept constant at the defined temperature and then to be increased continuously or in steps to the process temperature. The defined temperature may be formed by the abovementioned second temperature, which lies in a range between 700°C and 900°C, and the process temperature may be formed by a third temperature T_3, which lies in a range between 900°C and 1100°C.

Irrespective of the method measure described in the previous section, it has proven advantageous for the wafer temperature during the treatment step with the hydrogen/water mixture to be set to a process temperature in a range between 900°C and 1100°C.

Furthermore, during a second section of the treatment with the hydrogen-containing substance after the treatment step with the hydrogen/water mixture, the supply of heat may be set in a such a way that the wafer temperature is reduced continuously or in steps from a process temperature to a lower temperature. The process temperature may in this case be formed by the abovementioned third temperature T_3, which lies in a range between 900°C and 1100°C, and the lower temperature may be a temperature which lies below the abovementioned second temperature T_2 and therefore lies in a range between 300°C-600°C.

Before and, if appropriate, after the application of the hydrogen-containing substance, it is also possible to carry out a treatment with an inert gas, in particular pure nitrogen.

It should be ensured that, during the treatment step with the hydrogen/water mixture, at least a state in the vicinity of a reaction equilibrium between an oxidation reaction and a reduction reaction is adopted. Preferably, however, the water content in the hydrogen/water mixture supplied and the process temperature are selected in such a manner that in the pair of reaction equations

$$W + 3H_2O \rightleftarrows WO_3 + 3H_2$$

the reaction equation

$$WO_3 + 3H_2 \rightarrow W + 3H_2O$$

has a greater, in particular much greater reaction rate.

Furthermore, it has proven advantageous if the water content in the hydrogen/water mixture is below 20% for the duration of the treatment section and, at the same time, a process temperature is selected in such a manner that the above conditions with regard to the chemical reactions are maintained.

In principle, the method according to the invention can be carried out in any conditioning installation which includes a reaction chamber which has an inlet opening and an outlet opening, it being possible for substrates which include the metallization structures to be arranged in the reaction chamber in such a manner that process gases can flow past the substrates from the inlet opening to the outlet opening.

The method may, for example, be carried out in a lamp-heated RTP (rapid thermal processing) installation. This installation has a reaction chamber with an inlet

opening in which the process gases can be supplied in a controlled manner to the reaction chamber, for example by means of mass flow controllers. The process gases flow past the silicon wafers to an outlet opening, through which they can be sucked back out of the reaction chamber by means of a vacuum or a pump. The wafer is heated by being irradiated with a high-power lamp.

However, the method may also be employed in a conventional furnace installation, such as for example a vertical or horizontal tubular furnace.

Particularly good results are achieved if all the additional measures which have been described above in connection with the wafer temperature and the temperature ramps are carried out. However, it is also possible to dispense with some of these measures if the improvements which they are able to bring about no longer justify the expense of executing these measures.

It has been found that the vapor deposition of tungsten oxide is reduced very considerably by the newly developed procedure and therefore, in particular in lamp-heated RTP installations, there are no deposits which impair operation of the installation, and consequently the process stability can be considerably increased. When the selective oxidation is carried out in conventional furnace installations, the method according to the invention avoids harmful deposits of tungsten oxide on the semiconductor wafer itself and the structures formed thereon.

The method according to the invention and a preferred embodiment are explained in more detail below with reference to the figures of the drawing, in which:

figs. 1A-C show individual method steps

for a gate structure according to the prior art which includes a tungsten layer;

fig. 2 shows a diagram illustrating the reaction mechanisms and equilibria;

fig. 3 shows a preferred procedure for the method according to the invention.

Fig. 3 shows an example of a procedure in which a treatment with pure hydrogen gas (H_2) is carried out immediately before and after the water/hydrogen gas mixture has been supplied.

The wafer temperature plotted on the ordinate is not linear.

First of all, at a very low first temperature T_1, for example 50°C (the actual temperature cannot be determined by conventional pyrometer measurement), nitrogen is passed through the reaction chamber, in order to remove the oxygen from the reaction chamber. The first temperature T_1 may lie in the range between room temperature and 200°C.

This is followed by a treatment with pure hydrogen gas. Therefore, hydrogen gas is supplied through the inlet opening of the reaction chamber, initially at a constant first temperature T_1, and during the ongoing hydrogen treatment the temperature is continuously increased over a ramp to the second temperature T_2 of, for example, 800°C.

Then, a hydrogen/water mixture is fed to the reaction chamber, it being possible for the flow controllers to be set in such a way that an atmosphere with a water content of, for example, 14% by volume is established

in the reaction chamber. The process temperature is initially kept constant at the second temperature T_2 of 800°C, but is then increased continuously, over a second temperature ramp, to the third temperature T_3 of, for example, 1050°C. At this third temperature T_3 (process temperature), the treatment with the hydrogen/water mixture is carried out in the manner described above, with an SiO_2 layer being formed on the side walls of the polycrystalline silicon layer 2 and, if appropriate, on the silicon substrate 10 (cf. fig. 1B).

This is followed by a further treatment with pure hydrogen gas, during which the wafer temperature is continuously reduced from the third temperature T_3 to a temperature which is lower than the second temperature T_2. After this treatment, nitrogen flows through the reaction chamber once again, and during this period the wafer temperature is reduced to a discharge temperature. A different inert gas may also be used instead of nitrogen.

A hydrogen/nitrogen mixture may also be used instead of the treatment with pure hydrogen gas immediately before and after the treatment with the hydrogen/water mixture. Other inert gas mixtures which contain hydrogen are also conceivable.

As an alternative to the continuous temperature ramps which are illustrated, it is also possible for the temperature to be changed discontinuously, in steps.

The process time for the treatment with the hydrogen/water mixture is typically 30-60 seconds, while the temperature ramp times are, for example, in the range from 10-50°C/s. Other times may also be used, depending on the choice of the other process parameters, in particular of the temperature and of the

water content.

Patent Claims

1. A method for the selective oxidation of a metallization structure, in particular of a gate structure, which includes at least one silicon layer, which is to be oxidized and in particular is in polycrystalline form, and at least one tungsten layer, which is not to be oxidized, in which method
- the metallization structure is acted on by a mixture of hydrogen and water in a treatment step in which heat is supplied,
wherein
- the metallization structure is acted on by a nonaqueous hydrogen-containing substance, in particular pure hydrogen or a hydrogen/inert gas mixture, before and, if appropriate, after the treatment step.

2. The method as claimed in claim 1, wherein
- during a first section of the treatment with the hydrogen-containing substance before the treatment step, the supply of heat is set in such a way that the temperature of the metallization structure (wafer temperature) is increased from a first temperature (T_1) to a second temperature (T_2).

3. The method as claimed in claim 1 or 2, wherein
- during a section of the treatment step the supply of heat is set in such a way that the temperature of the metallization structure (wafer temperature) is increased from a defined temperature, in particular the second temperature (T_2), to a process temperature, in particular a third temperature (T_3).

4. The method as claimed in one of the preceding claims, wherein
- during a second section of the treatment with the hydrogen-containing substance after the treatment step, the supply of heat is set in such a way that the

temperature of the metallization structure is reduced continuously from a process temperature, in particular the third temperature (T_3), to a lower temperature, in particular the first temperature (T_1).

5. The method as claimed in one of the preceding claims, wherein
- the water content in the mixture is below 20% for the duration of the treatment step.

6. The method as claimed in one of claims 2 to 5, wherein
- the first temperature (T_1) is higher than room temperature and lower than 200°C.

7. The method as claimed in one of claims 2 to 6, wherein
- the second temperature (T_2) lies in the range from 700°C-900°C.

8. The method as claimed in one of claims 1 to 7, wherein
- at least during one section of the treatment step, the supply of heat is set in such a way that the temperature at or in the immediate vicinity of the metallization structure, in particular the third temperature (T_3), is in the range from 900°C-1100°C.

9. The method as claimed in one of the preceding claims, wherein
- the metallization structure is treated with an inert gas before and, if appropriate, after it has been acted on by the hydrogen-containing substance.

10. The method as claimed in one of the preceding claims, wherein
- during the treatment step the water content and the temperature are selected in such a manner that in the

pair of reaction equations

$$W - 3H_2O \rightleftarrows WO_3 + 3H_2$$

the reaction equation

$$WO_3 + 3H_2 \rightarrow W + 3H_2O$$

has the greater reaction rate.

11. The method as claimed in one of the preceding claims, wherein
- it is carried out in a reaction chamber which has an inlet opening and an outlet opening, and
- substrates which include the metallization structures are arranged in the reaction chamber in such a manner that process gases can flow past the substrates from the inlet opening to the outlet opening.

12. The method as claimed in one of the preceding claims, wherein
- the method is carried out in a conditioning device, in particular in a lamp-heated rapid thermal processing or rapid thermal annealing (RTP or RTA) device.

13. A method for fabricating a metallization structure, in particular a gate structure of a MOS component, having at least one silicon layer, in particular a polycrystalline silicon layer, and at least one tungsten layer, a selective oxidation method as claimed in one or more of the preceding claims being carried out during the fabrication.