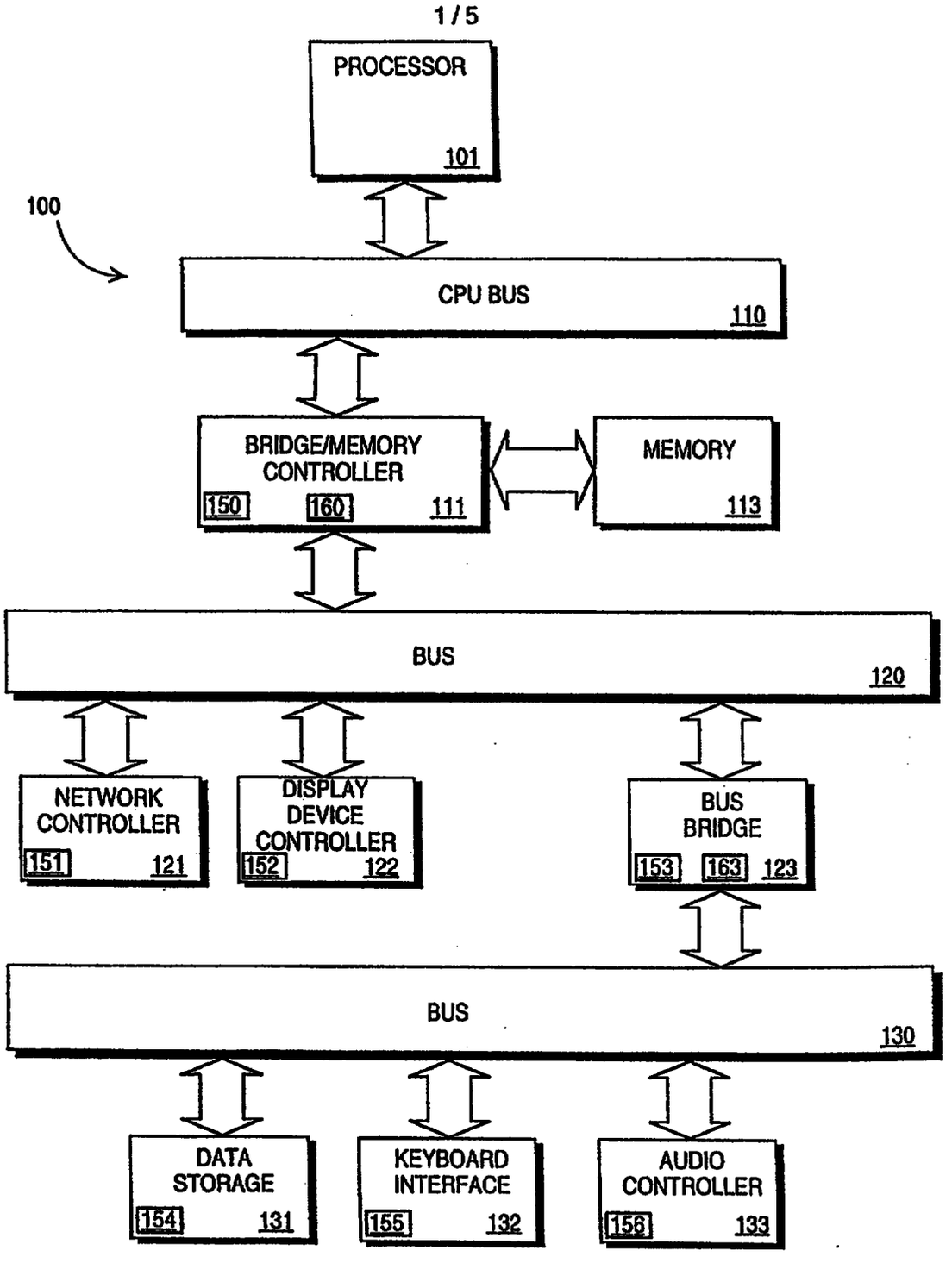

PROCESSOR
101
100
CPU BUS
110
BRIDGE/MEMORY CONTROLLER
150
160
111
MEMORY
113
BUS
120
NETWORK CONTROLLER
151
121
DISPLAY DEVICE CONTROLLER
152
122
BUS BRIDGE
153
163
123
BUS
130
DATA STORAGE
154
131
KEYBOARD INTERFACE
155
132
AUDIO CONTROLLER
156
133

FIG. 1

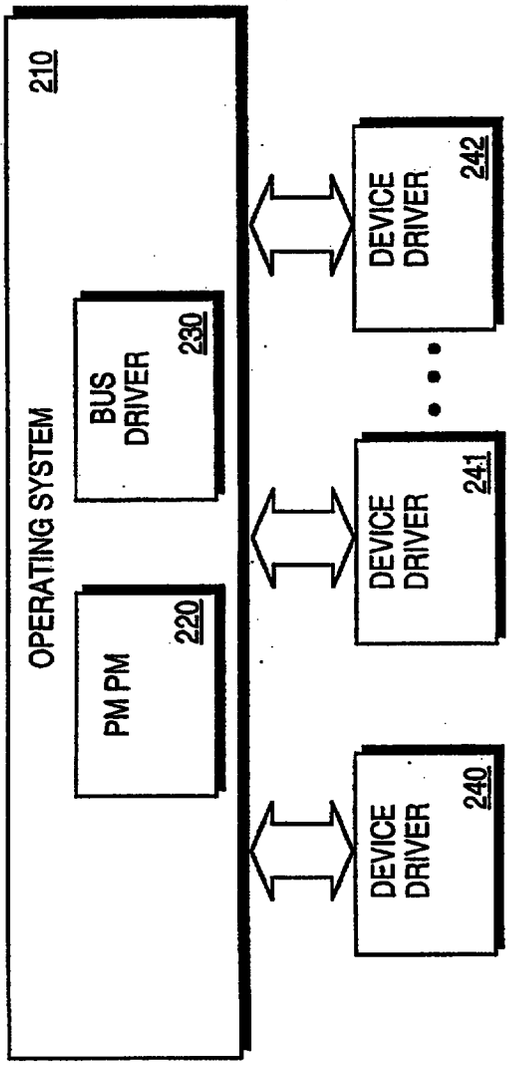

OPERATING SYSTEM
210
PM PM
220
BUS DRIVER
230
DEVICE DRIVER
240
DEVICE DRIVER
241
DEVICE DRIVER
242

FIG. 2

ORIGINATING DEVICE POWER STATE	I/O BUS POWER STATE	POSSIBLE FUNCTION POWER STATES
D0	B0	D0, D1, D2, D3
D1	B1	D1, D2, D3
D2	B2	D2, D3
D3 ($D3_{HOT}$, $D3_{COLD}$)	B3	D3

FIG. 3

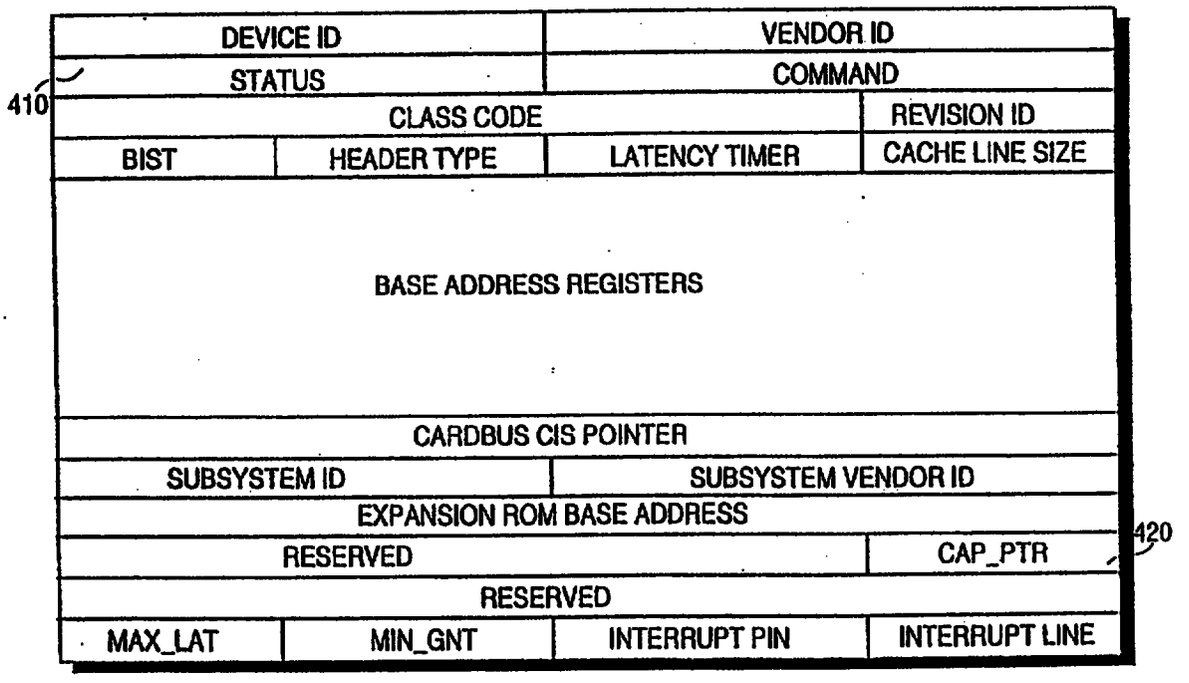

DEVICE ID
VENDOR ID
STATUS
COMMAND
410
CLASS CODE
REVISION ID
BIST
HEADER TYPE
LATENCY TIMER
CACHE LINE SIZE
BASE ADDRESS REGISTERS
CARDBUS CIS POINTER
SUBSYSTEM ID
SUBSYSTEM VENDOR ID
EXPANSION ROM BASE ADDRESS
RESERVED
CAP_PTR
420
RESERVED
MAX_LAT
MIN_GNT
INTERRUPT PIN
INTERRUPT LINE

FIG. 4

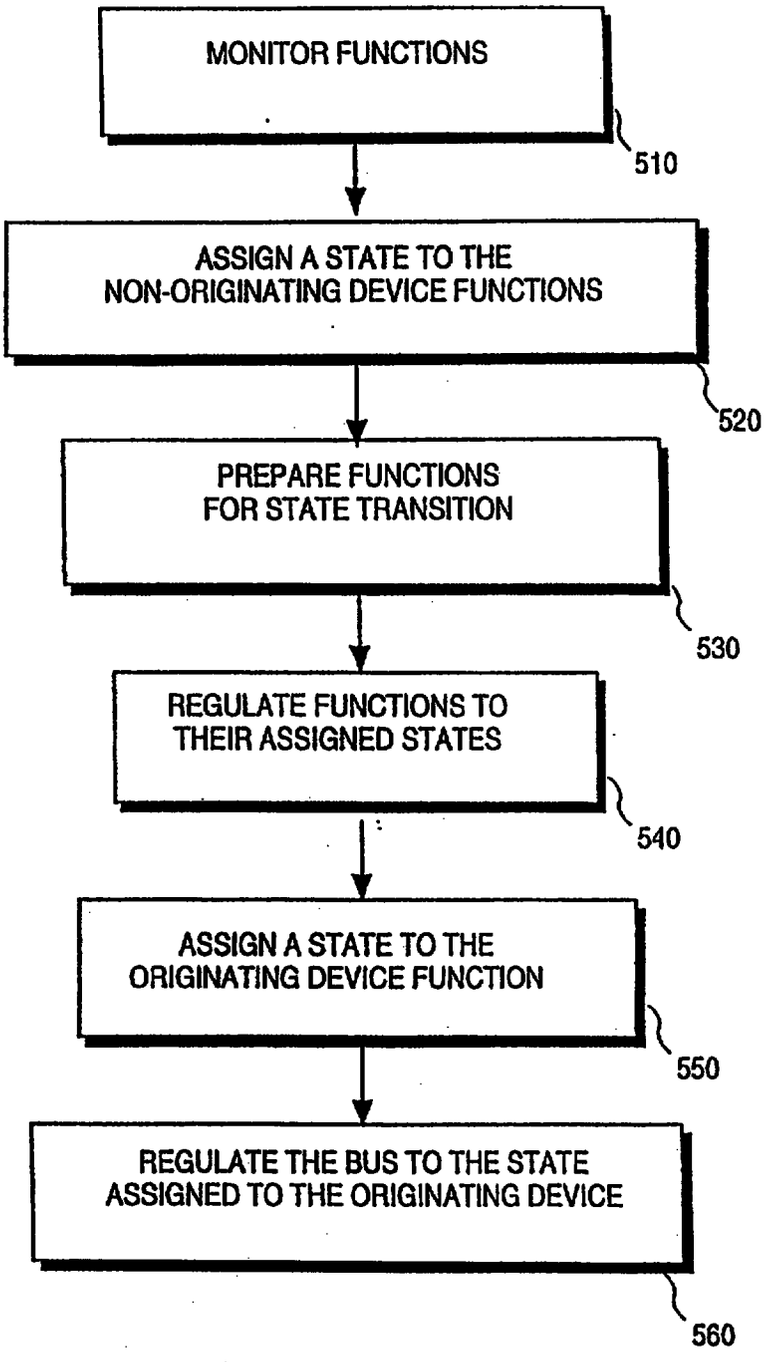

MONITOR FUNCTIONS
510
ASSIGN A STATE TO THE NON-ORIGINATING DEVICE FUNCTIONS
520
PREPARE FUNCTIONS FOR STATE TRANSITION
530
REGULATE FUNCTIONS TO THEIR ASSIGNED STATES
540
ASSIGN A STATE TO THE ORIGINATING DEVICE FUNCTION
550
REGULATE THE BUS TO THE STATE ASSIGNED TO THE ORIGINATING DEVICE
560

FIG. 5