USE OF A SELECTIVE HARD MASK FOR THE INTEGRATION OF DOUBLE DIFFUSED DRAIN MOS DEVICES IN DEEP SUB-MICRON FABRICATION TECHNOLOGIES

ABSTRACT

A process for integrating the fabrication of double diffused drain (DDD) MOSFET devices with the fabrication sub-micron CMOS devices, has been developed. The process features formation of an insulator hard mask shape on an underlying polysilicon gate structure shape in the DDD MOSFET region, while only a polysilicon gate structure shape is formed in the CMOS device region. High energy ion implantation procedures are employed to form the deep source/drain regions of the DDD MOSFET devices with the insulator hard mask shape preventing the high energy implantation procedure from disturbing the underlying channel region. An anneal procedure used activate and drive - in the implanted ions in the deep source/drain region of the DDD MOSFET device is followed by formation of the shallower source/drain regions of the sub-micron CMOS devices.

FIG. 9