New Fuse Structure

[0001] This application claims the benefit of U.S. Provisional Application No. 60/583,637, filed on June 29, 2004, entitled "E-Fuse Structure Design in Electrical Programmable Redundancy for Embedded Memory Circuit," which application is hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] This invention relates generally to an electrical fuse and more particularly to an electrical fuse having a vertical structure.

BACKGROUND

[0003] In the semiconductor industry, fuse elements are widely used features in integrated circuits for a variety of purposes, such as improving manufacturing yield or customizing a generic integrated circuit. For example, by replacing defective circuits on a chip with redundant circuits on the same chip, manufacturing yields can be significantly increased. Replacing defective circuits is especially useful for improving manufacturing yield of the memory chips since memory chips consist of a lot of identical memory cells and cell groups. By selectively blowing fuses within an integrated circuit that has multiple potential uses, a generic integrated circuit design may be economically manufactured and adapted to a variety of custom uses.

[0004] There are two different ways to disconnect fuses: in one way, the disconnection is carried out by the action of a laser beam, and the fuse is referred to as a laser fuse. In another way, the disconnection is carried out by electrical destruction resulting from the production of heat. The fuse is referred as an electrical fuse, or E-fuse.

[0005] Laser programmable redundancy has been widely used in large-scale memory devices. However, the laser repair rate in various structures such as in lower level metal layers is low and the process is complex. Figure 1 illustrates a laser fuse formed close to the surface of a chip. Device 6 is a laser fuse. Oxide 5 covers the fuse 6. If the fuse 6 is to be burned out from top of the oxide 5 by laser, the thickness T of the oxide 5 has to be within a certain range, for example, between about 0.1kÅ to about 4.0kÅ. Therefore, an extra mask is needed to form the opening 4, and the process has to be precisely controlled. If a laser fuse 10 is in a lower level layer deep in a chip, as shown in Figure 2, the opening 8 will be deeper, while the thickness T of the oxide still has to be controlled precisely, which increases the complexity significantly and decreases the repairable rate.

[0006] In addition, as technology is scaling down to 0.13μm or below, copper is implemented as interconnects or power lines. Copper is a material with high current density tolerance and is not easily burned out by using a laser gun. Furthermore, the combination of copper plus low-k material 12 (used as inter-layer dielectrics) is becoming a trend to improve RC delay. However, low-k material 12 cracks easily when etching the opening 8 in Figure 2. This decreases the device reliability and increases the production cost.

[0007] Electrical fuses were developed to improve repairable rates. Figure 3 illustrates a conventional electrical fuse 13. A polysilicon strip 15 is formed and patterned. The regions 14 and 16 of the polysilicon strip 15 are doped with p+ and n+ dopant. The central region 18 is left un-doped. A silicide 20 is formed over the polysilicon strip 15. Before the fuse 13 is burned out, its resistance is mainly determined by the resistance of the silicide 20 so that the resistance is low. When a predetermined programming potential is applied across the silicide layer 20 from nodes 22 and 24, the silicide layer 20 agglomerates to form an electrical discontinuity. Therefore the

resistance of the fuse 13 is mainly determined by the underlying polysilicon strip 15 so that the resistance is significantly increased. The central un-doped region 18 makes the fuse resistance higher. The electrical fuse shown in Figure 3 typically has a higher repairable rate than a laser fuse. However, the repairable rate is still not satisfactory. Additionally, the fuse of Figure 3 is formed laterally and occupies more layout space.

[0008] There are several disadvantages faced by conventional methods of making fuses. Firstly, the repairable rate is typically low. Secondly, the additional masking layer needed for laser repair incurs higher costs. The process is also more complex with higher uncertainty. Thirdly, the structure design is not flexible. Fuses typically have to be designed in higher layers, as it is harder to form deep laser trenches through to lower layers. Therefore, new methods of designing e-fuses are needed.

SUMMARY OF THE INVENTION

[00091 The preferred embodiment of the present invention presents a method of forming an electrical fuse having a vertical structure.

[0010] In accordance with one aspect of the present invention, an electrical fuse is disclosed, which comprises a first-layer conductive line is formed on a base material, a second conductive layer and a via is formed over the first-layer conductive line. The via preferably comprises a barrier layer and a conductive material. A second-layer conductive line is formed over the via. A first external pad is formed coupling the first-layer conductive line. A second external pad is formed coupling the second-layer conductive line. The via, first conductive line and second conductive line are adapted to be an electrical fuse.

[0010a] In another aspect of the present invention, a semiconductor device is disclosed, which comprises a semiconductor device comprising: a burned-out electrical fuse comprising:
a first conductive layer, a second conductive layer, and a via coupled between the first conductive layer and the second conductive layer and adapted to be a fuse.

[0010b] In yet another aspect of the present invention, a semiconductor device is disclosed, which comprises a semiconductor device comprising: an electrical circuit; a redundant circuit having a redundant design of the electrical circuit; a first conductive layer, a second conductive layer; and a first via coupled between the first conductive layer and the second conductive layer wherein one of the first and second conductive layers is coupled to the redundant circuit and wherein the first via, the first conductive layer and the second conductive layer are adapted to be an electrical fuse.

[0011] In accordance with another aspect of the present invention, copper is used in the via, the first-layer conductive line, and the second conductive line. Single or dual damascene processes are used to form the via, the first-layer copper line and the second-layer copper line.

[0012] The vertical structure of the preferred embodiment is suitable to be formed in any layer and saves layout space. The embodiments of the present invention have several advantageous features. Firstly, higher repairable rates can be achieved since the burn out process is easier to control and more reliable. Secondly, fewer masking layers are required, therefore reducing costs. Thirdly, the fuse may reside in any region of the inter layer vias for cell size reduction. This provides a flexible structure for circuit design.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0014] Figure 1 illustrates a laser fuse formed close to the surface of a chip;

[0015] Figure 2 illustrates a laser fuse formed deep in a chip;

[0016] Figure 3 illustrates a conventional electrical fuse;

[0017] Figures 4 through 7 are cross-sectional views of intermediate stages in the making of a preferred embodiment of the present invention;

[0018] Figures 8 through 12 are cross-sectional views of intermediate stages in the making of a preferred embodiment of the present invention using a damascene process;

[0019] Figure 13 illustrates three vias stacked;

[0020] Figures 14a and 14b illustrates borderless and non-borderless vias;

[0021] Figures 15a and 15b illustrate an application of the preferred embodiment of the present invention;

[0022] Figures 16 through 18 illustrate another preferred embodiment of the present invention; and

[0023] Figures 19a and 19b illustrate burned out fuses.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0024] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0025] The preferred embodiments of the present invention present a novel method of forming e-fuses. A via connecting a lower-layer conductive line and an upper-layer conductive line is adapted to be an e-fuse. The e-fuse can be burned out by applying a voltage on external pads that are coupled to the lower-layer conductive line and the upper-layer conductive line. Throughout the description, conductive lines are also referred to as conductive layers.

[0026] Figures 4 through 7 are cross-sectional views of intermediate stages in the making of a preferred embodiment of the present invention. It is to be noted that the cross-sectional views are taken in a plane perpendicular to the length direction of the conductive lines formed. Therefore, conductive lines appear to be rectangles. Figure 4 illustrates the formation of a lower-layer conductive line 44 on a base material 40. The lower-layer conductive line 44 is preferably a metal comprising tungsten, aluminum, copper, silver, gold, alloy thereof, compounds thereof, and combinations thereof. It can also be formed of other materials such as doped polysilicon. Base material 40 is typically an inter-layer dielectric (ILD) also sometimes known as a pre-metal dielectric (PMD) or an inter-metal dielectric (IMD) layer. It can also be formed of other non-conductive materials such as a contact etching stop layer (CESL).

[0027] An ILD layer 42 is formed beside the low-layer conductive line 44. The ILD layer 42 is preferably silicon dioxide deposited using, e.g., tetraethyl orthosilicate (TEOS), chemical vapor deposition (CVD), plasma enhanced CVD (PECVD), low pressure CVD (LPCVD), or other well-known deposition techniques. ILD 42 can also be other materials such as phospho-silicate glass (PSG) or other known materials. Typically, ILD layer 42 has a low dielectric constant (K value) so that the parasitic capacitance between conductive lines is reduced.

[0028] Figure 4 also shows an etching stop layer (ESL) 46 formed on the lower-layer conductive line 44. The ESL 46 is preferably a dielectric formed of an oxide or other materials such as silicon nitride. An ILD 48 is formed on the ESL 46. The ILD 48 provides insulation between the lower-layer metal line 44 and overlying conductive lines that will be formed subsequently.

[0029] Figure 5 illustrates a via opening 50 formed in the ILD 48 and ESL 46. A photo resist material (not shown) is formed and patterned over the ILD 48. The via opening 50 is formed in the ILD 48 and stops at the ESL 46. The ELS 46 protects the underlying lower-layer conductive line 44 when the ILD 48 is etched. Next, the exposed portion of ESL 46 is etched. Because the ESL 46 is quite thin relative to the ILD 48, process control and end-point detection are much more closely controlled, thus limiting the likelihood of over-etching through the underlying lower-layer conductive line 44.

[0030] Figure 6 illustrates the device after via 54 is formed in the contact openings. In the preferred embodiment, via 54 is formed of tungsten, aluminum, copper, silver, gold, or combinations and other well-known alternatives. In other embodiments, it can be formed of doped polysilicon. Preferably, via 54 has a composite structure, including a barrier layer 52 formed of a material comprising titanium, titanium nitride, tantalum, tantalum nitride, silicon

carbide, silicon oxycarbide, combinations thereof and other layers. The barrier layer 52 prevents the via material diffusing into the ILD 48, which would cause device failure. The thickness of the barrier layer 52 is preferably between about 10Å to about 1000Å, more preferably about 300Å. Via 52 and lower-layer conductive line 44 share an interface 49.

[0031] An upper-layer conductive line 58 and an ILD 56 are then formed using the methods mentioned in previous paragraphs, as illustrated in Figure 7. The upper-layer conductive line 58 is in a layer higher than the layer in which the lower-layer conductive line 44 is formed. Interface 55 exists between via 54 and the upper-layer conductive line 58. Both lower-layer conductive line 44 and upper-layer conductive line 58 are coupled to external pads 59 and 61, respectively. External pads 59 and 61 are formed at the surface of the chip. The structure formed in previous steps results in an electrical fuse that is defined in a region comprising via 54, interfaces 49 and 55 and surrounding regions. By applying a voltage to external pads 59 and 61, a current flows through the fuse and a discontinuity is formed in the fuse region.

[0032] In another preferred embodiment, the conductive lines and via are formed of copper. Copper has better conductivity and can withstand higher current so that it is widely used for 0.13μm and below. However, it is hard to etch. Therefore a damascene process is used. Figures 8 through 12 are cross-sectional views of intermediate stages in the making of a preferred embodiment of the present invention using damascene process. Figure 8 illustrates the formation of a lower-layer copper line 64. It is formed by forming a trench in the ILD 60, depositing a barrier layer 62 in the trench, depositing copper, and performing a CMP to polish the copper to the surface of the trench.

[0033] A dual damascene process is preferably performed to form a via and an upper-layer copper line. As shown in Figure 9, a first etch stop layer 66, a first ILD 68, a second etch stop layer 70, a second ILD 72 and a hard mask 74 are formed. The materials and methods of forming these layers are known in the art. Figure 10 illustrates a first opening 76 formed down to the first etch stop layer 66. A second opening 78 is formed in the second ILD 72. Then the exposed portion of the first etch stop layer 66 is removed. The resulting structure is shown in Figure 11. Figure 12 illustrates a structure with upper-layer copper line 82 and via 81. A barrier layer 80 is conformally deposited in the openings 76 and 78. Copper is then deposited in the openings. A CMP is performed to planarize the copper to the surface of upper-layer copper line 82.

[0034] Electrical fuses can be formed at different levels based on the requirements of the circuit design. Figure 13 illustrates a stacked via string coupled between conductive lines 100 and 111. Vias 102, 106 and 109 are formed in different layers and are interconnected by conductive islands 104 and 108. Islands 104 and 108 are coupled to external pads 112 and 114, respectively. Therefore, the vias can be burned out individually. The via string can also be used as one via. When a voltage is applied between pads 110 and 113, the weakest via is burned out first and the whole via string is open. In a different embodiment of the present invention, the cross section of a via can take the shape of square, rectangle, circle or other shapes. A via can also be tapered.

[0035] The e-fuse structure of the present invention can be non-borderless or borderless. Figure 14a illustrates a borderless structure. A via 124 is misaligned with at least one of the conductive lines 120 and 126. Part of the via 124 extends out of the conductive lines 120 and 126. The extension width E_w is preferably less than about ¾ of the via width W. The misalignment typically does not affect the function of the electrical fuse. It only lowers the current needed to

burn the fuse. In a non-borderless structure, the via 130 has no extension beyond conductive lines 128 and 132, as shown in Figure 14b.

[0036] Figures 15a and 15b illustrate applications of the preferred embodiment. Figure 15a illustrates an electrical circuit 148 coupled in series with a fuse 146. The electrical circuit could be a circuit that may be replaced when it malfunctions. When the fuse 146 is burned out by applying a current through external pads 142 and 144, the electrical circuit 148 is disconnected from the other circuits. Figure 15b illustrates an e-fuse 134 coupled in parallel with a redundant circuit 136. One end of the e-fuse 134 is coupled to the ground. Therefore the redundant circuit 136 is grounded by the e-fuse 134 and not activated. If a circuit element is found defective and needs to be replaced by the redundant circuit 136, a voltage is applied to external pads 138 and 140 to burn the e-fuse 134. When the e-fuse 134 is open, the redundant circuit 136 is activated. A circuit redundancy scheme can be established by combining the circuits in Figure 15a and Figure 15b.

[0037] Figures 16 and 17 illustrate another embodiment of the present invention. Figure 16 is a cross sectional view of the embodiment. A fuse comprising a via 168, a second-level conductive line 166, and a via group 170 is formed between two portions 160_1, 160_2 of a conductive line 160. Conductive line 160 and 166 are also referred to as conductive layers. Conductive line 160_1 is the cathode end and conductive line 160_2 is the anode end. Figure 17 is a top view of the embodiment. At the anode end, via group 170 comprises two or more vias and can sustain higher current density than the via 168. With the asymmetric design, when the same current flows through via 168 and via group 170, via 168 has higher current density than vias in the via group 170 and thus is more prone to be burned out. Although Figure 16 illustrates a preferred embodiment in which conductive line 166 is formed in a lower metal layer than

conductive lines 160_1 and 160_2, they may have different relative positions in other embodiments. For example, assuming line 160_1 is in metal layer m, the conductive line 166 may be in metal layer m-1, m+1, and metal lines 160_2 may be in other metal layers such as metal layer m-2, m+1, m+2, etc.

[0038] Figure 18 illustrates a circuit for burning out a fuse. A fuse 176 is connected in series with a transistor 178, which in this configuration is preferably an nMOS device. The fuse 176 and the transistor 178 are coupled between power nodes Vcc and Vss, wherein the source of the transistor 178 is connected to Vss, and the drain is connected to the fuse 176. When a high voltage is applied to the gate of the transistor 178, transistor 178 conducts. A current flows through and burns fuse 176. If the fuse to be burned has an asymmetric design as in Figures 16 and 17, it is preferred that the cathode of the fuse, which is the single via end, is coupled to node 174, and the anode is coupled to the high power supply node Vcc. It is easier to burn the fuse with such a connection. When a fuse illustrated in Figures 16 and 17 is used as the fuse 176, the cathode end 160_1 is preferably connected to the drain of the transistor 178, and the anode end 160_2 is preferably connected to the power node Vcc.

[0039] The current density required for burning out a fuse is dependent on the material of the via and conductive lines, and the process used. One skilled in the art can find the right current density through routine experiment. Table 1 presents exemplary data measured on the vias formed using 90nm technology.

Layer	Dimension(μm)	Burn-out Current (mA)	Burn-out Current density (A/cm^2)
M1	0.12 x 0.25	0.200	6.66×10^5
M2 ~ M7	0.14 x 0.325	0.312	6.86×10^5
M8, M9	0.42 x 0.9	2.880	7.62×10^5

Contact	0.12 x 0.12	0.294	2.04×10^6
Via 1 ~ Via 6	0.13 x 0.13	0.189	1.12×10^6
Via 7, Via 8	0.36 x 0.36	1.452	8.8×10^5
All stacked vias except Via7 and 8	0.13 x 0.13	0.189	1.12×10^6
Stacked vias with Via 7 and Via 8	0.36 x0.36	1.452	8.8×10^5

[0040] M1 through M9 are metal lines at different layers, with M9 being the top layer metal, and M1 being the bottom layer metal. Via 1 is between M1 and M2. Via2 is between M2 and M3, and via 8 is between M8 and M9. Typically, M8 and M9 are power lines so that they have the greatest thickness of 0.9μm, which is the second value found in their dimensions. The dimensions of M1 through M9 indicate width x thickness, and dimensions for vias indicate cross sectional dimensions.

[0041] In table 1, Rows marked as M1 through M9 present the current and current density needed to burn out the metal lines. Rows marked as via1 through via8 present the current and current density needed to burn out the vias. The burn-out current density is calculated based on the burn-out current divided by the cross sectional area, which in turn can be calculated from the dimension. While the current density to burn out the via is affected by the material and process, the current for burning out a via is also affected by the cross sectional area. Preferably, the cross sectional area of the via is between about $1 \times 10^4 \mu m^2$ to about $1 \mu m^2$. By adjusting the cross sectional area for an e-fuse or a portion of an e-fuse, the burn-out current can be adjusted into a desired range. One skilled in the art can take the factors such as the material, process, dimension, current, and current density into consideration so that the structure comprising upper-layer conductive line, lower-layer conductive line and the via is adapted to be an e-fuse.

[0042] It is observed that in order to burn out the vias or the metal lines, the required current density is in the order of about $10^5 A/cm^2$ to about $10^6 A/cm^2$. Although the data shows that the burn-out current density of metal lines are in the same order as, or some times even lower than the burn-out current density of vias, which suggests that the burn-out region should occur in metal lines instead of vias, the experiment results have revealed that the burn-out regions are typically in via or close to the interfaces between the via and metals lines (refer to Figures 16a and 16b), providing the burn-out current densities for metal lines are not too much lower than for vias. This result has indicated that the vias are suitable for e-fuses.

[0043] There is no special requirement as to the height of a via. The height is preferably determined by the distance between metal layers. This provides flexibility in the design of the fuse since the fuse design can be easily integrated into the chip design without incurring extra processing steps and cost. In a preferred embodiment, the height is between about 500Å to about 10000Å.

[0044] Figures 19a and 19b illustrate side views of two examples of burned fuses 154, which are coupled between two respective conductive lines 150 and 152, of the present embodiment. Typically, the burned out region 156 is close to the interfaces between the via and the upper-layer/lower-layer conductive lines. In Figure 19a, the burn out region 156 is mainly in via 154. In Figure 19b, the burn out region 156 extends to one of the conductive lines 152.

[0045] There are several advantages features provided by the embodiments of the present invention. These include (but are not limited to): first, higher repairable rate can be achieved since the burn out process is easier to control and more reliable. Second, fewer masking layers is required therefore reducing cost. Third, the preferred embodiments provide a flexible structure

for circuit designers. The fuse may reside in any region of the inter layer vias for cell size reduction.

[0046] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

WHAT IS CLAIMED IS:

1. An electrical fuse comprising:

a first conductive layer;

a second conductive layer; and

a via coupled between the first conductive layer and the second conductive layerwherein at least one of the via, the first conductive layer and the second conductive layer are adapted to be an electrical fuse.

2. The electrical fuse of claim 1 wherein the electrical fuse further comprises a first external pad coupled to the first conductive layer, and a second external pad coupled to the second conductive layer.

3. The electrical fuse of claim 1 further comprising:

a third conductive layer; and

a plurality of vias coupled between the second conductive layer and the third conductive layer.

4. The electrical fuse of claim 3 further comprising

an nMOS transistor having a drain coupled to the third conductive layer; and

a source coupled to a first power supply node wherein the first conductive layer is coupled to a second power supply node.

5. The electrical fuse of claim 1 wherein the via has a cross sectional area of between about $10^{-4}\mu m^2$ and about $1\mu m^2$.

6. The electrical fuse of claim 1 wherein the via has a height of between about 500Å and about 1μm.

7. The electrical fuse of claim 1 wherein the via comprises a conductive material and a barrier layer outside the conductive material.

8. The electrical fuse of claim 1 further comprising:

a plurality of additional vias each in a different layer; and

a plurality of additional conductive layers wherein the additional vias are coupled in series and each of the additional vias is coupled between two of the additional conductive layers.

9. The electrical fuse of claim 8 further comprising:

a plurality of external pads each coupled to one of the additional conductive layers

10. The electrical fuse of claim 1 wherein the first conductive layer, the secondconductive layer and the via comprise copper and are formed by a method selected from the group consisting of single damascene process and dual damascene process.

11. The electrical fuse of claim 1 wherein the via is misaligned to the first and/or the second conductive layers.

12. The electrical fuse of claim 12 wherein the misalignment is smaller than about ¾ of the via dimension in the misalignment direction.

13. A semiconductor device comprising:

a burned-out electrical fuse comprising:

a first conductive layer;

a second conductive layer; and

a via coupled between the first conductive layer and the second conductive layer and adapted to be a fuse.

14. The electrical fuse of claim 1 wherein the electrical fuse comprises a first external pad coupled to the first conductive layer; a second external pad coupled to the second conductive layer; and an electrical discontinuity in the via or adjacent the interfaces between the via and the first and the second conductive layers.

15. The electrical fuse of claim 14 further comprising a plurality of vias between the first and the second external pads.

16. The electrical fuse of claim 1 further comprising:

a third conductive layer; and

a plurality of vias coupled between the second conductive layer and the third conductive layer wherein the vias are not burned-out.

17. The electrical fuse of claim 1 wherein the via has a cross sectional area of between about $10^{-4}\mu m^2$ and about $1\mu m^2$.

18. A semiconductor device comprising:

an electrical circuit;

a redundant circuit having a redundant design of the electrical circuit;

a first conductive layer;

a second conductive layer; and

a first via coupled between the first conductive layer and the second conductive layer wherein one of the first and second conductive layers is coupled to the redundant circuit and wherein the first via, the first conductive layer and the second conductive layer are adapted to be an electrical fuse.

19. The semiconductor device of claim 18 further comprises a first external pad coupled to the first conductive layer; and a second external pad coupled to the second conductive layer.

20. The semiconductor device of claim 18 further comprising:

a second via coupled in parallel with the electrical circuit;

wherein the second via is coupled between a third conductive layer and a fourth conductive layer;

wherein the second via, the third conductive layer and the fourth conductive layer are adapted to be an electrical fuse;

a third external pad coupled to the third conductive layer; and

a fourth external pad coupled to the fourth conductive layer.