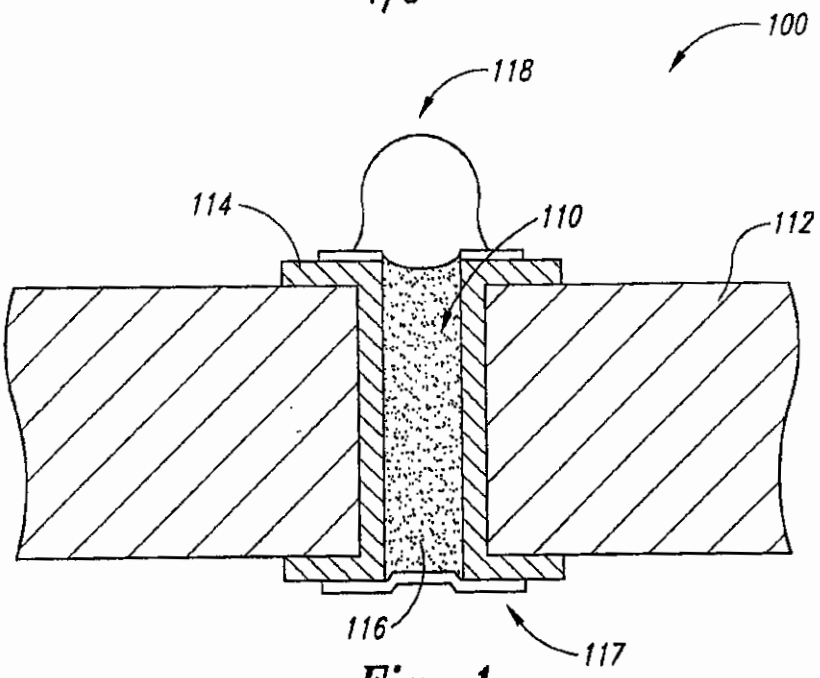


Fig. 1
(Prior Art)

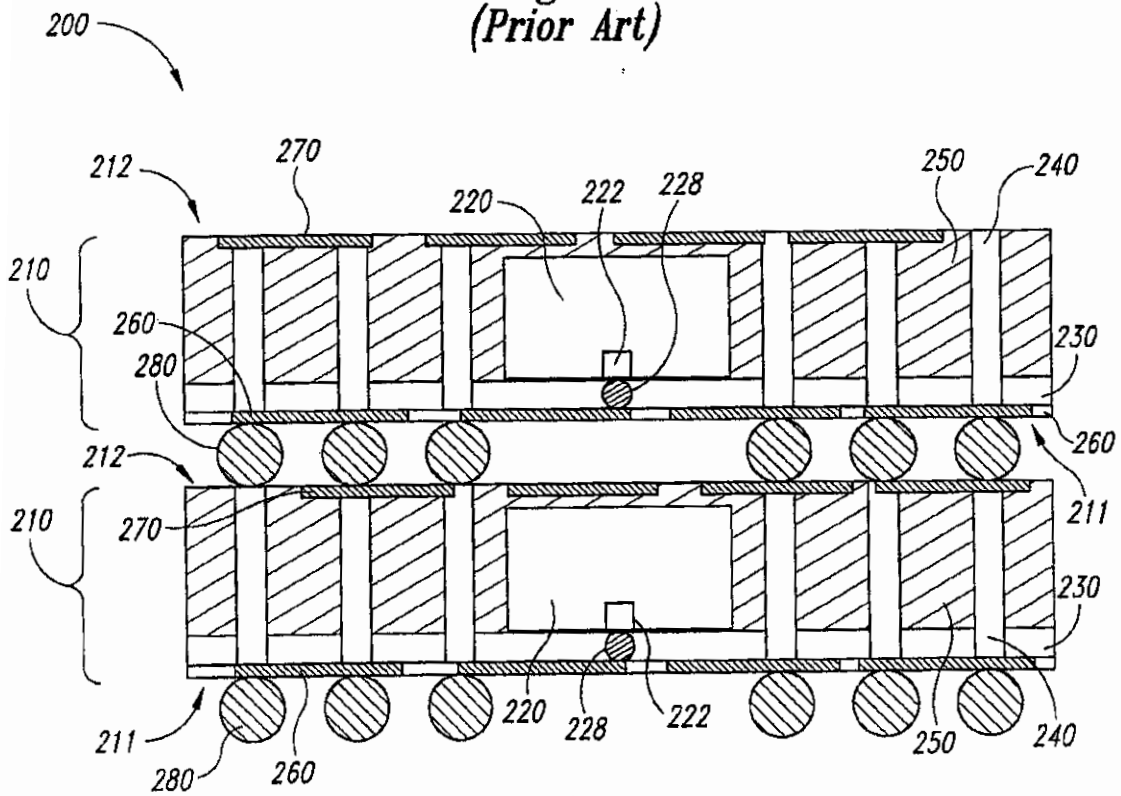


Fig. 2

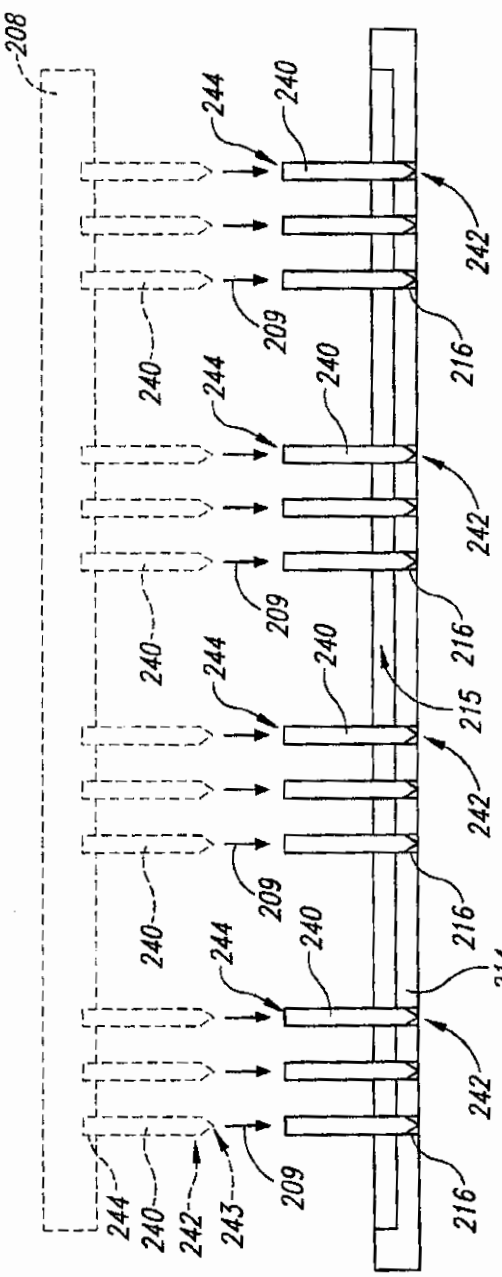

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Fig. 3

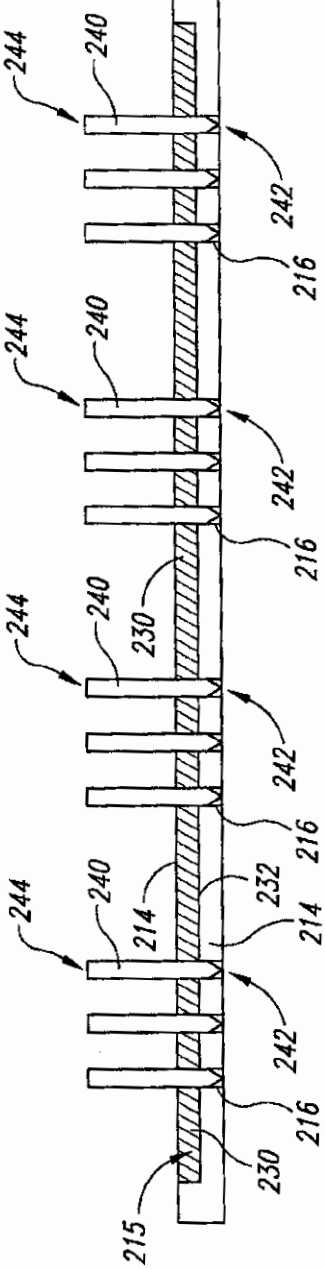

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Fig. 4

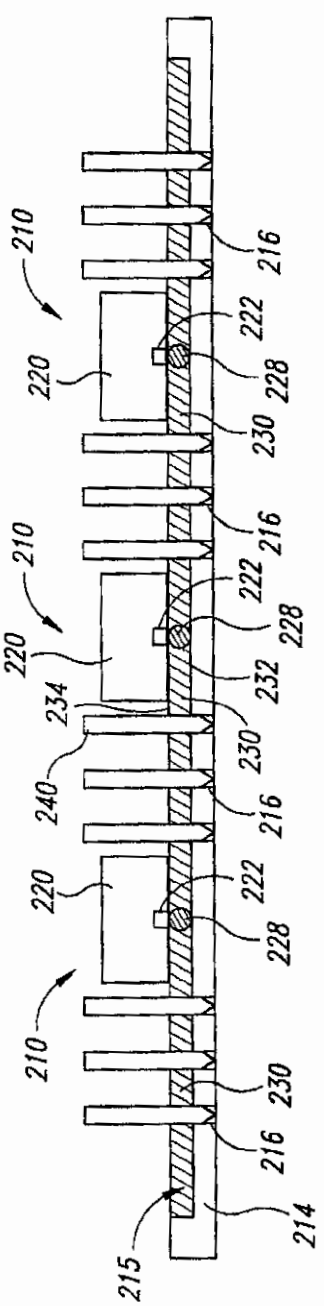

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Fig. 5

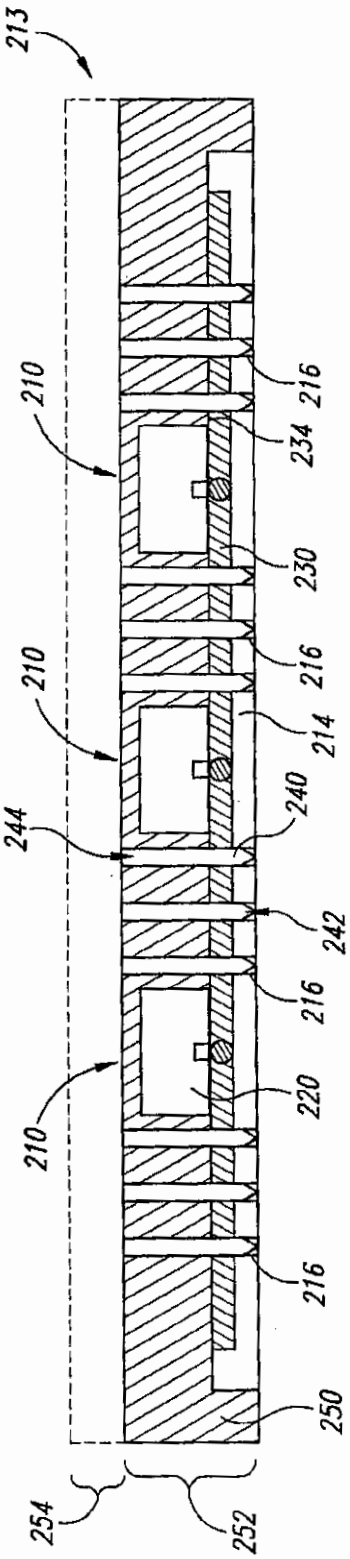

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Fig. 6

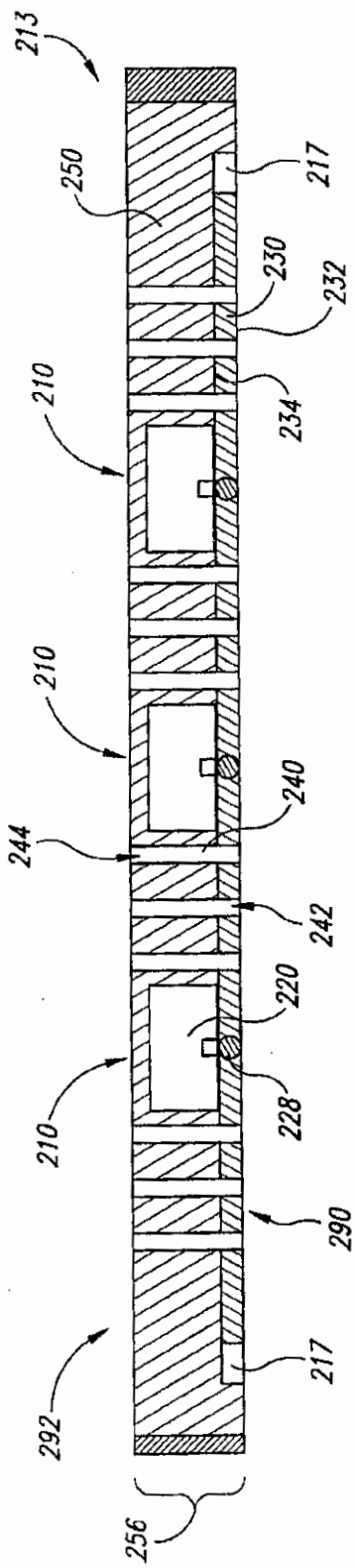

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Fig. 7

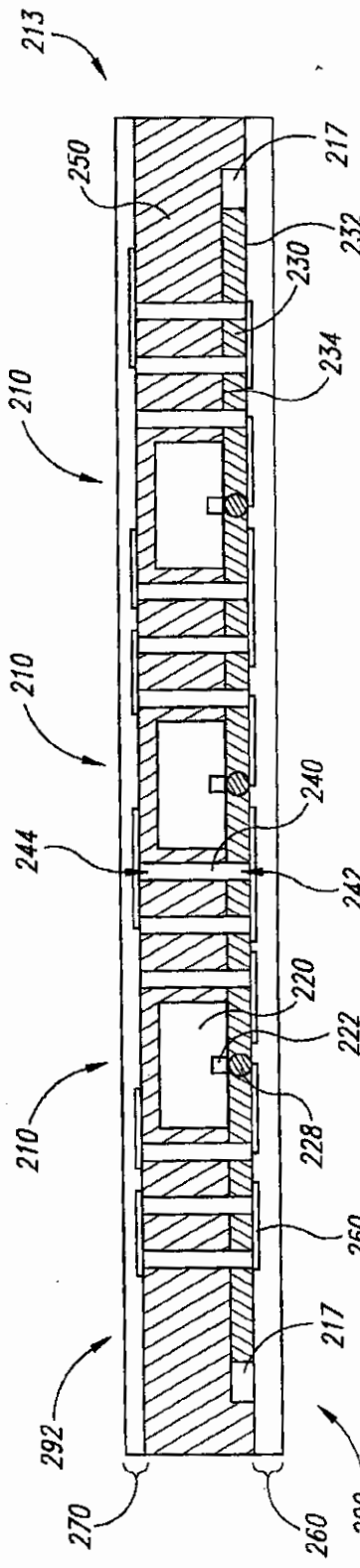

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Fig. 8

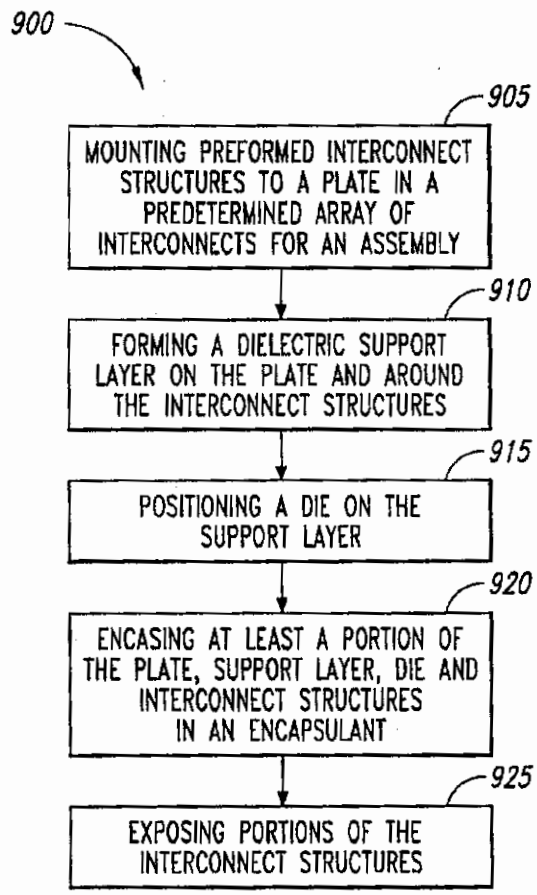

900
905
MOUNTING PREFORMED INTERCONNECT STRUCTURES TO A PLATE IN A PREDETERMINED ARRAY OF INTERCONNECTS FOR AN ASSEMBLY
910
FORMING A DIELECTRIC SUPPORT LAYER ON THE PLATE AND AROUND THE INTERCONNECT STRUCTURES
915
POSITIONING A DIE ON THE SUPPORT LAYER
920
ENCASING AT LEAST A PORTION OF THE PLATE, SUPPORT LAYER, DIE AND INTERCONNECT STRUCTURES IN AN ENCAPSULANT
925
EXPOSING PORTIONS OF THE INTERCONNECT STRUCTURES

Fig. 9

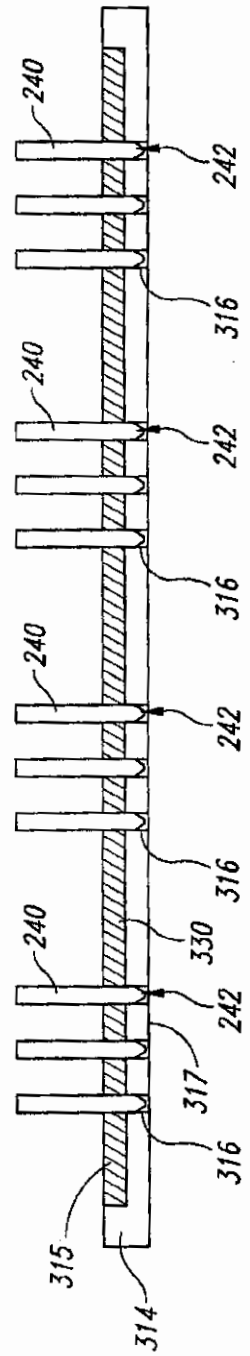


Fig. 10A

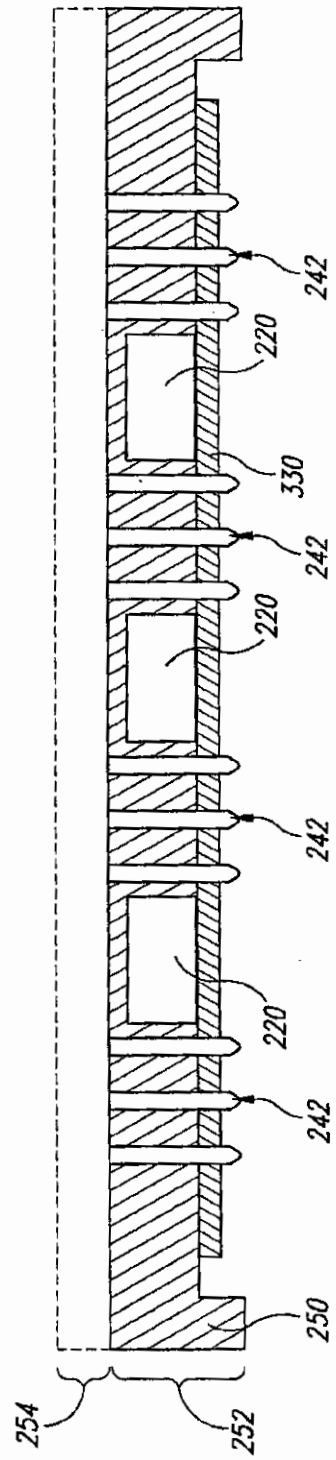


Fig. 10B

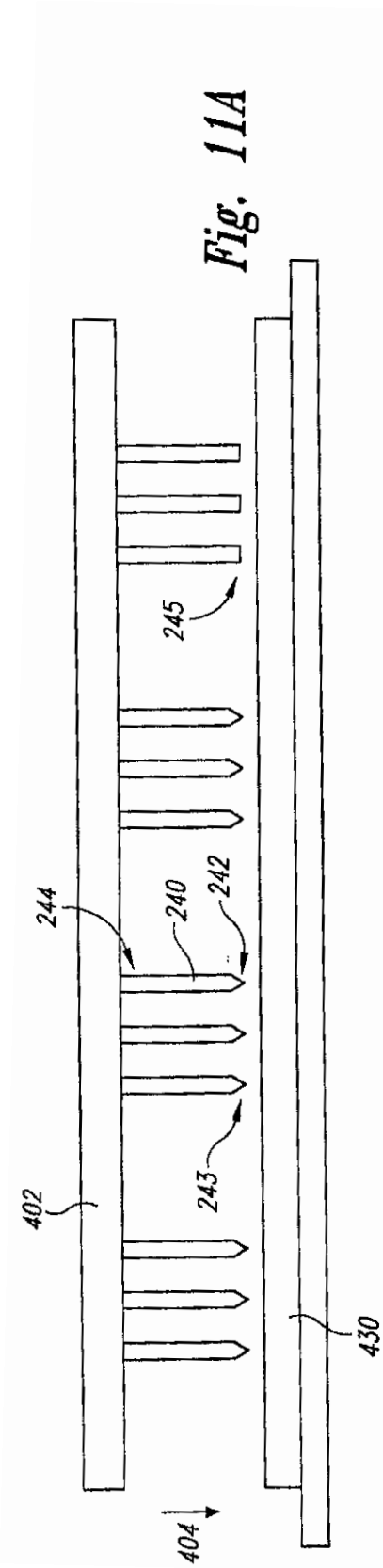


Fig. 11A

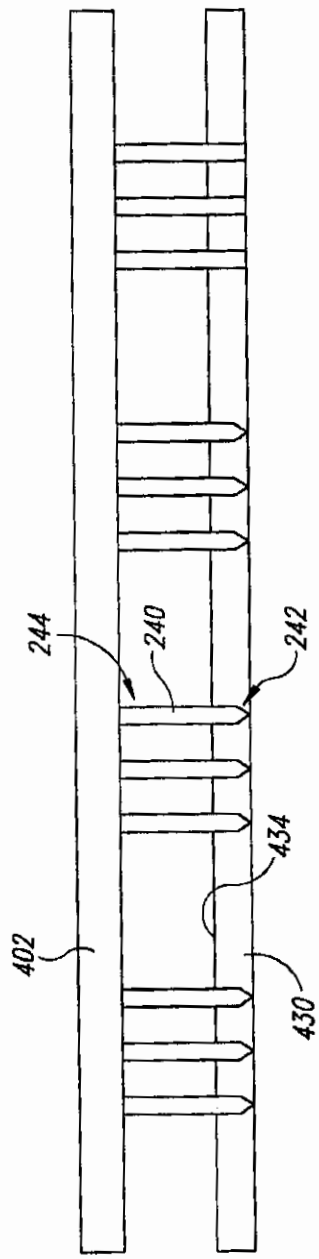


Fig. 11B

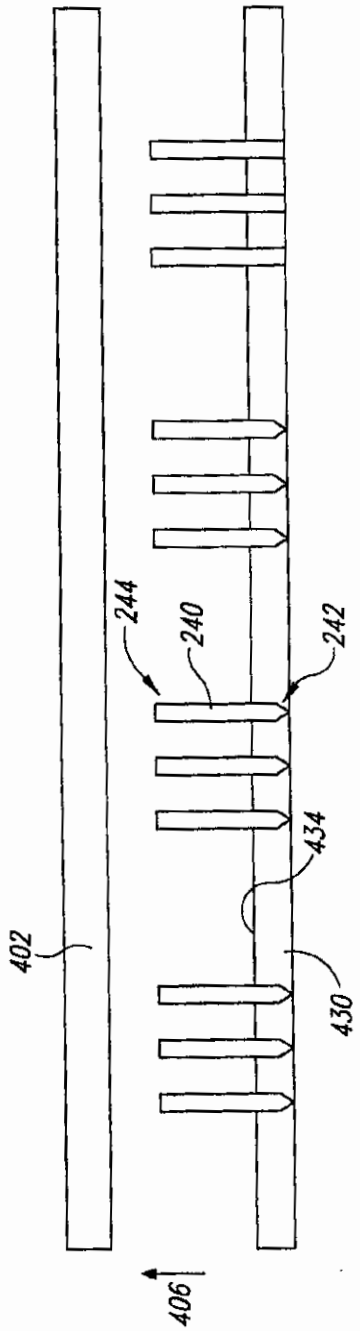


Fig. 11C

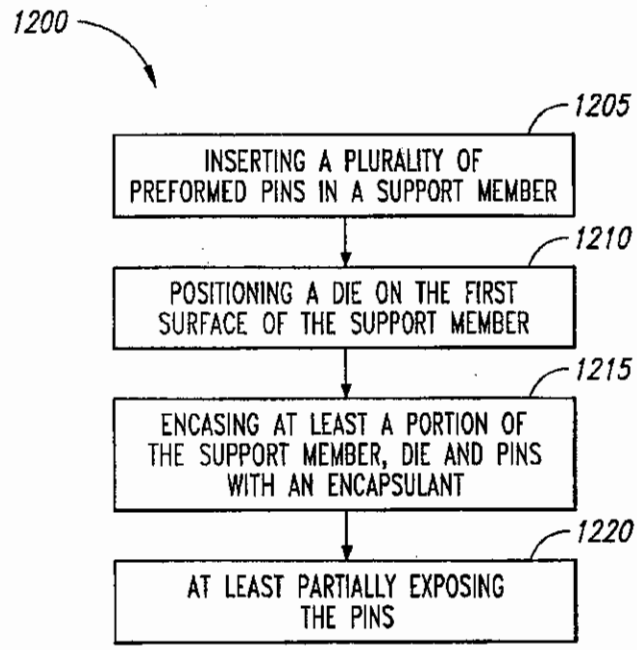

1200
1205
INSERTING A PLURALITY OF PREFORMED PINS IN A SUPPORT MEMBER
1210
POSITIONING A DIE ON THE FIRST SURFACE OF THE SUPPORT MEMBER
1215
ENCASING AT LEAST A PORTION OF THE SUPPORT MEMBER, DIE AND PINS WITH AN ENCAPSULANT
1220
AT LEAST PARTIALLY EXPOSING THE PINS

Fig. 12

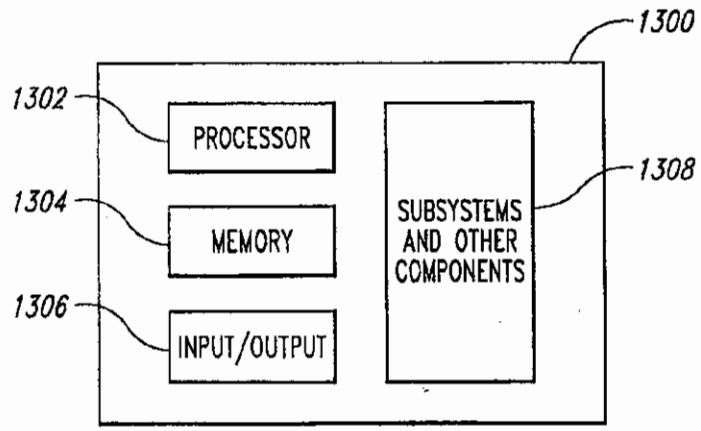

1300
1302
PROCESSOR
1304
MEMORY
1306
INPUT/OUTPUT
SUBSYSTEMS AND OTHER COMPONENTS
1308

Fig. 13