

PATENT SPECIFICATION

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DRAWINGS ATTACHED.

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COMPLETE SPECIFICATION

Electrical Circuits Including Field-Effect Transistors.

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electrical circuits employing field-effect transistors.

It is an object of this invention to provide an improved electrical circuit employing a field-effect transistor, and the present invention accordingly comprises an electrical circuit including a field-effect transistor with a gate electrode and source and drain operating electrodes formed on a substrate and defining a current path controllable as a function of the potential applied to the gate electrode, said gate electrode being electrically insulated from the substrate and the source and drain operating electrodes, a source of alternating voltage coupled by a capacitor to the gate electrode to control the conductivity of the current path, an output circuit including a load impedance connected in series with the current path, a first impedance connected between a reference potential and the gate electrode and providing with the capacitor a discharge time constant greater than the period of the alternating voltage, the source electrode being connected to the reference potential with the substrate providing a rectifying junction with the source electrode and having a direct connection including a second impedance to the gate electrode to bias the rectifying junction forwardly during the excursions of the alternating voltage in one polarity direction

whereby the alternating voltage in the one direction is limited, and to cause the gate electrode to be driven to a cut off bias potential by the excursions of the alternating voltage in the opposite direction.

In the accompanying drawing:

Figure 1 is a diagrammatic view of a field-effect transistor suitable for use in circuits embodying the invention;

Figure 2 is a cross section taken along line 2—2 of Figure 1;

Figure 3 is a graph showing drain current versus drain voltage curves, for various values of gate-to-source voltages for the transistor of Figure 1;

Figure 4 represents a limiter circuit embodying the invention;

Figure 5 represents a synchronizing signal separator, for television receivers, embodying the invention; and

Figure 6 represents an oscillator circuit embodying the invention.

Referring to Figure 1, a field-effect transistor 10 includes a body 12 of semiconductor material. The body 12 may be either a single crystal wafer or polycrystalline wafer and may be of any suitable material used in the semiconductor art. For example, the body 12 may be lightly doped P-type silicon of 100 ohm cm. material.

In its manufacture silicon dioxide heavily doped with N-type material is deposited over the surface of the silicon body 12. By means of a photo-resist and acid etching, or other suitable technique, the silicon dioxide is removed where the gate electrode is to be formed, and around the outer edges of the wafer. The deposited silicon dioxide is left over those areas where the source-drain regions are to be formed.

The body or wafer 12 is then heated in a suitable atmosphere so that exposed silicon areas are oxidized to form grown silicon

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dioxide layers indicated by the lightly stippled areas of Figure 1. During the heating process, impurities from the deposited silicon dioxide layer diffuse into silicon body 12 to form the source and drain regions. Figure 2 shows the source-drain regions labelled S and D respectively.

By means of another photo-resist and acid etching or like step the deposited silicon dioxide over part of the source-drain diffused regions is removed. Electrodes are formed for the source, drain and gate regions by evaporation of a conductive material by means of an evaporation mask. The conductive material evaporated may be chromium and gold in the order named, for example, but other suitable conductive materials may be used.

The finished wafer is shown in Figure 1, in which the lightly stippled area between the outside boundary and the first dark zone 14 is grown silicon dioxide. The white area 16 is the conductive electrode corresponding to the source electrode. Dark zones 14 and 18 are deposited silicon dioxide zones overlying portions of the diffused source region and the dark zone 20 is a deposited silicon dioxide zone overlying a portion of the diffused drain region. White areas 22 and 24 are the conductive electrodes which correspond to the gate and drain electrodes respectively. The lightly stippled zone 28 is a layer of grown silicon dioxide, on a portion of which the gate electrode 22 is placed, and which insulates the gate electrode 22 from the substrate silicon body 12 and from the source and drain electrodes as shown in Figure 2. The input resistance of the device at low frequencies is of the order of 10^{14} ohms. The silicon wafer or substrate is mounted on a conductive base or header 26, which serves as a substrate electrode, as shown in Figure 2. The layer of grown silicon dioxide 28 on which the gate electrode 22 is mounted, overlies an inversion layer or channel connecting the source and drain regions. The gate electrode 22 is displaced towards the source region S so that the distance between the source region S and the gate electrode 22 is smaller than the distance between the gate electrode 22 and the drain region D. If desired, the gate electrode may overlap the deposited silicon dioxide layer 18. Alternatively, the gate electrode may be symmetrically disposed between the source and drain regions.

The drain and source electrodes are connected to each other by a channel C. The electrons flow from source to drain in this thin channel region close to the surface. The conductive channel C is shown in Figure 2 in dotted lines.

Alternatively, the wafer 12 may be of lightly doped N-type semiconductor ma-

terial, and the source and drain regions of P-type material. The source electrode is defined as the electrode from which majority carriers flow, and the drain electrode as that electrode to which majority carriers flow. In the case of the device of Figures 1 and 2 with a P-type wafer and N-type source and drain regions the majority carriers are electrons which flow toward the terminal of positive potential. Accordingly, since the device is substantially symmetrical, the one of the electrodes 16 and 24 to which the positive potential of a supply source is applied operates as the drain electrode. If the device has an N-type substrate or wafer, the majority carriers are holes, and the electrode to which the negative terminal of a supply source is applied operates as the drain electrode.

Figure 3 is a family of curves 30-39 in which drain current, represented along the ordinate, is plotted against drain voltage, represented along the abscissa, for the transistor of Figures 1 and 2, for different values of gate-to-source voltage. Curves 38-39 are representative of high drain current, and curves 30-33 are representative of relatively low drain current and are relatively closely spaced, whereas the intermediate curves 34-37 are relatively uniformly spaced. The equal spacing of the latter curves for equal gate-to-source voltage increments of voltage is indicative of a linear operating region for the transistor. A feature of an insulated-gate field-effect transistor is that the zero bias characteristic can be at any one of the curves 30-39 shown in Figure 3 with the curves above the zero bias curve representing positive gate voltages relative to the source, and the curves below the zero bias point representing negative gate voltages relative to the source.

The location of the zero bias curve can be selected by control of the processing of the transistor during its manufacture. For example, by controlling the time and/or temperature of the step of the process when the silicon dioxide layer 28 is grown, the number of free charge carriers in the device can be controlled. The longer the transistor is baked, and the higher the temperature, in a dry oxygen atmosphere, the more the drain current for a given amount of drain voltage for zero bias between the source and gate electrodes. By way of example, to establish the curve 36 as the zero bias curve, during the step which produces the silicon dioxide layer 28, the transistor was baked for two hours at 900° centigrade in an atmosphere of dry oxygen. If the temperature, or time of baking, or both are increased, the zero bias curve will correspond to one of the curves

37—39. By decreasing the temperature of time or both, in the baking cycle the zero bias curve will occur for lower values of drain current such as for example one of the curves 30—35.

In Figure 4, a limiter circuit is shown, which may, for example, comprise one of the stages in the intermediate frequency amplifier portion of a frequency modulation superheterodyne receiver, for limiting the amplitude of an i-f wave prior to its application to an f-m detector. The insulated-gate field-effect transistor 10 has the source electrode 16 connected to a point of reference potential shown as ground. The drain electrode 24 is connected through a tuned circuit 50 to the positive terminal of a source of bias potential 52, the negative terminal of which is connected to ground. The tuned circuit 50 is coupled to a suitable load indicated by a resistor 54.

The gate electrode 22 is biased to a desired bias potential for optimum signal translation from a source of bias potential through a resistor 56. In the present instance, no gate bias voltage is applied under steady state conditions, and accordingly the resistor 56 is connected between the gate electrode 22 and ground. Input signals are coupled to the gate electrode 22 through a coupling capacitor 58 from a signal source comprising the tuned primary circuit 60 and secondary circuit 62 of an intermediate frequency transformer.

A pair of rectifying junctions 64 and 66 effectively appear between the substrate electrode 26 and the drain and source electrodes 24 and 16, respectively. Since the transistor 10 has P-type impurities in the substrate, the substrate comprises the anode portion of the rectifying junctions and the source and drain electrodes operate respectively as the cathode portions of the rectifying junctions. If a transistor is used which has N-type impurities in the substrate, the rectifying junctions will be oppositely poled as will the poling of the potential supply source 52. The substrate electrode 26 is conductively connected for direct current, as by a wire or resistor 68, to the gate electrode 22. If the connection is a wire, the resistor 68 represents the spreading resistance (inherent series resistance) of the rectifying junction 66, as measured between the substrate and source electrodes.

The transistor 10 is preferably selected as one whose zero gate-to-source bias characteristic provides the desired initial or quiescent operating point for the circuit. For example, the zero bias characteristic of the transistor may correspond to the curve 36 of Figure 3, which is presumed to be at the approximate centre of the linear

operating or signal transfer characteristic of the transistor. The signal applied to the gate electrode 22 is translated by the circuit, which for small signals may operate as a common source Class A amplifier, and output signals are developed in the tuned drain circuit 50.

As the signal drives the gate electrode, and the substrate electrode, in the positive polarity direction, the rectifying junction 66 becomes conductive and tends to limit the positive going excursions of the signal as a function of the value of the resistor 68. The conduction of the rectifying junction 66 charges the capacitor 58, which on negative half cycles of the signal discharges through the resistor 56 thereby establishing a negative bias voltage between the gate electrode 22 and source electrode 16. The time constant of the resistor 56-capacitor 58 network is preferably made longer than the period of the i-f wave supplied by the input circuit 62. Accordingly, the circuit including the rectifying junction 66 effectively operates as a peak detector circuit and clamps the positive peaks of the applied signals to substantially the potential of the source electrode 16, which is grounded.

As the signal level increases, the operating point of the transistor moves successively from the curve 36 to the curves 35—34—33 etc. (see Figure 3). Hence, the negative going excursion of the stronger signals will drive the transistor into cut-off more quickly. For still stronger signals, the transistor may be cut off by the bias voltage developed in the peak detecting circuit for a substantial portion of the cycle of the input signal whereby a series of output pulses of current are derived from the drain electrode 24. These pulses of current will be regenerated as substantially a sine wave by the tuned output circuit 50.

If the transistor is of the "depletion" type, i.e. has a zero bias characteristic corresponding to one of the curves 37—39 of Figure 3, a negative bias voltage must be applied to the gate electrode 22 relative to the source electrode 16 if the transistor is to operate at the centre of its linear transfer characteristic. The appropriate bias voltage may be applied by connecting the gate electrode through a resistor (not shown) of suitable value, to the negative terminal of a source of operating potential (also not shown). The negative voltage at the gate electrode 22 is also applied to the substrate electrode 26 and provides a "delay", or increased threshold before the rectifying junction 66 becomes conductive. Stated otherwise, the rectifying junction 66 will not conduct until the applied signal level is sufficiently large to overcome the

negative bias voltage applied to the gate electrode. To reduce the amount of delay provided by such negative gate bias, a suitable potential supply source such as a battery (not shown) is connected in series with the resistor 68 between the source and substrate electrodes, with the battery polarized in a direction to hold the substrate electrode positive relative to the gate electrode.

As a further alternative of the circuit of Figure 4, if the transistor is of the "enhancement" type, i.e. has a zero bias characteristic corresponding to one of the curves 30—35, a positive voltage applied to the gate electrode causes the transistor to operate at the centre of its linear operating characteristic. The appropriate bias voltage may be applied by connecting the gate electrode 22 through a resistor of suitable value (not shown) to the positive terminal of a source of operating potential which may comprise the source 52. The positive voltage at the gate electrode is also applied to the substrate electrode and causes the rectifying junction 66 to conduct current under the steady state conditions. To prevent excessive bias current drain by the rectifying junction 66, and undesirable limiting of weak signals, a suitable potential supply source such as a battery is connected in series with the resistor 68 between the source and substrate electrodes. Of course, if no resistor is used, the battery is connected in series with the gate-substrate conductor. The above mentioned battery (which is not shown) is polarized in a direction to hold the substrate electrode at negative potential relative to the gate electrode.

From the foregoing, it will be seen that the circuit of Figure 4 operates to provide substantial limiting of the signals above a certain threshold value, which are applied thereto. An important feature of the circuit is the means including a direct current circuit connecting the gate and substrate electrodes for maintaining the substrate and source electrodes at substantially the same potential. In the case of the circuit shown in Figure 4, the means comprises a transistor having the appropriate zero bias characteristic for small signal translation, and the connection between gate and substrate electrodes. In the cases where the transistor is of the enhancement or depletion types and the gate is maintained at a potential substantially different from zero relative to the source electrode, the means includes a potential supply source of appropriate value between the gate and source electrodes.

The schematic circuit diagram of Figure 5 represents a synchronizing signal separator for television receivers. A source of

composite television signals, such as a video amplifier stage (not shown), is coupled to a signal synchronizing stage through a double time constant network which enhances the immunity of the synchronizing signal separator to spurious noise impulses. One portion of the double time constant network comprises a series capacitor 72 and a shunt resistor 74 which are selected to provide a relatively long time constant. The second portion of the double time constant network comprises a parallel connected resistor 76 and capacitor 78 of relatively short time constant which are connected between the capacitor 72 and the gate electrode 22 of an insulated-gate field-effect transistor 10 of the type described in connection with Figures 1 and 2 having its source electrode 16 grounded. The drain electrode 24 is connected to the positive terminal of a potential supply source 88 through a load resistor 90. The separated synchronizing pulses are derived from across the resistor 90. The substrate electrode 26 is connected to the gate electrode 22 through a resistor 68 which may comprise the spreading resistance of the rectifying junction between the substrate electrode and source electrode or a physical external resistor.

The transistor in this circuit is of the enhancement type, that is it has a zero bias characteristic curve corresponding to the curve 30 of Figure 3. Hence, in the absence of signals substantially no drain current flows through the load resistor 90. Since the composite television signals are capacitively coupled to the synchronizing signal separator stage through the capacitor 72, the relative amplitude of the synchronizing pulses with respect to ground potential varies as a function of the picture content or brightness. In order effectively to separate the synchronizing pulses from the remainder of the composite signal it is desirable to refer the synchronizing pulse peak amplitude at a fixed potential. Ordinarily, in tube or junction transistor types of circuits the referencing of the synchronizing signal peaks is effected by the rectifying action between grid and cathode of a vacuum tube or base and emitter of the junction transistor. In operation, the synchronizing signal amplitude causes conduction of the base-emitter or grid-cathode path to clamp the peaks thereof to a fixed potential.

However, in a synchronizing signal separator circuit employing an insulated-gate field-effect transistor, an extremely high impedance exists between the gate electrode and the other electrodes of the device. In order to effect the desired clamping action of the synchronizing signal peaks, the gate electrode is direct current con-

ductively connected to the substrate electrode 26. When the composite signal is applied to the transistor, with a synchronizing signal excursion in the positive polarity direction, the rectifying junction between the substrate 26 and the source electrode 16 conducts, and thereby the synchronizing peaks appearing at the gate electrode are clamped to ground or to a potential more positive than ground depending upon the value of the resistance 68. The resistance 68 in this circuit is large enough to permit the gate electrode to go sufficiently positive with respect to the source electrode to drive the transistor into substantially source-drain conduction.

When the synchronizing signal peaks cause the rectifying junction between the substrate electrode and the source electrode to conduct current, the capacitors 78 and 72 are charged. The discharge of these capacitors through resistors 76 and 74 respectively bias the gate electrode 22 negatively relative to ground as a function of the peak amplitude of the synchronizing pulses. The larger the peak amplitude of the synchronizing pulses, the further the transistor is driven into cut-off. Hence, the transistor is automatically maintained cut off except during the synchronizing pulse interval even though the average amplitude or picture content of the composite signal changes, and is thereby effective to separate the synchronizing pulses from the remainder of the composite signal.

If the transistor used in the circuit of Figure 5 provides substantial drain current under the zero gate bias condition, then a d-c voltage is applied between the gate and source electrodes so that substantially no drain current flows under no signal conditions. Accordingly a suitable potential supply source may be connected between the gate and substrate electrodes so that the substrate is maintained at substantially the same potential as the source electrode.

A further embodiment of the invention is shown in Figure 6 which represents a tuned-drain tuned-gate oscillator circuit. In this oscillator circuit the source electrode 16 of the transistor 10 is connected to ground, and the drain electrode 24 is connected through a resonant tank circuit 102 to the positive terminal of a source of operating potential (not shown). Oscillatory waves from the oscillator may be applied to a capacitor by a coupling winding coupled to the tuned drain circuit 102.

The gate electrode 22 is coupled through a tuned gate circuit 104 and a capacitor 106, which is of low impedance at oscillator frequencies, to ground. The circuits 102 and 104 are tuned to the desired frequency of oscillation, with oscillation being sustained by regenerative feedback through a

capacitor 108. The transistor 10 in this circuit may be selected to provide sufficient transconductance under zero bias conditions to be self starting. Accordingly, the gate electrode 22 is connected to ground through a gate bias resistor 110. If the transistor does not exhibit sufficient transconductance for the oscillator to be self starting, then the resistor 110 is connected to a bias source to bias the gate electrode to a point where the transistor does exhibit the necessary transconductance.

Disregarding the direct current conductive connection between the gate electrode 22 and the substrate electrode 26, the amplitude of oscillation of the circuit shown in Figure 6 tends to be a function of the biasing between the gate electrode 22 and source electrode 16. Hence, the oscillator is not automatically self-adjusting in the face of load variations and the like, as are many tube or junction transistor oscillators. This lack of self-adjustment is because extremely high impedance exists between the gate electrode and the source and drain electrodes. In order to permit the oscillator to be self-adjusting, the conductive connection provided between the gate electrode 22 and the substrate electrode 26 permits rectification of the positive oscillator signal swing occurring in the gate electrode 22 through the rectifying junction appearing at the substrate 26 and source electrode 16. This causes the bias at the gate electrode to become more negative with respect to ground until an equilibrium point has been established between the total loading on the oscillator and average conductance of the transistor over the cycle of the oscillatory wave. Thus, with increased amplitude of oscillation, for example, due to load changes, the gate electrode is driven more negatively and cuts down the current flow through the transistor. Hence, the amplitude of oscillation tends to remain substantially constant for fairly wide variations of oscillator loading.

The circuit operates by considering the feedback signal through capacitor 108 as an input source of alternating voltage to the gate electrode 22. During a positive half cycle, capacitors 108 and 106 are charged from ground through the forwardly biased junction between the source 16 and the substrate 26. During the negative half cycle, the capacitors discharge through the resistor 110. If the time constant of the discharge circuit is greater than the frequency of the oscillator, then the gate 22 will be driven in a negative direction when the amplitude of oscillation exceeds an equilibrium operating value.

WHAT WE CLAIM IS:—

1. An electrical circuit including a field. 130



ductively connected to the substrate electrode 26. When the composite signal is applied to the transistor, with a synchronizing signal excursion in the positive polarity direction, the rectifying junction between the substrate 26 and the source electrode 16 conducts, and thereby the synchronizing peaks appearing at the gate electrode are clamped to ground or to a potential more positive than ground depending upon the value of the resistance 68. The resistance 68 in this circuit is large enough to permit the gate electrode to go sufficiently positive with respect to the source electrode to drive the transistor into substantially source-drain conduction.

When the synchronizing signal peaks cause the rectifying junction between the substrate electrode and the source electrode to conduct current, the capacitors 78 and 72 are charged. The discharge of these capacitors through resistors 76 and 74 respectively bias the gate electrode 22 negatively relative to ground as a function of the peak amplitude of the synchronizing pulses. The larger the peak amplitude of the synchronizing pulses, the further the transistor is driven into cut-off. Hence, the transistor is automatically maintained cut off except during the synchronizing pulse interval even though the average amplitude or picture content of the composite signal changes, and is thereby effective to separate the synchronizing pulses from the remainder of the composite signal.

If the transistor used in the circuit of Figure 5 provides substantial drain current under the zero gate bias condition, then a d-c voltage is applied between the gate and source electrodes so that substantially no drain current flows under no signal conditions. Accordingly a suitable potential supply source may be connected between the gate and substrate electrodes so that the substrate is maintained at substantially the same potential as the source electrode.

A further embodiment of the invention is shown in Figure 6 which represents a tuned-drain tuned-gate oscillator circuit. In this oscillator circuit the source electrode 16 of the transistor 10 is connected to ground, and the drain electrode 24 is connected through a resonant tank circuit 102 to the positive terminal of a source of operating potential (not shown). Oscillatory waves from the oscillator may be applied to a capacitor by a coupling winding coupled to the tuned drain circuit 102.

The gate electrode 22 is coupled through a tuned gate circuit 104 and a capacitor 106, which is of low impedance at oscillator frequencies, to ground. The circuits 102 and 104 are tuned to the desired frequency of oscillation, with oscillation being sustained by regenerative feedback through a

capacitor 108. The transistor 10 in this circuit may be selected to provide sufficient transconductance under zero bias conditions to be self starting. Accordingly, the gate electrode 22 is connected to ground through a gate bias resistor 110. If the transistor does not exhibit sufficient transconductance for the oscillator to be self starting, then the resistor 110 is connected to a bias source to bias the gate electrode to a point where the transistor does exhibit the necessary transconductance.

Disregarding the direct current conductive connection between the gate electrode 22 and the substrate electrode 26, the amplitude of oscillation of the circuit shown in Figure 6 tends to be a function of the biasing between the gate electrode 22 and source electrode 16. Hence, the oscillator is not automatically self-adjusting in the face of load variations and the like, as are many tube or junction transistor oscillators. This lack of self-adjustment is because extremely high impedance exists between the gate electrode and the source and drain electrodes. In order to permit the oscillator to be self-adjusting, the conductive connection provided between the gate electrode 22 and the substrate electrode 26 permits rectification of the positive oscillator signal swing occurring in the gate electrode 22 through the rectifying junction appearing at the substrate 26 and source electrode 16. This causes the bias at the gate electrode to become more negative with respect to ground until an equilibrium point has been established between the total loading on the oscillator and average conductance of the transistor over the cycle of the oscillatory wave. Thus, with increased amplitude of oscillation, for example, due to load changes, the gate electrode is driven more negatively and cuts down the current flow through the transistor. Hence, the amplitude of oscillation tends to remain substantially constant for fairly wide variations of oscillator loading.

The circuit operates by considering the feedback signal through capacitor 108 as an input source of alternating voltage to the gate electrode 22. During a positive half cycle, capacitors 108 and 106 are charged from ground through the forwardly biased junction between the source 16 and the substrate 26. During the negative half cycle, the capacitors discharge through the resistor 110. If the time constant of the discharge circuit is greater than the frequency of the oscillator, then the gate 22 will be driven in a negative direction when the amplitude of oscillation exceeds an equilibrium operating value.

WHAT WE CLAIM IS:—

1. An electrical circuit including a field-



effect transistor with a gate electrode and source and drain operating electrodes formed on a substrate and defining a current path controllable as a function of the potential applied to the gate electrode, said gate electrode being electrically insulated from the substrate and the source and drain operating electrodes, a source of alternating voltage coupled by a capacitor to the gate electrode to control the conductivity of the current path, an output circuit including a load impedance connected in series with the current path, a first impedance connected between a reference potential and the gate electrode and providing with the capacitor a discharge time constant greater than the period of the alternating voltage, the source electrode being connected to the reference potential with the substrate providing a rectifying junction with the source electrode and having a direct connection including a second impedance to the gate electrode to bias the rectifying junction forwardly during the excursions of the alternating voltage in one polarity direction whereby the alternating voltage in the one direction as limited, and to cause the gate electrode to be driven to a cut off bias potential by the excursions of the alternating voltage in the opposite direction.

2. An electrical circuit according to Claim 1, wherein the direct current connection between said gate electrode and said substrate establishes said substrate at substantially the same potential as said source electrode under steady state conditions and wherein voltage excursions at said gate electrode in one polarity direction are rectified by the rectifying junction appearing between said substrate and source electrode.

3. An electrical circuit according to Claim 1 and arranged for operation as a limiter circuit, wherein the transistor provides Class A operation under steady state and small signal conditions, and said first impedance is connected between said gate and source electrodes so that substantially zero direct voltage exists between said gate and source electrodes under no signal conditions.

4. An electrical circuit according to

Claim 3 wherein said transistor has a signal transfer characteristic at substantially zero gate-to-source bias voltage which provides the Class A operation.

5. An electrical circuit according to Claim 1 and arranged for operation as a limiter circuit, said first impedance connected between said gate and source electrodes being arranged to bias said transistor for Class A operation under weak signal conditions, the time constant of said resistor and capacitor together with the rectifying junction between said source and substrate electrodes providing a peak detector circuit for developing a direct voltage across said resistor as a function of the level of applied signals.

6. An electrical circuit according to Claim 1 and arranged as a synchronizing signal separator, said source of alternating voltage including a signal input circuit for a composite signal including the synchronizing pulses, the time constant of said capacitor and the resistor between said gate and source electrodes together with the rectifying junction between said source and substrate electrodes providing a peak detector circuit for developing a direct voltage across said resistor as a function of the peak amplitude of said synchronizing pulses.

7. An electrical circuit according to any one of Claims 1, 2 and 6 wherein said transistor has substantially no drain current at zero gate-to-source bias voltage.

8. An electrical circuit including a field-effect transistor, substantially as herein described with reference to Figures 1 and 2 and 4 of the accompanying drawings.

9. An electrical circuit including a field-effect transistor, substantially as herein described with reference to Figures 1 and 2 and 5 of the accompanying drawings.

10. An electrical circuit including a field-effect transistor, substantially as herein described with reference to Figures 1 and 2 and 6 of the accompanying drawings.

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