MICROELECTRONIC DEVICES AND METHODS FOR PACKAGING MICROELECTRONIC DEVICES

TECHNICAL FIELD

The present invention relates to packaging microelectronic devices and, in particular, methods for packaging microelectronic devices at the wafer level and microelectronic devices formed by such methods.

BACKGROUND

Microelectronic devices are used in cell phones, pagers, personal digital assistants, computers, and many other products. A packaged microelectronic device can include a microelectronic die, an interposer substrate or lead frame attached to the die, and a molded casing around the die. The microelectronic die generally has an integrated circuit and a plurality of bond-pads coupled to the integrated circuit. The bond-pads are coupled to terminals on the interposer substrate or lead frame. The interposer substrate can also include ball-pads coupled to the terminals by traces in a dielectric material. An array of solder balls is configured so that each solder ball contacts a corresponding ball-pad to define a "ball-grid array." Packaged microelectronic devices with ball-grid arrays are generally higher grade packages that have lower profiles and higher pin counts than conventional packages that use a lead frame.

Packaged microelectronic devices are typically made by (a) forming a plurality of dies on a semiconductor wafer, (b) cutting the wafer to singulate the dies, (c) attaching individual dies to an interposer substrate, (d) wire-bonding the bond-pads of the dies to the terminals of the interposer substrate, and (e) encapsulating the dies with a molding compound. It is, however, time consuming

and expensive to mount individual dies to interposer substrates or lead frames. Also, as the demand for higher pin counts and smaller packages increases, it becomes more difficult to form robust wire-bonds that can withstand the forces involved in molding processes. Moreover, the handling processes for attaching individual dies to interposer substrates or lead frames may damage the bare dies. Packaging processes, therefore, have become a significant factor in producing semiconductor devices and other types of microelectronic devices.

Another process for packaging microelectronic devices is wafer-level packaging. In wafer-level packaging, a plurality of microelectronic dies are formed on a wafer, and then a redistribution layer is formed over the dies. The redistribution layer has a dielectric layer, a plurality of ball-pad arrays on the dielectric layer, and conductive traces in the dielectric layer that are coupled to individual ball-pads of the ball-pad arrays. Each ball-pad array is arranged over a corresponding die, and the ball-pads in each array are coupled to corresponding bond-pads of the corresponding die by conductive traces. After forming the redistribution layer on the wafer, a highly accurate stenciling machine deposits discrete masses of solder paste onto the individual ball-pads. The solder paste is then reflowed to form small solder balls or "solder bumps" on the ball-pads. After forming the solder balls, the wafer is singulated to separate the individual microelectronic devices from one another.

Wafer-level packaging is a promising development for increasing efficiency and reducing the cost of manufacturing microelectronic devices. By "pre-packaging" individual dies with a redistribution layer before cutting the wafers to singulate the dies, sophisticated semiconductor processing techniques can be used to form smaller arrays of solder balls. Additionally, wafer-level packaging is an efficient process that simultaneously packages a plurality of dies, thereby reducing costs and increasing throughput.

Packaged microelectronic devices can also be produced by "build-up" packaging. For example, a sacrificial substrate can be attached to a panel that includes a plurality of microelectronic dies and an organic filler that couples the

dies together. The sacrificial substrate is generally a ceramic disc and it is attached to the active side of the dies. Next, the back side of the dies is thinned and a ceramic layer is attached to the back side. The sacrificial substrate is then removed from the active side of the dies and build-up layers or a redistribution layer is formed on the active side of the dies.

The build-up packaging process, however, has several drawbacks. For example, the build-up process is relatively expensive and may not be used on equipment set up for circular substrates. Furthermore, the resulting packaged microelectronic devices may not be stacked on top of each other to reduce the surface area or "footprint" of the devices on a printed circuit board. Accordingly, there is a need for an efficient and cost-effective process to package microelectronic devices that are stackable.

SUMMARY

The present invention is directed toward methods for packaging microelectronic devices and microelectronic devices formed by such methods. One aspect of the invention is directed toward a method for packaging microelectronic devices including microelectronic dies having a first side with a plurality of bond-pads and a second side opposite the first side. In one embodiment, the method includes providing a plurality of singulated microelectronic dies, coupling the individual dies to a support member, covering the dies and at least a portion of the support member with a dielectric layer, forming a plurality of vias through the dielectric layer between the dies, and fabricating a plurality of conductive links in corresponding vias. The conductive links can be electrically coupled to the dies.

In one aspect of this embodiment, providing the dies includes forming the dies on a microelectronic workpiece and cutting the microelectronic workpiece to separate the dies from each other before coupling the dies to the support member. The dies can be spaced apart by a first distance on the microelectronic workpiece and a second distance on the support member. The second distance

is greater than the first distance such that the dies are spaced farther apart from each other on the support member than when they are part of the workpiece. In another aspect of this embodiment, the method can include forming apertures in the support member that are aligned with corresponding vias in the dielectric layer. The conductive links can extend into the apertures. In another aspect of this embodiment, the method can include removing the support member from the dies and the dielectric layer.

Another aspect of the invention is directed toward a plurality of microelectronic devices. In one embodiment, the microelectronic devices include a support member, a plurality of microelectronic dies coupled to the support member, a dielectric layer over the dies and at least a portion of the support member, and a plurality of conductive links extending from a first surface of the dielectric layer to a second surface of the dielectric layer. The dies include an integrated circuit and a plurality of bond-pads coupled to the integrated circuit, and the conductive links are disposed between the dies. In one aspect of this embodiment, the support member includes apertures and the conductive links are at least partially disposed in corresponding apertures. In another aspect of this embodiment, the devices further include a cover over at least a portion of the dielectric layer. In another aspect of this embodiment, the devices further include a plurality of pads in and/or on the support member that are electrically coupled to corresponding conductive links. The pads may not be aligned with the conductive links.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1F illustrate various stages in a method of packaging microelectronic devices in accordance with one embodiment of the invention.

Figure 1A is a schematic side cross-sectional view of a microelectronic workpiece having a plurality of microelectronic dies.

Figure 1B is a schematic side cross-sectional view of a plurality of microelectronic devices after attaching the microelectronic dies to a mounting member.

Figure 1C is a schematic side cross-sectional view of the microelectronic devices after forming a plurality of conductive lines.

Figure 1D is a schematic side cross-sectional view of the microelectronic devices after forming a plurality of ball-pads and a plurality of conductive links.

Figure 1E is a schematic side cross-sectional view of the microelectronic devices after forming a second portion of the conductive links in the support member.

Figure 1F is a schematic side cross-sectional view of an upper microelectronic device stacked on top of a lower microelectronic device.

Figure 2 is a schematic side cross-sectional view of a plurality of microelectronic devices in accordance with another embodiment of the invention.

Figure 3 is a schematic side cross-sectional view of a plurality of microelectronic devices in accordance with another embodiment of the invention.

DETAILED DESCRIPTION

The following disclosure describes several embodiments of microelectronic devices and methods for packaging microelectronic devices. Many specific details of the present invention are described below with reference to semiconductor devices. The term "microelectronic workpiece," however, is used throughout to include substrates upon which and/or in which microelectronic devices, micromechanical devices, data storage elements, read/write components, and other features are fabricated. For example, microelectronic workpieces can be semiconductor wafers (e.g., silicon or gallium arsenide wafers), glass substrates, insulative substrates, and many other types of substrates. Many specific details of several embodiments of the invention are described below with reference to microelectronic devices including microelectronic dies in order to provide a thorough understanding of such

embodiments. A person of ordinary skill in the art will understand, however, that the invention may have other embodiments with additional elements or without several of the elements shown and described with reference to the embodiments of Figures 1A-3.

A. Microelectronic Devices and Methods For Packaging Microelectronic Devices

Figures 1A-1F illustrate various stages in a method of packaging microelectronic devices in accordance with one embodiment of the invention. Figure 1A, more specifically, is a schematic side cross-sectional view of a microelectronic workpiece 102 having a plurality of microelectronic dies 110 (identified individually as 110a-c). The microelectronic dies 110 can include an integrated circuit 112, a first side 116 having a plurality of bond-pads 114 electrically coupled to the integrated circuit 112, and a second side 118 opposite the first side 116. The dies 110 are typically individual components such that the integrated circuits 112 and bond-pads 114 are specific to each die 110. The dies 110 are formed on the microelectronic workpiece 102 in an arrangement in which the dies 110 are spaced apart from each other by, at most, a first distance D_1. After forming the dies 110, the microelectronic workpiece 102 is cut along lines A_1-A_1 to singulate the dies 110.

Figure 1B is a schematic side cross-sectional view of a plurality of microelectronic devices 100 (identified individually as 100a-b) after attaching the microelectronic dies 110 to a support member 104. After cutting the workpiece 102 of Figure 1A to separate the dies 110 into individual devices, the second side 118 of the microelectronic dies 110 can be attached to a first surface 106 of the support member 104. The support member 104 can be a separate substrate made of silicon, glass, or other suitable materials. Moreover, the support member 104 can be a tape, such as a polyimide tape or wafer-mounting tape. The dies 110 are arranged such that the dies 110 are spaced apart from adjacent dies 110 by at least a second distance D_2. The second distance D_2 is greater than the first distance D_1 (Figure 1A), and thus the spacing between the dies 110 is greater on

the support member 104 than on the workpiece 102 (Figure 1A). In one aspect of this embodiment, the microelectronic dies 110 can be tested to ensure that they function properly before they are attached to the support member 104 to enhance the reliability of the packaged microelectronic devices 100.

After attaching the dies 110 to the support member 104, a first dielectric layer 130 is deposited across the dies 110 and across the exposed areas of the first surface 106 of the support member 104 between the dies 110. The first dielectric layer 130 has a first surface 132, a second surface 134 opposite the first surface 132, and a thickness T_1. A plurality of vias 150 and 160 are then formed in the dielectric layer 130. More specifically, portions of the first dielectric layer 130 directly above the bond-pads 114 of the dies 110 are removed to form the vias 150 that extend from the first surface 132 of the first dielectric layer 130 to the bond-pads 114. In addition, portions of the first dielectric layer 130 between the dies 110 are removed to form the vias 160. The vias 160 extend from the first surface 132 of the first dielectric layer 130 to the second surface 134. In this embodiment, two of the vias 160 are illustrated between the dies 110. In other embodiments, however, a different number of the vias 160 can be formed in the first dielectric layer 130 between the dies 110. The vias 150 and 160 can be formed by etching, drilling, or other suitable methods.

Figure 1C is a schematic side cross-sectional view of the microelectronic devices 100 after forming a plurality of conductive lines 154 coupled to corresponding bond-pads 114. After forming the vias 150 in the first dielectric layer 130, the conductive lines 154 are formed on the microelectronic devices 100. The conductive lines 154 can be discrete traces that have a first end 153 electrically coupled to individual bond-pads 114 of the dies 110 and a second end 155 opposite the first end 153. In addition, a first portion of a plurality of conductive links 164a is formed in the vias 160. In one aspect of this embodiment, the first portions of the conductive links 164a are electrically coupled to corresponding bond-pads (not shown) on the dies 110. In other embodiments, as discussed in greater detail below, the first portion of the conductive links 164a

may not be coupled to the bond-pads of the dies 110. In another aspect of this embodiment, the conductive lines 154 and the first portion of the conductive links 164a can be formed by sputtering a thin film of a conductive material across the first dielectric layer 130 including the vias 150 and 160. The conductive material can be titanium, copper or another suitable conductive material. Portions of the conductive material can be removed by etching to form the conductive lines 154 and the first portion of the conductive links 164a. In other embodiments, the conductive lines 154 and the first portion of the conductive links 164a can be formed separately and by other suitable methods.

After forming the conductive lines 154 and the first portion of the conductive links 164a, a second dielectric layer 170 is deposited across the microelectronic devices 100. Next, portions of the second dielectric layer 170 proximate to the second ends 155 of the conductive lines 154 are removed to form a plurality of vias 152. Furthermore, portions of the second dielectric layer 170 proximate to the first portion of the conductive links 164a are removed to form a plurality of vias 162.

Figure 1D is a schematic side cross-sectional view of the microelectronic devices 100 after forming a plurality of ball-pads 156 and a plurality of second portions of the conductive links 164b. After forming the vias 152 in the second dielectric layer 170, arrays of the ball-pads 156 can be formed in the vias 152. Each array of ball-pads 156 can be associated with a corresponding die 110, and each ball-pad 156 in an array can be electrically coupled to a corresponding bond-pad 114 of the die 110 by a conductive line 154. In addition, the second portion of the conductive links 164b can be formed on the first portion of the conductive links 164a in the vias 162. Together, the first and second portions of the conductive links 164a-b form a plurality of conductive links 165 that extend through the first and second dielectric layers 130 and 170 to the first surface 106 of the support member 104. Next, a plurality of solder balls 174 can be deposited on the corresponding ball-pads 156 and the corresponding conductive links 165 proximate to a first surface 172 of the second dielectric layer 170.

In one aspect of this embodiment, the second portion of the conductive links 164b can be formed by depositing solder paste into the vias 162 or electroplating a conductive material such as copper. In other embodiments, the conductive links 165 can be formed by other methods. In one aspect of this embodiment, the conductive links 165 can include ball-pads (not shown) proximate to the first surface 172 of the second dielectric layer 170. In another aspect of this embodiment, the conductive links 165 can be electrically coupled to the microelectronic dies 110. In other embodiments, the conductive links 165 can include pass-through circuitry and not be electrically coupled to the dies 110.

Figure 1E is a schematic side cross-sectional view of the microelectronic devices 100 after forming a third portion of the conductive links 164c in the support member 104. In one aspect of this embodiment, portions of the support member 104 that are aligned with the conductive links 165 can be removed to create a plurality of apertures 163. Next, the third portion of the conductive links 164c can be formed in the apertures 163 and form part of the conductive links 165. The third portion of the conductive links 164c can include ball-pads or contacts. Accordingly, the conductive links 165 can extend from the first surface 172 of the second dielectric layer 170 to the second surface 105 of the support member 104. After forming the conductive links 165 through the first dielectric layer 130, the second dielectric layer 170, and the support member 104, the assembly can be cut along lines A_2-A_2 to singulate the microelectronic devices 100. In additional embodiments, such as those described below with reference to Figure 3, the conductive links 165 may not extend through the support member 104. In other embodiments, a plurality of apertures can be formed in the support member 104 before the first dielectric layer 130 is deposited (as shown in Figure 1B), and the first portion of the conductive links 164a can be formed in the apertures of the support member 104. In additional embodiments, portions of the support member 104 can be removed to form the apertures 163 when the vias 160 are formed in the first dielectric layer 130. In other embodiments, the solder

balls can be deposited on the conductive links 165 after the conductive links 165 are formed in the support member 104.

Figure 1F is a schematic side cross-sectional view of an upper microelectronic device 200 stacked on top of a lower microelectronic device 300. The upper and lower microelectronic devices 200 and 300 can be generally similar to the microelectronic devices 100 described above with reference to Figures 1B-1E. For example, the upper and lower microelectronic devices 200 and 300 each include a microelectronic die 110 (identified individually as 110a-b). The microelectronic dies 110 can be the same type of die, or the dies 110 can be different types. The upper microelectronic device 200 is coupled to the lower microelectronic device 300 by attaching the conductive links 165 of the upper microelectronic device 200 to the solder balls 174 on the conductive links 165 of the lower microelectronic device 300. In this embodiment, the upper microelectronic device 200 does not include pads or contacts that are coupled to the solder balls 174 on the ball-pads 156 of the lower microelectronic device 300. In other embodiments, such as those described below with reference to Figure 2, the ball-pads 156 of one microelectronic device can be electrically coupled to another microelectronic device when the devices are stacked. In one aspect of the illustrated embodiment, the upper microelectronic device 200 can be attached to a printed circuit board before or after the lower microelectronic device 300 is attached. In other embodiments, one microelectronic device can be attached to a support member and multiple microelectronic devices can be stacked on top of the single device.

One advantage of the microelectronic devices is that they can be stacked on top of each other. Stacking microelectronic devices increases the capacity or performance of a device within a given surface area or footprint on a circuit board. For example, when a second microelectronic device is stacked on top of a first microelectronic device, the second microelectronic device is electrically and operably coupled to the circuit board without using significantly more surface area on the circuit board. Another advantage of the microelectronic devices 100 is that

the conductive links 165 and the solder balls 174 create a redistribution system with a greater pitch (i.e., greater distance between the solder balls). A greater pitch between solder balls allows for a greater pitch between corresponding contacts on a circuit board. Circuit boards with a greater pitch between contacts are cheaper and easier to manufacture. Moreover, a greater pitch may allow the microelectronic devices to use a standard rather than a custom ball-grid array pitch.

B. Other Microelectronic Devices

Figure 2 is a schematic side cross-sectional view of a plurality of microelectronic devices 400 in accordance with another embodiment of the invention. The microelectronic devices 400 are generally similar to the microelectronic devices 100 described above with reference to Figures 1B-1E. For example, the microelectronic devices 400 include a support member 404, a plurality of microelectronic dies 110 coupled to the support member 404, first and second dielectric layers 130 and 170 over the support member 404, a plurality of solder balls 174 on corresponding ball-pads 156 in the second dielectric layer 170, and a plurality of conductive links 165 that extend through the microelectronic devices 400. The mounting member 404 includes a plurality of pads 480 and a plurality of conductive lines 482 electrically coupling the pads 480 to corresponding conductive links 165. In one aspect of this embodiment, the mounting member 404 can be a polyimide tape having pads and interconnecting circuitry. In other embodiments, the pads 480 can be formed on and/or in the mounting member 404. The pads 480 on the microelectronic devices 400 can be arranged to contact corresponding solder balls 174 on other microelectronic devices 400 when the devices 400 are stacked.

Figure 3 is a schematic side cross-sectional view of a plurality of microelectronic devices 500 in accordance with another embodiment of the invention. The microelectronic devices 500 are generally similar to the microelectronic devices 100 described above with reference to Figures 1B-1E. For example, the microelectronic devices 500 include a plurality of microelectronic

dies 110, first and second dielectric layers 130 and 170 over the dies 110, a plurality of arrays of ball-pads 156 in the second dielectric layer 170, and a plurality of conductive links 165 that extend through the dielectric layers 130 and 170. In one aspect of this embodiment, the microelectronic devices 500 do not include a mounting member attached to the dies 110. The microelectronic devices 500 can be fabricated on a mounting member and the mounting member can be removed during the manufacturing process. Alternatively, the microelectronic devices 500 can be fabricated without a mounting member. The lack of a mounting member creates a thinner microelectronic device 500 and/or allows for a heat sink to be attached to the dies 110. In another aspect of this embodiment, the microelectronic devices 500 do not include solder balls on the ball-pads 156. In other embodiments, the ball-pads 156 may include solder balls. In another aspect of this embodiment, the microelectronic devices 500 are encapsulated to form a cover 590 over the second dielectric layer 170. The cover 590 protects the microelectronic devices 500 from air, dirt, moisture and other contaminants. In other embodiments, the microelectronic devices 500 may include a cover over the second side 118 of the microelectronic dies 110 and/or may not include the cover 590 over the second dielectric layer 170.

From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A method for packaging microelectronic devices, comprising:

providing a plurality of singulated microelectronic dies;

coupling the plurality of individual microelectronic dies to a support member;

covering the dies and at least a portion of the support member with a dielectric layer;

forming a plurality of vias through the dielectric layer between the dies;

fabricating a plurality of conductive links in corresponding vias; and

removing the support member from the dies and the dielectric layer.

2. The method of claim 1 wherein providing the microelectronic dies comprises:

forming the dies on a microelectronic workpiece; and

cutting the microelectronic workpiece to separate the dies from each other before coupling the dies to the dielectric substrate.

3. The method of claim 1 wherein providing the microelectronic dies comprises:

forming the dies on a microelectronic workpiece, wherein the dies are spaced apart by a first distance; and

cutting the microelectronic workpiece to separate the dies from each other before coupling the dies to the dielectric substrate;

wherein coupling the dies to the dielectric substrate comprises spacing apart the dies a second distance greater than the first distance.

4. The method of claim 1, further comprising testing the dies before coupling the dies to the dielectric substrate.

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5. The method of claim 1, further comprising forming a plurality of ball-pad arrays on and/or in the dielectric layer, wherein the ball-pad arrays are electrically coupled to corresponding dies.

6. The method of claim 1 wherein the dies comprise a first die and a second die, wherein fabricating conductive links comprises forming ball-pads on and/or in the dielectric layer, and wherein the method further comprises:

depositing a plurality of solder balls on corresponding ball-pads;

cutting the dielectric substrate and the dielectric layer to separate the first and second dies; and

stacking the first die on top of the second die.

7. The method of claim 1 wherein fabricating the conductive links comprises electrically coupling the conductive links to corresponding dies.

8. The method of claim 1, further comprising forming a plurality of apertures in the dielectric substrate aligned with corresponding conductive links.

9. The method of claim 1 wherein the plurality of conductive links comprises a first plurality of conductive links, and wherein the method further comprises:

forming a plurality of apertures in the dielectric substrate aligned with corresponding conductive links; and

forming a second plurality of conductive links in corresponding apertures.

10. The method of claim 1, further comprising encapsulating at least a portion of the dielectric layer and/or the dielectric substrate.

11. The method of claim 1 wherein the dies comprise a first die and a second die, wherein forming the vias comprises forming first and second vias

between the first and second dies, and wherein the first via is spaced apart from the second via.

12. The method of claim 1, further comprising forming a plurality of pads in and/or on the dielectric substrate, the pads being electrically coupled to and not aligned with corresponding conductive links.

13. A method for stacking microelectronic devices, comprising:

providing a first microelectronic device having a first dielectric substrate, a first microelectronic die having a first side with bond-pads and a second side attached to the first dielectric substrate, a first dielectric layer over the first die, and a first plurality of conductive links extending through the first dielectric layer and the first dielectric substrate;

providing a second microelectronic device having a second dielectric substrate, a second microelectronic die having a first side with bond-pads and a second side attached to the second dielectric substrate, a second dielectric layer over the second die, a second plurality of conductive links extending through the second dielectric layer and the second dielectric substrate, and solder balls at least partially aligned with the second conductive links; and

stacking the second microelectronic device on top of the first microelectronic device with the first plurality of conductive links aligned with and electrically coupled to corresponding solder balls that are at least partially aligned with conductive links in the second plurality of conductive links.

14. The method of claim 13 wherein providing a first microelectronic device comprises:

constructing the first microelectronic die on a microelectronic workpiece;

cutting the microelectronic workpiece to separate the first microelectronic die;

coupling the first microelectronic die and a first plurality of microelectronic dies to the first dielectric substrate; and

cutting the first dielectric substrate to separate the first microelectronic device.

15. The method of claim 13 wherein providing a first microelectronic device comprises encapsulating at least a portion of the first dielectric layer.

16. The method of claim 13 wherein:

providing a first microelectronic device comprises depositing a plurality of solder balls on corresponding first conductive links; and

wherein stacking the first and second microelectronic devices comprises coupling the second conductive links to corresponding solder balls.

17. The method of claim 13 wherein providing a first microelectronic device comprises forming a plurality of pads in and/or on the first dielectric substrate that are electrically coupled to corresponding first conductive links.

18. A plurality of microelectronic devices, comprising:

a dielectric support member;

a plurality of microelectronic dies coupled to the dielectric support member, the individual dies having an integrated circuit, a first side facing away from the support member and having a plurality of bond-pads coupled to the integrated circuit, and a second side attached to the support member;

a dielectric layer over the dies and at least a portion of the support member, the dielectric layer having a first surface and a second surface opposite the first surface;

a plurality of conductive links extending from the first surface of the dielectric layer to the second surface, wherein the conductive links are between the dies; and

a plurality of external pads at least partially aligned with corresponding conductive links.

19. The microelectronic devices of claim 18 wherein the support member comprises a polyimide tape.

20. The microelectronic devices of claim 18 wherein the support member comprises a plurality of apertures, and wherein the conductive links are at least partially disposed in corresponding apertures.

21. The microelectronic devices of claim 18 wherein at least a portion of the conductive links are electrically coupled to corresponding dies.

22. The microelectronic devices of claim 18, further comprising a cover over at least a portion of the dielectric layer.

23. The microelectronic devices of claim 18 wherein:

the dies comprise first and second dies; and

the conductive links comprise first and second conductive links disposed between the first and second dies.

24. The microelectronic devices of claim 18, further comprising a plurality of pads at the support member, the pads being electrically coupled to corresponding conductive links and not aligned with the conductive links.