WHAT IS CLAIMED IS:

1. A vertical memory device, comprising:

conductive lines stacked on a substrate, the conductive lines being spaced apart from each other in a vertical direction perpendicular to an upper surface of the substrate, and each of the conductive lines extending lengthwise in a first direction parallel to the upper surface of the substrate;

first and second semiconductor patterns extending through the conductive lines in the vertical direction;

first and second pads on the first and second semiconductor patterns, respectively;

first and second electrodes electrically connected to the first and second pads, respectively;

a third electrode electrically connected to a first conductive line of the conductive lines; and

a first division pattern extending lengthwise in a second direction parallel to the upper surface of the substrate and crossing the first direction, the first division pattern extending through and dividing the first conductive line,

wherein in a plan view, the first and second semiconductor patterns and a portion of the first conductive line are disposed at one side of the first division pattern, and

wherein the first and second semiconductor patterns, the first and second pads, and the portion of the first conductive line form a transistor.

2. The vertical memory device of claim 1, wherein the first conductive line is disposed at an uppermost level among levels at which the conductive lines are respectively disposed.

3. The vertical memory device of claim 1, wherein the first conductive line is disposed at a second level from above among levels at which the conductive lines are respectively disposed.

4. The vertical memory device of any one of claims 1 to 3, wherein the first division pattern extends lengthwise through ones of the conductive lines at an uppermost level and a second level from above.

5. The vertical memory device of any one of claims 1 to 4,

wherein a plurality of first division patterns is disposed in the first direction, each of the plurality of first division patterns dividing the first conductive line, and

wherein a plurality of first semiconductor patterns, a plurality of second semiconductor patterns, a plurality of first electrodes, a plurality of second electrodes, and a plurality of third electrodes are formed in the first direction.

6. The vertical memory device of any one of claims 1 to 5, further comprising:

a second division pattern connected to the first division pattern, the second division pattern extending in the first direction to penetrate through and divide the first conductive line.

7. The vertical memory device of claim 6,

wherein the first division pattern includes a pair of first division patterns spaced apart from each other in the first direction, and

wherein the first and second semiconductor patterns and the first conductive line are

formed in a space between the pair of first division patterns.

8. The vertical memory device of claim 7, wherein the second division pattern crosses the pair of first division patterns to divide the space between the pair of first division patterns into two spaces.

9. The vertical memory device of claim 8, wherein in a plan view, the first and second semiconductor patterns and the first to third electrodes are disposed in one of the two spaces formed by the pair of first division patterns and the second division pattern.

10. The vertical memory device of claim 8 or claim 9, wherein in a plan view, the first and second semiconductor patterns and the first to third electrodes are disposed in each of the two spaces formed by the pair of first division patterns and the second division pattern.

11. The vertical memory device of any one of claims 1 to 10, further comprising:

a third semiconductor pattern commonly contacting lower surfaces of the first and second semiconductor patterns to connect the first and second semiconductor patterns with each other.

12. The vertical memory device of claim 11,

wherein the first division pattern includes a pair of first division patterns spaced apart from each other in the first direction, and

wherein in a plan view, the third semiconductor pattern is disposed between the pair of first division patterns.

13. The vertical memory device of any one of claims 1 to 10, further comprising:

circuit patterns on the substrate;

an insulating interlayer covering the circuit patterns;

a base pattern on the insulating interlayer; and

a third semiconductor pattern commonly contacting lower surfaces of the first and second semiconductor patterns to connect the first and second semiconductor patterns with each other;

wherein the conductive lines are stacked on the base pattern, and

wherein the first to third semiconductor patterns, the first and second pads, and the first conductive line form the transistor.

14. The vertical memory device of any one of claims 1 to 13, wherein a source voltage is applied to the first electrode, a drain voltage is applied to the second electrode, and a gate voltage is applied to the third electrode.

15. A vertical memory device, comprising:

conductive lines stacked on a substrate, the conductive lines being spaced apart from each other in a vertical direction perpendicular to an upper surface of the substrate, and each of the conductive lines extending lengthwise in a first direction parallel to the upper surface of the substrate;

semiconductor patterns extending through the conductive lines in the vertical direction;

conductive pads on the semiconductor patterns, respectively;

source and drain electrodes electrically connected to first and second pads,

respectively, of the conductive pads;

a gate electrode electrically connected to a first conductive line of the conductive lines; and

a pair of first division patterns, each of the pair of first division patterns extending lengthwise in a second direction and dividing the first conductive line, the second direction being parallel to the upper surface of the substrate and crossing the first direction,

wherein first and second semiconductor patterns under the first and second pads, respectively, among the semiconductor patterns are connected with each other, and

wherein in a plan view, the first and second pads, the first and second semiconductor patterns, and a portion of the first conductive line are disposed between the pair of first division patterns to form a transistor.

16. The vertical memory device of claim 15, wherein the first conductive line is disposed at an uppermost level among levels at which the conductive lines are respectively disposed.

17. The vertical memory device of claim 15 or claim 16, wherein the first and second semiconductor patterns are connected with each other by a third semiconductor pattern commonly contacting lower surfaces of the first and second semiconductor patterns on the substrate.

18. The vertical memory device of claim 17, wherein in a plan view, the third semiconductor pattern is disposed between the pair of first division patterns.

19. A vertical memory device, comprising:

conductive lines stacked on a substrate in a vertical direction perpendicular to an upper surface of the substrate, the substrate including first and second regions;

channels extending through the conductive lines in the vertical direction;

conductive pads on the channels, respectively, the conductive pads including first pads on the first region of the substrate and second and third pads on the second region of the substrate;

a first wiring for applying a first signal to the first pads on the first region of the substrate;

second and third wirings for applying second and third signals to the second and third pads, respectively, on the second region of the substrate, the second and third wirings being different from the first wiring; and

a fourth wiring for applying a fourth signal to a portion of one conductive line among the conductive lines on the second region of the substrate,

wherein the second and third pads, the channels under the second and third pads, respectively, and the portion of one conductive line form a transistor.

20. The vertical memory device of claim 19, further comprising:

circuit patterns on the substrate;

an insulating interlayer covering the circuit patterns; and

a base pattern on the insulating interlayer,

wherein the conductive lines are stacked on the base pattern.