METHOD TO REMOVE SPACER AFTER SALICIDATION TO ENHANCE CONTACT ETCH STOP LINER STRESS ON MOS

Abstract

An example process to remove spacers from the gate of a NMOS transistor. A stress creating layer is formed over the NMOS and PMOS transistors and the substrate. In an embodiment, the spacers on gate are removed so that stress layer is closer to the channel of the device. The stress creating layer is preferably a tensile nitride layer. The stress creating layer is preferably a contact etch stop liner layer. In an embodiment, the gates, source and drain region have a silicide layer thereover before the stress creating layer is formed. The embodiment improves the performance of the NMOS transistors.

Figure 7