NITRIDE AS AN ETCHBACK OR CMP STOP IN INTERLAYER DIELECTRIC PLANARIZATION INCORPORATING LOW DIELECTRIC CONSTANT SPIN-ON POLYMER

ABSTRACT

A method for preserving the integrity of the underlying metal lines during planarization by inserting a nitride layer as an etch stop in an oxide-nitride-oxide dielectric layer underlying a spin-on polymer is described. Semiconductor device structures are provided in and on a semiconductor substrate. A conducting layer is deposited overlying the surfaces of the semiconductor device structures and patterned to form conducting lines wherein a gap is formed between the conducting lines. A first dielectric layer is deposited over the surfaces of the conducting lines wherein the first dielectric layer contains an etch stop layer wherein the gap remains between the conducting lines. A second dielectric layer is deposited overlying the first dielectric layer wherein the gap is filled by the second dielectric layer. The second dielectric layer is etched back so that the second dielectric layer remains only within the gap wherein the etch stop layer preserves the integrity of the underlying conducting lines. A third dielectric layer is deposited over the first and second dielectric layers and planarized. Alternatively, instead of etching back the second dielectric layer, chemical mechanical polishing (CMP) is used to planarize the layer wherein the etch stop acts as a CMP stop. A third dielectric layer is then deposited over the substrate to complete fabrication of the integrated circuit device.

(FIGURE 3 IS SUGGESTED FOR PUBLICATION)