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A CIRCUIT FOR GENERATING A SCROLL WINDOW SIGNAL IN
DIGITAL IMAGE APPARATUS

This invention relates to a circuit for generating a scroll window signal in digital image apparatus, and particularly to a circuit for generating a scroll window signal capable of displaying two different screen sources, one on the right and the other on the left section of a common screen simultaneously.

Techniques of displaying more than two screen sources simultaneously on a common screen, such as a picture-in-picture system and a scroll screen displaying system are known. The picture-in-picture system, which inserts a small screen into a main screen having a different screen source, has an advantage that it can display an entire original source screen. However, it has a shortcoming that, due to the small screen size, it can not be viewed easily at long distances.

A known technique displays two screens having different screen sources simultaneously on a common screen, one on the top and the other on the bottom, or one on the right and the other on the left respectively. The system displays either the two pictures with the same size or one of them with a larger size and the other with a smaller size. In the scroll window displaying system, although both pictures may be full-sized, only respective parts of each picture may be viewed simultaneously.

When a multiple screen is selected and displayed, in a conventional scroll window

displaying system, the desired portion of the screen is displayed by setting a window by means of handling selection keys for top and bottom or right and left control. However, the top and bottom or the right and left window scrolling method utilises different screen selecting window pulses according to the types of scroll screen. Then, each screen scroll type is selected by a decoded window signal.

Therefore, this may have a disadvantage that the selection logic circuit for selecting screen scroll types becomes complicated and the capacity for logic signal processing must be relatively high.

Preferred embodiments of the invention aim :

- to provide a circuit for comparing scroll screen mode signals for discriminating a given mode by means of (+), (-) key input signal representing a scroll type;
- to provide a circuit for generating a scroll screen window signal suitable to a scroll screen mode; and
- to provide a circuit capable of displaying on a displaying device a desired scroll screen by separating vertically a screen which is corresponding to a given scroll mode.

According to a first aspect of the present invention, there is provided a scroll window generating circuit for use in digital image processing apparatus, the circuit comprising:

a first counter means connected to receive a clock input and arranged to count from an initial count value in response to a START signal;

a second counter means arranged to count upwardly and downwardly from a preset value, in response to UP and DOWN count signals input by a user;

a comparator means connected to receive count outputs from said first and second counter means and to generate or modify a scroll window signal when the count outputs from said first and second counter means have a predetermined mutual relationship; and

means for resetting said first and second counter means to said initial count value and said preset value, respectively.

Preferably, said first counter means comprises two counter circuits connected to count sequentially, each counter circuit being connected to receive CLEAR and CLOCK pulses simultaneously on respective inputs of the counter circuits.

The scroll window generating circuit may include an OR gate for receiving a clock signal on one input thereof and passing the clock signal to the first counter means.

The said OR gate may be connected to receive said scroll window signal on an another input thereof, whereby said clock signal is inhibited when said scroll window signal is generated or modified.

Preferably, the circuit includes first and second AND gates for receiving on respective input terminals said UP and DOWN count signals when input by a user.

Said comparator means preferably comprises a plurality of exclusive-OR gates connected to receive said count outputs from said first and second counter means and compare them, and a NOR gate connected to receive the outputs of said exclusive-OR gates and to output or modify said scroll window signal.

Limit means may be provided for receiving the count output of said second counter means and inhibiting counting up or counting down of said second counter means when the count output thereof is at an upper or lower limit respectively.

Such limit means may comprise first and second NAND gates, each connected to receive an n-bit output of the second counter means through a respective array of inverters. Then, said first and second AND gates are preferably connected to receive the outputs of said first and second NAND gates.

The invention also extends to image processing apparatus including a scroll window generating circuit according to the first aspect of the invention.

In such image processing apparatus, said clock signal preferably has a frequency of 3.58 MHz.

Preferably, said means for resetting said first counter means to said initial count value is arranged to divide a synchronising signal of the image processing apparatus in order to provide a synchronous RESET signal to which said first counter means responds.

The image processing apparatus preferably includes display means for displaying on a common screen

two separate screen images each of which comprises a window formed in the other, and scrolling means for scrolling the point of division of the two images.

The said scrolling means is preferably arranged to respond to the count output of said first counter means, which count output represents the degree of scrolling - that is, the point of division of said two images.

Preferably, said two images are arranged to occupy respectively a left and a right portion of said common screen, such that said point of division comprises a substantially upright line.

Said preset value of said second counter means preferably represents said point of division being in a middle portion of said common screen.

According to another aspect of the invention, a circuit for generating a scroll screen window signal comprises: an OR gate for receiving a basic clock signal 3.58 MHz; a first counter CNT1 and a second counter CNT2 for receiving a synchronous signal from a synchronized-divider and receiving an output of said OR gate; a first AND gate and a second AND gate for receiving a right/left scroll window selecting signal generated by a user; a third counter CNT3 for receiving a scroll window selecting signal from a fifth input terminal and generating a scroll window setting signal; a plurality of exclusive OR gates and a NOR gate for receiving outputs counted from said second counter and said third counter, comparing the outputs, logicizing them, and generating a scroll window signal to be input to said OR gate; and a

first NAND gate and a second NAND gate for receiving the output of said second counter after inverting outputs of said second counter in a given manner.

For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1 is a circuit diagram of one embodiment of the invention;

Figure 2 is an operational diagram illustrating one example of a scroll window screen of a preferred embodiment of the invention; and

Figure 3 is an operational waveform diagram illustrating one example of operation of the embodiment of Figure 1.

Referring to Figure 1, a circuit for generating a scroll screen window signal is schematically shown, having a first counter means 100 comprising an OR gate for receiving a basic clock signal of 3.58 MHz on a first input terminal 10, and two counter circuits CNT1, CNT2 for receiving a synchronous READ-START signal from a synchronous divider (not shown) at a clear input terminal CLR. A second input terminal 20 is connected to the clear terminal CLR of each counter circuit CNT1, CNT2, each of which receives the output of the OR gate at a clock terminal CK, and according to an input signal at the second input terminal 20, counts in a given manner the signal input from the clock terminal CK.

A second counter means 200 comprises two AND gates AND1, AND2 for receiving through third and fourth input terminals 30, 40 a scroll window right/left selection signal generated by a user, and a third counter circuit CNT3 for receiving the outputs of said AND gates AND1, AND2 at count-up and count-down terminals thereof, and thereby counting in response to the outputs of the AND gates. A load terminal LOAD of the third counter CNT3 receives a scroll selection signal through a fifth input terminal 50 while input terminals A, B, C, D thereof are set for a pre-set middle position of a scroll-screen.

A Comparator means 300 comprises four exclusive-OR gates XOR2 to XOR5 for receiving the counted values from said first and second counter means 100, 200, thereby comparing said counted values, and a NOR gate NOR for logicizing the scroll window signal to produce an output signal SW, which output signal is input to the OR gate of the first counter means 100 and sets a corresponding scroll window.

A limit means 400 comprises four inverters N1 to N4 for receiving the output of the second counter means 200 to produce an inverted output to NAND gates NA1, NA2, said NAND gates generating window recognition signals corresponding to leftmost and rightmost sides of the screen, which signals are sent to said AND gates AND1 and AND2.

Figure 2 is an operational diagram showing one example of operation of the circuit of Figure 1. When a scroll screen 188, vertically set in division, is divided into twelve scroll position setting modes, it is intend to display a main screen at the

left side, and a digital sub-screen at the right side, according to the output signal SW generated at the output terminal of the NOR gate NOR of Figure 1. That is, the sizes of the right and left screens are proportionally changed according to the change of the scroll window selecting signal SW. A default window selecting signal SW shown in Figure 2 has an initial configuration 288, at which scroll function is set up automatically for an initial state - namely, the input terminals A - D of counter 3 CNT3 are set up preferentially at the value 0110.

In the example of operation, illustrated in Figure 3A :

(3a) shows a READ-START signal input to the second input terminal 20 of Figure 1;

(3b) shows the output signal at the terminal QD of the counter circuit CNT1 of Figure 1;

(3c)-(3f) show output signals at output terminals QA - QD of the counter circuit CNT2 of Figure 1;

(3g) shows a control input signal input to the fifth input terminal 50;

(3h) shows an input signal waveform of the third input terminal 30;

(3i) shows an output data waveform of the counter circuit CNT3; and

(3j) shows a scroll window signal waveform SW output from the NOR gate.

In Figure 3B, alternative operations in response to user signals input at terminals 30, 40 are illustrated. Thus (3k) corresponds to (3g) of Figure 3A; (3l) and (3m) illustrate signals input at terminals 30,40; and (3n) illustrates corresponding output signals from the counter circuit CNT3.

In Figure 1, if a user turns a scroll function key (not shown) ON, a scroll pulse becomes logic high. The scroll selecting signal of the fifth input terminal 50 is input as 3g, 3k because it is accepted as active low state. Subsequently, the READ-START signal 3a is generated by the main synchronous signal generating circuit (not shown) during scrolling, by which the two counter circuits CNT1, CNT2 are cleared. After this, the two counter circuits CNT1, CNT2 start counting from their initial zero value, which is pre-set at their respective terminals A,B,C,D.

If the whole screen 188 is set up with twelve modes as shown in Figure 2, a window 1 region is cleared at the next synchronizing interval, a reference frequency being counted 16 times and the window 1 then being generated. And the window selecting signal of a window 12 region is generated after the reference frequency is counted $16 \times 11 = 176$ times. Namely, a scroll window requires eleven windows according to the position of each screen scroll. When the scroll is initially switched "ON", the position 288 of the scroll window signal SW is automatically in the initial position as in Figure 2, corresponding to a mid-position of the scroll.

The example of Figure 2 will now be described in more detail, with reference to Figures 1 and 3.

The first and the second counters CNT1, CNT2 are cleared by each READ-START received from the second input terminal 20. Thus each READ-START signal is to match initial parts of a virtual image signal except a synchronous signal of an image synthesized signal.

After the two counter circuits CNT1, CNT2 are cleared by signal (3a) of Figure 3, an input clock signal is counted by inputting the reference frequency clock of 3.58 MHz via the first input terminal 10 to the clock terminals CK of the counter circuit CNT1, CNT2 through the OR gate, and the output signal (3b) from the output terminal (QD) of counter circuit CNT1 is output. When the ripple carry signal of the counter circuit CNT1 is carried to the counter circuit CNT2, and the input clock signal from the OR gate is counted, the output signals of the output terminals QA - QD of the counter circuit CNT2 are output as (3c)-(3f), and input to the exclusive OR gates XOR2 - XOR5. During a period of one horizontal synchronous video signal, one horizontal screen can be completely counted out by the counter circuits CNT1, CNT2, wherein a count of about 192 is needed to count all of the effective screen section.

As a result, a 5-bit-counting output out of the maximum possible output of 8 bits from the first counter means 100 is output as (3b)-(3f) in Figure 3. If a user inputs a scroll key, a signal such as (3g) (3k) in Figure 3 is generated and the load terminal LOAD of the counter circuit CNT3 is activated.

Since the states of the input terminals A, B, C, D of the third counter CNT3 are at 0110 simultaneously with the activation of the third counter CNT3, the output at the output terminals QA - QD of the counter circuit CNT3 is correspondingly output as (3i). Thereafter, it is compared with the output of the counter circuit CNT2 by the exclusive OR gates XOR2 to XOR5 and passed through the NOR gate. Then, the window selecting signal SW corresponding to the middle position of the scroll screen window in Figure. 2 is output. If the selecting signal SW is input to the OR gate OR, the pulse inputting of the counter circuits CNT1 - CNT2 is stopped, causing the counters to stop counting. This preferred example shows two different screen sources in the same size. Thus, if the two screen sources were to illustrate two different people's faces, only a half of each person's face would be displayed on the scroll screen.

If a user selects a key (+) to display the left half of the screen, the input of (3h) is input to the AND gate AND1 of the third input terminal 30. When the output of the NAND gate NA1 is input to the other input terminal of said AND gate AND1 an output of the AND gate AND1 is input to the up-counter terminal of the third counter CNT3. The third counter CNT3 is up-counted from 0110 as at (3i) and finally a sequence of 0110-0111-1000 is output from output terminals QA - QD.

The output of the third counter CNT3 is compared with the output of the output terminals QA - QD of the second counter CNT2 at the exclusive OR gates XOR2-XOR5. Then, if the outputs of the second and the third counters CNT2-CNT3 are all the same, all the

outputs of the exclusive OR gates XOR2-XOR5 become logic low, and the scroll window signal SW is generated to be logic high as at (3j), by the NOR gate NOR.

Thus, when the region 8 of a selected window point in Figure 2 is selected and the scroll window is generated, the first and the second counters CNT1, CNT2 always have logic high input to their clock terminal CK by a scroll window signal SW input to the OR gate OR, thereby stopping the count. Thereafter, the scroll window is cleared by the read-start signal input to the second input terminal 20.

If a user selects a key (-), data is input to the AND gate AND2 through the fourth input terminal 40 and the output of NAND gate NA2 is input to the other input terminal of said AND gate AND2. Therefore, if the third counter CNT3 is set for down-count by the output of the NAND gate NA2 to count down, the outputs of the output terminals QA-AD of the third counter CNT3 are down-counted and input to the exclusive OR gates XOR2-XOR5. Thereafter, the output of the third counter CNT3 is compared with the output of the second counter CNT2. According to the above compared values, when all of the values become logic low, the output of the NOR gate NOR becomes logic high. Hence a window is set such that the left scroll screen in Figure 2 is reduced and the right-sub digital screen is displayed on a large scale.

The window of scroll screen 1 in Figure 2 is readily selected by (3k) - (3n) in Fig. 3, according to the change of inputs of the third and fourth input terminals 30, 40. If the output of output terminals QA - QD of the third counter CNT3 is 0001 (corresponding to the leftmost window) or 1011 (corresponding to the

rightmost window), the outputs of the NAND gates NA1, NA2 respectively become logic low and are input to the AND gates AND1, AND2. Therefore, the outputs of the AND gates AND1, AND2 become logic low and any inputs of the third counter CNT3 are not accepted. So, the scroll screen window does not exceed over a given scope.

In the preferred embodiment according to this invention, there are 11 scroll windows on a screen. However, scroll function can be easily increased by increasing the number of scroll screen window, applying 5 bit, 6 bit, 7 bit or 8 bit instead of 4 bit.

As described above, the scroll window signal can be generated, easily and effectively, by using a picture-in-picture technique or a horizontal synchronous counter for use in other various digital processing and by key inputting with the help of an up/down counter.



CLAIMS:

1. A scroll window generating circuit for use in digital image processing apparatus, the circuit comprising:

a first counter means connected to receive a clock input and arranged to count from an initial count value in response to a START signal;

a second counter means arranged to count upwardly and downwardly from a preset value, in response to UP and DOWN count signals input by a user;

a comparator means connected to receive count outputs from said first and second counter means and to generate or modify a scroll window signal when the count outputs from said first and second counter means have a predetermined mutual relationship; and

means for resetting said first and second counter means to said initial count value and said preset value, respectively.

2. A scroll window generating circuit according to claim 1, wherein said first counter means comprises two counter circuits connected to count sequentially, each counter circuit being connected to receive CLEAR and CLOCK pulses simultaneously on respective inputs of the counter circuits.

3. A scroll window generating circuit according to claim 1 or 2, including an OR gate for receiving a clock signal on one input thereof and passing the clock signal to the first counter means.

4. A scroll window generating circuit according to claim 3, wherein said OR gate is connected to receive said scroll window signal on an another input thereof,



whereby said clock signal is inhibited when said scroll window signal is generated or modified.

5. A scroll window generating circuit according to any of claims 1 to 4, including first and second AND gates for receiving on respective input terminals said UP and DOWN count signals when input by a user.
6. A scroll window generating circuit according to any of claims 1 to 5, wherein said comparator means comprises a plurality of exclusive-OR gates connected to receive said count outputs from said first and second counter means and compare them, and a NOR gate connected to receive the outputs of said exclusive-OR gates and to output or modify said scroll window signal.
7. A scroll window generating circuit according to any of claims 1 to 6, including limit means for receiving the count output of said second counter means and inhibiting counting up or counting down of said second counter means when the count output thereof is at an upper or lower limit respectively.
8. A scroll window generating circuit according to claim 7, wherein said limit means comprises first and second NAND gates, each connected to receive an n-bit output of the second counter means through a respective array of inverters.
9. A scroll window generating circuit according to claims 5 and 8, wherein said first and second AND gates are connected to receive the outputs of said first and second NAND gates.
10. A scroll window generating circuit substantially



as hereinbefore described with reference to the accompanying drawings.

11. Image processing apparatus including a scroll window generating circuit according to any of the preceding claims.

12. Image processing apparatus according to claim 11, wherein said clock signal has a frequency of 3.58 MHz.

13. Image processing apparatus according to claim 11 or 12, wherein said means for resetting said first counter means to said initial count value is arranged to divide a synchronising signal of the image processing apparatus in order to provide a synchronous RESET signal to which said first counter means responds.

14. Image processing apparatus according to any of claims 11 to 13, including display means for displaying on a common screen two separate screen images each of which comprises a window formed in the other, and scrolling means for scrolling the point of division of the two images.

15. Image processing apparatus according to claim 14, wherein said scrolling means is arranged to respond to the count output of said first counter means, which count output represents the degree of scrolling - that is, the point of division of said two images.

16. Image processing apparatus according to claim 14 or 15, wherein said two images are arranged to occupy respectively a left and a right portion of said common screen, such that said point of division comprises a substantially upright line.



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17. Image processing apparatus according to claim 15 or 16, wherein said preset value of said second counter means represents said point of division being in a middle portion of said common screen.
