CLAIMS:

1. A circuit member including a frame substrate formed, by patterning a rolled copper plate or a rolled copper alloy plate, with a die pad portion for a semiconductor chip to be mounted thereon, and a lead portion for an electrical connection to the semiconductor chip, comprising:

rough surfaces formed as roughed surfaces on upsides and lateral wall sides of the die pad portion and the lead portion; and

smooth surfaces formed on downsides of the die pad portion and the lead portion, wherein

the die pad portion and the lead portion are configured to be buried in a sealing resin, having a downside of the lead portion exposed.

2. The circuit member as claimed in claim 1, comprising metallic skins formed on obverse surfaces of the die pad portion and the lead portion, for enhancement of connectability with a bonding wire and a solder paste.

3. A circuit member including a frame substrate formed, by patterning a rolled copper plate or a rolled copper alloy plate, with a die pad portion for a semiconductor chip to be mounted thereon, and a lead portion for an electrical connection to the semiconductor chip, comprising:

smooth surfaces formed on a portion of an upside of the die pad portion and on a portion of an upside of the lead portion to be connected to a bonding wire;

metallic skins on the smooth surfaces; and

rough surfaces formed on regions excepting downsides of the die pad portion and the lead portion and regions where the metallic skins are formed.

4. The circuit member as claimed in claim 3, wherein a metallic skin comprises an Ag skin.

5. The circuit member as claimed in claim 3, wherein a metallic skin comprises a Ni skin and a Pd skin laminated in order on the rolled copper plate.

6. The circuit member as claimed in claim 3, wherein a metallic skin comprises a Ni skin, a Pd skin, and an Au skin laminated in order on the rolled copper

plate.

7. The circuit member as claimed in claim 3, wherein a rough surface has a surface roughness (Ra) of 0.3 μm or more.

8. The circuit member as claimed in claim 4, wherein the Ag skin has a thickness within a range of 2 to 15 μm.

9. The circuit member as claimed in claim 5, wherein the Ni skin has a thickness within a range of 0.5 to 2 μm, and the Pd skin has a thickness within a range of 0.005 to 0.2 μm.

10. The circuit member as claimed in claim 6, wherein the Ni skin has a thickness within a range of 0.5 to 2 μm, the Pd skin has a thickness within a range of 0.005 to 0.2 μm, and the Au skin has a thickness within a range of 0.003 to 0.01 μm.

11. The circuit member as claimed in claim 1, wherein a rough surface is treated by a micro-etching solution having hydrogen peroxide and sulfuric acid as components.

12. A manufacturing method for circuit members, comprising:

forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled copper plate or a rolled copper alloy plate;

roughing upside surfaces and lateral wall surfaces of the frame substrate, using a micro-etching solution having hydrogen peroxide and sulfuric acid as components, with a making material covering downside surfaces of the frame substrate; and

having, past a removal of the masking material, metallic skins laminated on obverse surfaces of the frame substrate.

13. A manufacturing method for circuit members, comprising:

forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled copper plate or a rolled copper alloy plate;

laminating metallic skins on an upside surface of the die pad portion, and on a portion of the lead portion to be connected to a bonding wire;

surface-roughing the frame substrate, using a micro-etching solution having hydrogen peroxide and sulfuric acid as principal components, with a masking

material covering downside surfaces of the frame substrate having the metallic skins laminated thereon; and

removing the masking material.

14. The manufacturing method for circuit members as claimed in claim 12, wherein the step of laminating the metallic skins comprises laminating an Ag skin on an obverse surface of the frame substrate.

15. The manufacturing method for circuit members as claimed in claim 12, wherein the step of laminating the metallic skins comprises laminating a Ni skin and a Pd skin in order on an obverse surface of the frame substrate.

16. The manufacturing method for circuit members as claimed in claim 15, comprising laminating an Au skin on the Pd skin.

17. A semiconductor device comprising:

a circuit member composed of a rolled copper plate or a rolled copper alloy plate, comprising:

a die pad portion and a lead portion;

rough surfaces formed on upsides and lateral wall sides of the die pad portion and the lead portion;

smooth surfaces formed on downsides of the die pad portion and the lead portion; and

metallic skins on the surfaces;

a semiconductor chip mounted on an upside of the die pad portion;

a bonding wire interconnecting the semiconductor chip and the lead portion; and

an electrically insulating sealing resin configured to have the circuit member, the semiconductor chip, and the bonding wire sealed in, with a downside of the lead portion exposed.

18. A semiconductor device comprising:

a circuit member composed of a rolled copper plate or a rolled copper alloy plate, comprising:

a die pad portion and a lead portion;

smooth surfaces formed on an upside of the die pad portion, and on a portion of an obverse side of the lead portion to be connected to a bonding wire;

metallic skins on the smooth surfaces; and

rough surfaces formed on regions excepting reverse sides of the die pad portion and the lead portion and regions where the metallic skins are formed;

a semiconductor chip mounted on the upside of the die pad portion;

the bonding wire interconnecting the semiconductor chip and the lead portion; and

an electrically insulating sealing resin configured to have the circuit member, the semiconductor chip, and the bonding wire sealed in, with a downside of the lead portion exposed.

19. A surface lamination structure for a circuit member to be joined to an insulating resin, comprising:

a rough surface formed on an obverse side of a conductive substrate composed of a rolled copper plate or a rolled copper alloy, with a surface roughness (Ra) of 0.3 μm or more; and

a Ni skin and a Pd skin laminated in order on the rough surface, wherein

the Ni skin has a thickness within a range of 0.5 to 2 μm, and the Pd skin has a thickness within a range of 0.005 to 0.2 μm.

20. The surface lamination structure for a circuit member as claimed in claim 19, further comprising an Au skin laminated on the Pd skin, with a thickness within a range of 0.003 to 0.01 μm.

The invention claimed is:

1. A manufacturing method for circuit members, comprising:

forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled copper plate or a rolled copper alloy plate;

roughing upside surfaces and lateral wall surfaces of the frame substrate, using a micro-etching solution having hydrogen peroxide and sulfuric acid as components, with a making material covering bottom surfaces of the frame substrate; and

after a removal of the masking material, laminating metallic skins on the roughed upper surfaces, the roughed lateral wall surfaces and the bottom surface of the frame substrate simultaneously so that the metallic skins on roughed upper surfaces and the roughed lateral wall surfaces of the frame substrate have needle-shaped projections.

2. The manufacturing method for circuit members as claimed in claim 1, wherein the step of laminating the metallic skins comprises laminating an Ag skin on an obverse surface of the frame substrate.

3. The manufacturing method for circuit members as claimed in claim 1, wherein the step of laminating the metallic skins comprises laminating a Ni skin and a Pd skin in order on an obverse surface of the frame substrate.

4. The manufacturing method for circuit members as claimed in claim 3, comprising laminating an Au skin on the Pd skin.

5. A manufacturing method for circuit members, comprising:

forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled copper plate or a rolled copper alloy plate;

laminating metallic skins on a semiconductor chip mounting portion of an upper surface of the die pad portion, and on a portion of the lead portion to be connected to a bonding wire;

roughing upper surfaces and lateral surfaces of the die pad portion and the lead portion so as to selectively maintain a smooth surface of the semiconductor chip mounting portion, using a micro-etching solution having hydrogen peroxide and sulfuric acid as principal components, with a masking material covering entire bottom surfaces of the die pad portion and the lead portion;

and removing the masking material.

6. A manufacturing method for a semiconductor device, comprising:

forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled

copper plate or a rolled copper alloy plate;

roughing upper surfaces and lateral wall surfaces of the die pad portion and the lead portion, using a micro-etching solution having hydrogen peroxide and sulfuric acid as components, with a masking material covering bottom surfaces of the die pad portion and the lead portion and a part of the upper surfaces of the lead portion to be brought into contact with a resin sealing mold so as to maintain smooth surfaces;

after removal of the masking material, laminating metallic skins on obverse surfaces of the die pad portion and the lead portion;

mounting a semiconductor chip on the upper surface of the die pad portion;

connecting the semiconductor chip and the lead portion with a bonding wire and

molding the semiconductor chip with a sealing resin by contacting a resin sealing mold to the smooth surfaces of the part of the part of the upper surfaces of the lead portion and the smooth surface of the die pad portion and the lead portion.

7. A manufacturing method for a semiconductor device, comprising:

forming a frame substrate with a die pad portion and a lead portion, by patterning a rolled copper plate or a rolled copper alloy plate;

laminating metallic skins on an upper surface of the die pad portion, and on a portion of the lead portion to be connected to a bonding wire;

surface-roughing the die pad portion and the lead portion, using a micro-etching solution having hydrogen peroxide and sulfuric acid as principal components, with a masking material covering bottom surfaces of the die pad portion and the lead portion having the metallic skins laminated thereon and a part of the upper surfaces of the lead portion to be brought into contact with a resin sealing mold so as to maintain smooth surfaces;

removing the masking material;

mounting a semiconductor chip on the upper surface of the die pad portion;

connecting the semiconductor chip and the lead portion with a bonding wire; and

molding the semiconductor chip with a sealing resin by contacting a resin sealing mold to the smooth surfaces of the part of the upper surfaces of the lead portion and the smooth surfaces of the bottom surfaces of the die pad portion and the lead portion.