ABSTRACT

DUAL THREAD PROCESSOR

A pipeline processor architecture, processor, and methods are provided. In one implementation, a processor is provided that includes an instruction fetch unit operable to fetch instructions associated with a plurality of processor threads, a decoder responsive to the instruction fetch unit, issue logic responsive to the decoder, and a register file including a plurality of banks corresponding to the plurality of processor threads. Each bank is operable to store data associated with a corresponding processor thread. The processor can include a set of registers corresponding to each of a plurality of processor threads. Each register within a set is located either before or after a pipeline stage of the processor.

FIG. 3



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